

The TTL Data Book Volume 1

1987

**Standard TTL,
Low-Power Schottky, Schottky**



**TEXAS
INSTRUMENTS**

The TTL Data Book

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The TTL Data Book

Volume 1

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INTRODUCTION

In this volume, Texas Instruments presents pertinent technical information on the industry's broadest families of TTL integrated circuits.

You'll find complete specifications on the following product types:

- Standard TTL circuits
Series 54/74
- Schottky TTL circuits
Schottky clamped[†] Series 54LS/74LS and 54S/74S

This edition is designed for ease of circuit selection with an alphanumerical index as well as a functional index to all bipolar digital device types available or under development showing the available technologies for each type (Standard TTL, Schottky and Advanced Schottky, Low-Power Schottky and Advanced Low-Power Schottky). Included in the general information section is an explanation of the function tables, parameter measurement information, and typical characteristics related to the TTL products listed in this volume.

Package dimensions given in the Mechanical Data section of this book are in metric measurement (and parenthetically in inches) to simplify board layout for designers involved in metric conversion and new designs.

This volume is one in a series of Digital Bipolar data books available from Texas Instruments. The complete series is listed below:

- The TTL Data Book, Volume 1
Standard TTL, Schottky, Low-Power Schottky
- The TTL Data Book, Volume 2
Advanced Low-Power Schottky, Advanced Schottky
- The TTL Data Book, Volume 3
Bipolar Programmable Logic and Memory

Complete technical data for any TI semiconductor/component products are available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing Information Services, Texas Instruments Incorporated, P.O. Box 225012, MS 308, Dallas, Texas 75265.

We sincerely hope you will find the new TTL Data Book, Volume 1, a meaningful addition to your technical library.

[†] Integrated Schottky Barrier diode clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max}	Maximum clock frequency The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
I_{CC}	Supply current The current into* the V _{CC} supply terminal of an integrated circuit.
I_{CCH}	Supply current, outputs high The current into* the V _{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.
I_{CCL}	Supply current, outputs low The current into* the V _{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.
I_{IH}	High-level input current The current into* an input when a high-level voltage is applied to that input.
I_{IL}	Low-level input current The current into* an input when a low-level voltage is applied to that input.
I_{OH}	High-level output current The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
I_{OL}	Low-level output current The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.
I_{OS}	Short-circuit output current The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).
I_{OZH}	Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

* Current out of a terminal is given as a negative value.

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GLOSSARY TTL SYMBOLS, TERMS, AND DEFINITIONS

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I_{OZL}	Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.
V_{IH}	High-level input voltage An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IK}	Input clamp voltage An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.
V_{IL}	Low-level input voltage An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{OH}	High-level output voltage The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.
V_{OL}	Low-level output voltage The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.
t_a	Access time The time interval between the application of a specific input pulse and the availability of valid signals at an output.
t_{dis}	Disable time (of a three-state output) The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t _{dis} = t _{PHZ} or t _{PLZ}).
t_{en}	Enable time (of a three-state output) The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t _{en} = t _{PZH} or t _{PZL}).

*Current out of a terminal is given as a negative value.

GLOSSARY TTL SYMBOLS, TERMS, AND DEFINITIONS

t_h	Hold time The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.
t_{pd}	Propagation delay time The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL} \text{ or } t_{PLH}$).
t_{PHL}	Propagation delay time, high-to-low-level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{PHZ}	Disable time (of a three-state output) from high level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.
t_{PLH}	Propagation delay time, low-to-high-level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PLZ}	Disable time (of a three-state output) from low level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.
t_{PZH}	Enable time (of a three-state output) to high level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.
t_{PZL}	Enable time (of a three-state output) to low level The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.
t_{sr}	Sense recovery time The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.
t_{su}	Setup time The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal. NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
t_w	Pulse duration (width) The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

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GENERAL INFORMATION

GLOSSARY TTL SYMBOLS, TERMS, AND DEFINITIONS

PART II — CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.



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GENERAL INFORMATION

EXPLANATION OF FUNCTION TABLES



Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q ₀	=	level of Q before the indicated steady-state input conditions were established
\bar{Q}_0	=	complement of Q ₀ or level of \bar{Q} before the indicated steady-state input conditions were established
Q _n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at output Q_B, and so forth, following a low-to-high clock transition.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \bar{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Q₀ and \bar{Q}_0 are now at Q_A and Q_B respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

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GENERAL INFORMATION

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE														
CLEAR	MODE		INPUTS								OUTPUTS			
			CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	
	S ₁	S ₀		LEFT	RIGHT	A	B	C	D					
L	X	X	X	X	X	X	X	X	X	L	L	L	L	
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	
H	H	H	↑	X	X	a	b	c	d	a	b	c	d	
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H	
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L	
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S₁ and S₀ are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

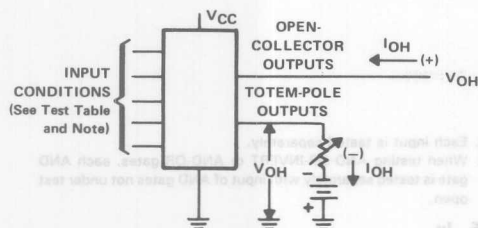
The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S₁ is low and S₀ is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S₁ is high and S₀ is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

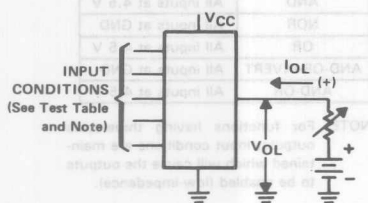
SERIES 54/74, 54H/74H, 54L, 54LS/74LS, 54S/74S TRANSISTOR-TRANSISTOR LOGIC

PARAMETER MEASUREMENT INFORMATION



NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 1. V_{IH} , V_{IL} , V_{OH} , I_{OH}



NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 2. V_{IH} , V_{IL} , V_{OL}

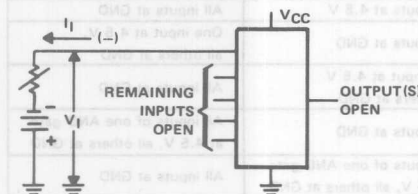


FIGURE 3. V_I

FUNCTION	INPUT CONDITIONS
NAND	Input under test at V_{IL} max, all others at 4.5 V
AND	All inputs at V_{IH} min
NOR	All inputs at V_{IL} max
OR	Input under test at V_{IH} min, all others at GND
AND-OR	Inputs under test (a set including one input of each AND gate) at V_{IL} max, all others at 4.5 V
INVERT	All inputs of AND gate under test at V_{IH} min, all others at GND

FUNCTION	INPUT CONDITIONS
NAND	All inputs at V_{IH} min
AND	Input under test at V_{IL} max, all others at 4.5 V
NOR	Input under test at V_{IH} min, others at GND
OR	All inputs at V_{IL} max
AND-OR	All inputs of AND gate under test at V_{IH} min, all others at GND
INVERT	Inputs under test (a set including one input of each AND gate) at V_{IH} min, all others at 4.5 V

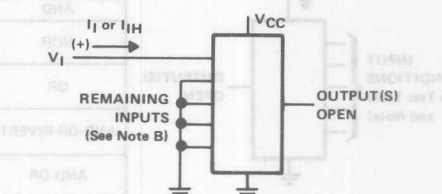


FIGURE 4. I_I , I_{IH}

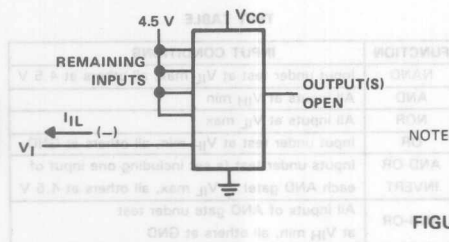
NOTE: Each input is tested separately.
 A. Each input is tested separately.
 B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open when testing I_I and grounded when testing I_{IH} .

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GENERAL INFORMATION

PARAMETER MEASUREMENT INFORMATION

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- NOTES:
- Each input is tested separately.
 - When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with input of AND gates not under test open.

FIGURE 5. I_{IL}

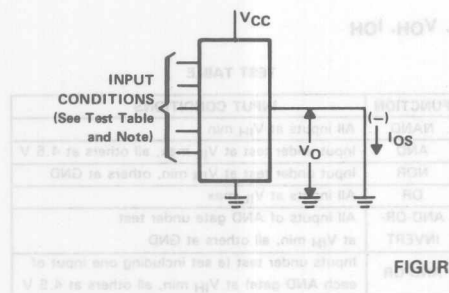
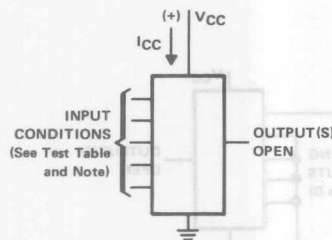


FIGURE 6. I_{OS}, I_O

TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at GND
AND	All inputs at 4.5 V
NOR	All inputs at GND
OR	All inputs at 4.5 V
AND-OR-INVERT	All inputs at GND
AND-OR	All inputs at 4.5 V

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).



TEST TABLE

FUNCTION	INPUT CONDITIONS FOR I_{CCH}	INPUT CONDITIONS FOR I_{CCL}
NAND	All inputs at GND	All inputs at 4.5 V
AND	All inputs at 4.5 V	All inputs at GND
NOR	All inputs at GND	One input at 4.5 V, all others at GND
OR	One input at 4.5 V, all others at GND	All inputs at GND
AND-OR-INVERT	All inputs at GND	All inputs of one AND gate at 4.5 V, all others at GND
AND-OR	All inputs of one AND gate at 4.5 V, all others at GND	All inputs at GND

NOTE: I_{CC} is measured simultaneously for all functions in a package. The average-per-gate values are calculated from the appropriate one of the following equations:

$$I_{CC}, I_{CCH}, \text{ or } I_{CCL} \text{ (average per gate or flip-flop)} = \frac{\text{total } I_{CC}, I_{CCH}, \text{ or } I_{CCL}}{\text{(number of gates or flip-flops in package)}}$$

$$I_{CC} \text{ (average per gate, 50% duty cycle)} = \frac{I_{CCH} + I_{CCL}}{2 \text{ (number of gates in package)}}$$

FIGURE 7. I_{CC}

PARAMETER MEASUREMENT INFORMATION

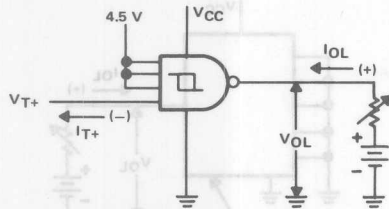


FIGURE 8. V_{T+} , I_{T+} , V_{OL}
(FOR NAND SCHMITT TRIGGERS)

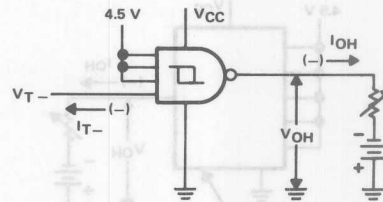


FIGURE 9. V_{T-} , I_{T-} , V_{OH}
(FOR NAND SCHMITT TRIGGERS)

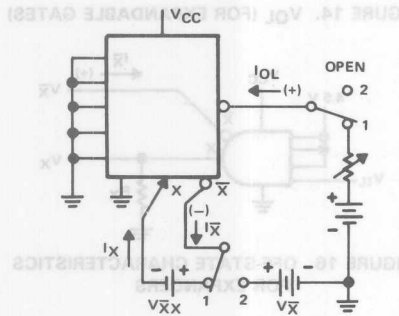


FIGURE 10. I_X (FOR EXPANDABLE GATES)

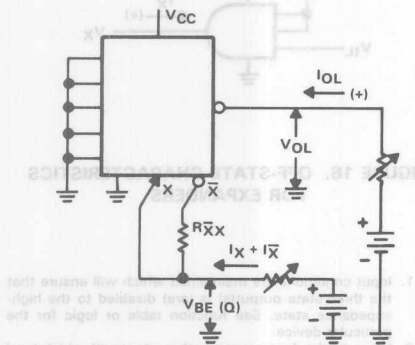


FIGURE 11. $V_{BE(Q)}$ (FOR EXPANDABLE GATES)

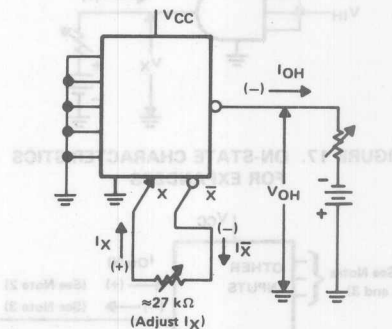


FIGURE 12. V_{OH} (FOR EXPANDABLE GATES)

- NOTES: A. Switches are in position 1 for SN54'/SN74', position 2 for SN54H'/SN74H'.
- B. The I_X limit for SN54' and SN74' circuits may be verified by an alternate equivalent procedure. The V_{XX} source is replaced by a resistor (see table below) in parallel with a voltmeter between the X and \bar{X} pins. If the measured voltage, V_{XX} , is less than 0.4, the specified limit for I_X is met.

RESISTANCE VALUE TABLE

SN5423	114 Ω
SN5450, SN5453	138 Ω
SN7423	105 Ω
SN7450, SN7453	130 Ω

PARAMETER MEASUREMENT INFORMATION

1 GENERAL INFORMATION

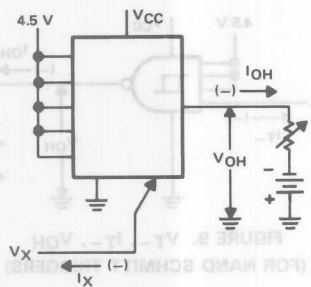


FIGURE 13. V_{OH} (FOR EXPANDABLE GATES)

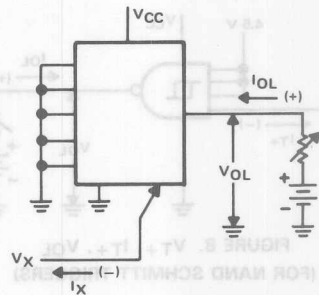


FIGURE 14. V_{OL} (FOR EXPANDABLE GATES)

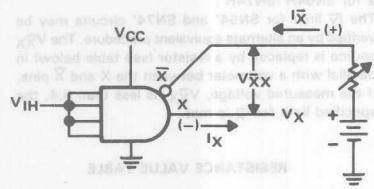


FIGURE 15. ON-STATE CHARACTERISTICS FOR EXPANDERS

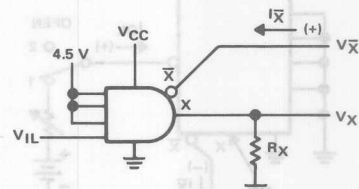


FIGURE 16. OFF-STATE CHARACTERISTICS FOR EXPANDERS

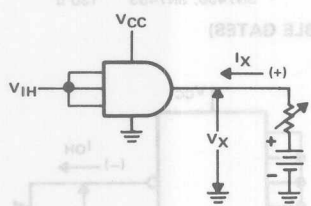


FIGURE 17. ON-STATE CHARACTERISTICS FOR EXPANDERS

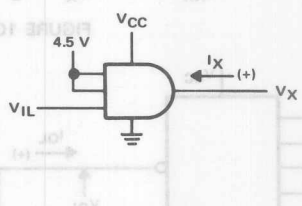


FIGURE 18. OFF-STATE CHARACTERISTICS FOR EXPANDERS

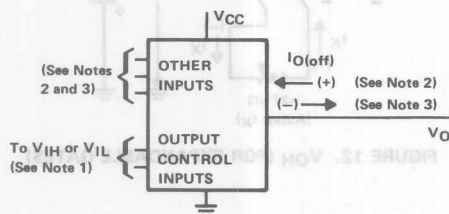
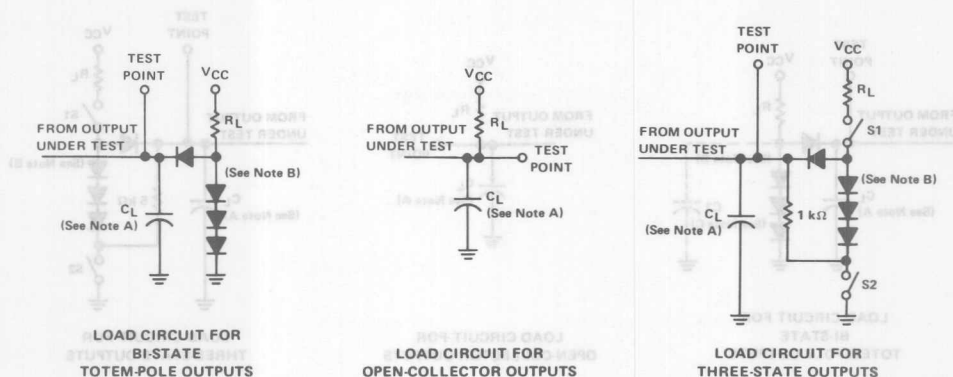


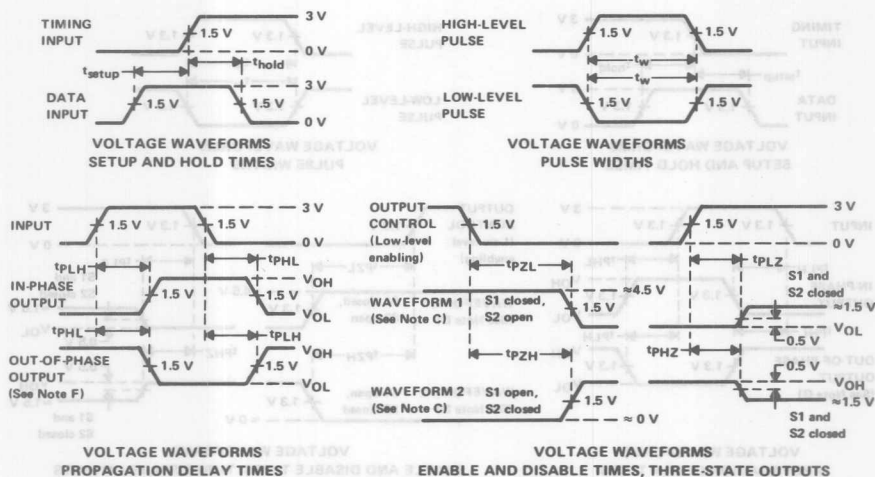
FIGURE 19. $I_{O(off)}$ (THREE-STATE OUTPUTS)

- NOTES: 1. Input conditions are maintained which will ensure that the three-state output(s) is (are) disabled to the high-impedance state. See function table or logic for the particular device.
2. When testing for current into the output with a high-level output voltage, input conditions are applied that would cause the output to be low if it were enabled.
3. When testing for current out of the output with a low-level output voltage, input conditions are applied that would cause the output to be high if it were enabled.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.



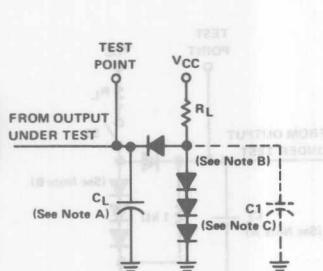
NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$ and:
For Series 54/74 and 54H/74H, $t_r \leq 7 \text{ ns}$, $t_f \leq 7 \text{ ns}$;
For Specified[†] Series 54L/74L devices: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$;
For Series 54S/74S, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
G. The outputs are measured one at a time with one input transition per measurement.

[†]L42, 'L43, 'L44, 'L46, 'L47, 'L75, 'L77, 'L96, 'L121, 'L122, 'L123, 'L153, 'L154, 'L157, 'L164

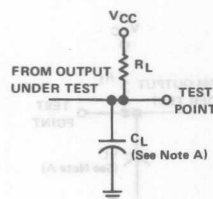
PARAMETER MEASUREMENT INFORMATION

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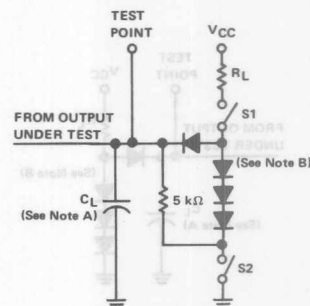
GENERAL INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

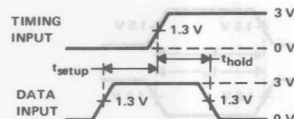


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

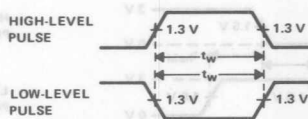


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

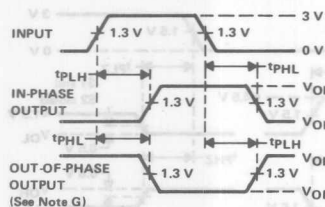
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. C_1 (30 pF) is used for testing Series 54L devices only.



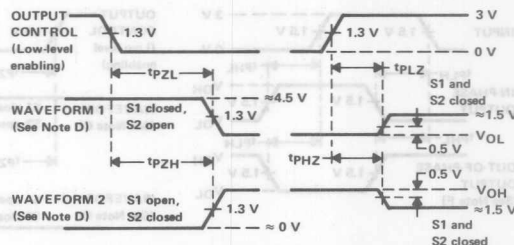
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$ and:
For Series 54L/74L gates and inverters, $t_r = 60$ ns, $t_f = 60$ ns;
For Series 54L/74L flip-flops and MSI, $t_r \leq 25$ ns, $t_f \leq 25$ ns;
For Series 54LS/74LS, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
H. The outputs are measured one at a time with one input transition per measurement.

[†]L42, L43, L44, L46, L47, L75, L77, L96, L121, L122, L123, L153, L154, L157, L164

TYPICAL CHARACTERISTICS†

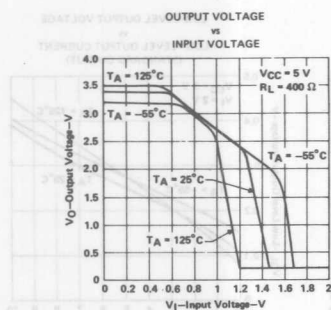


FIGURE A1

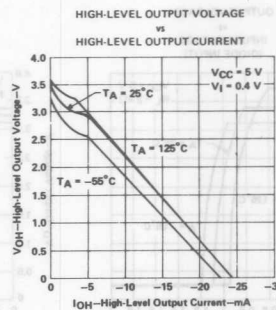


FIGURE A2

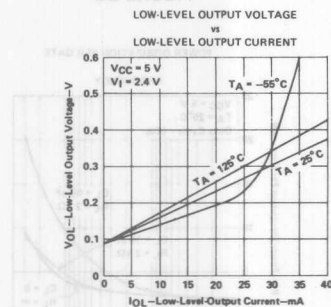


FIGURE A3

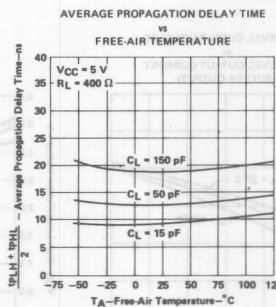


FIGURE A4

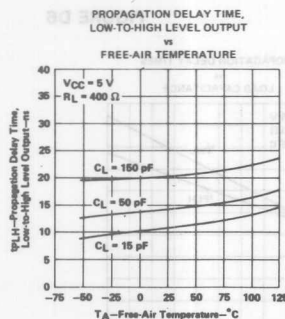


FIGURE A5

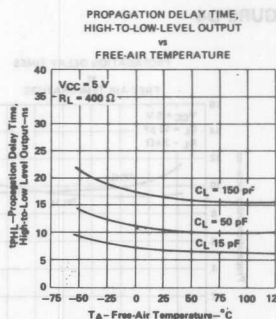


FIGURE A6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54 circuits only.
Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†

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GENERAL INFORMATION

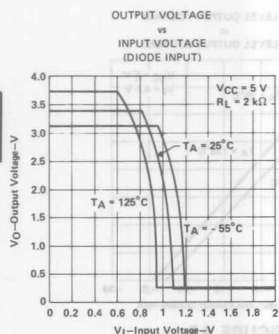


FIGURE D1

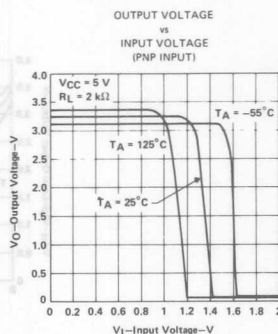


FIGURE D2

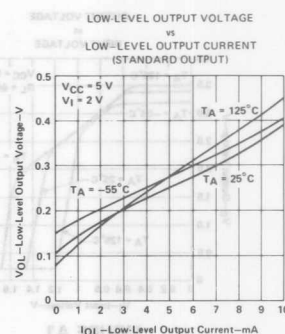


FIGURE D3

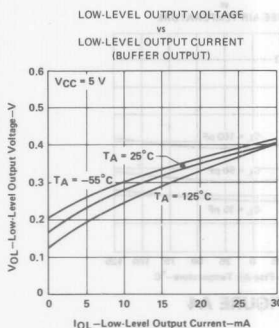


FIGURE D4

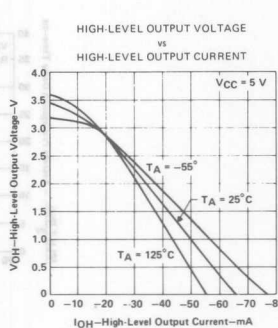


FIGURE D5

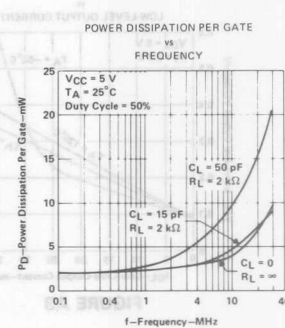


FIGURE D6

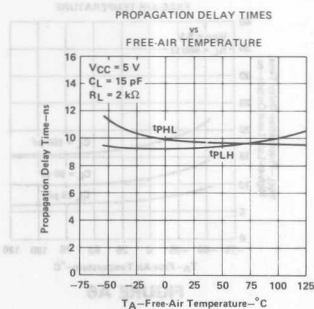


FIGURE D7

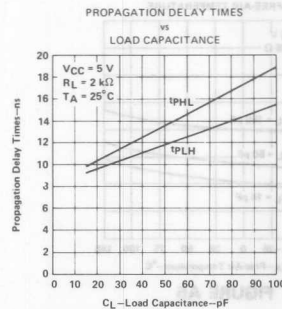


FIGURE D8

†Data for temperatures below 0°C and above 70°C are applicable for Series 54LS circuits only.

SERIES 54S/74S SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS†

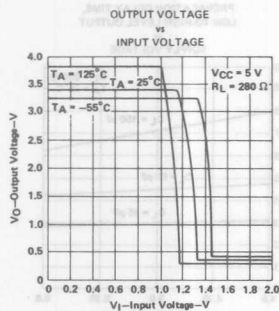


FIGURE E1

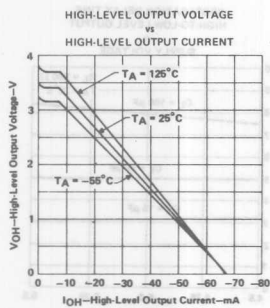


FIGURE E3

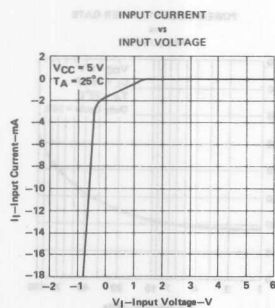


FIGURE E5

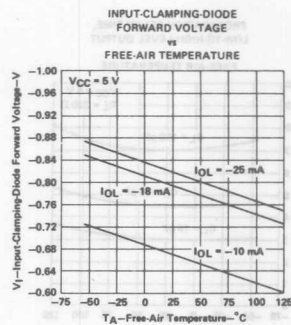


FIGURE E2

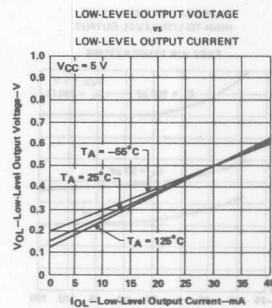


FIGURE E4

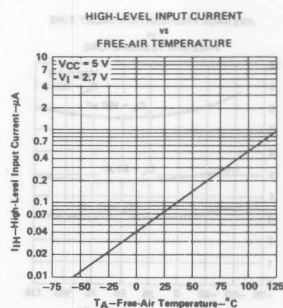


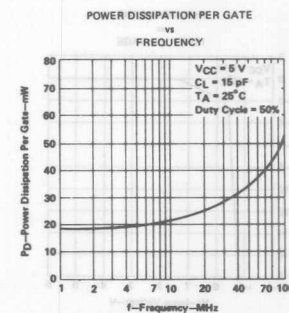
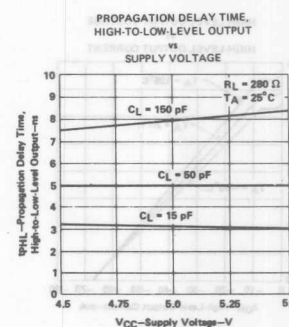
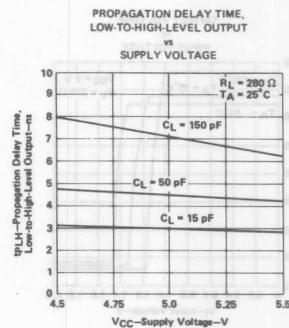
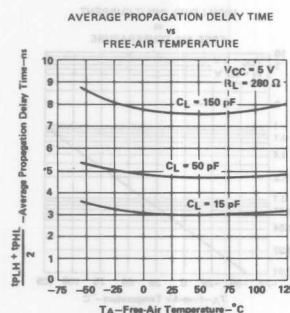
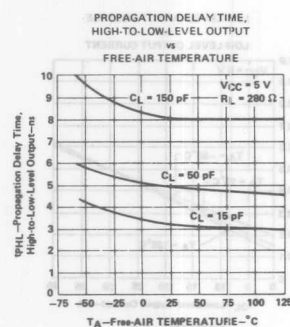
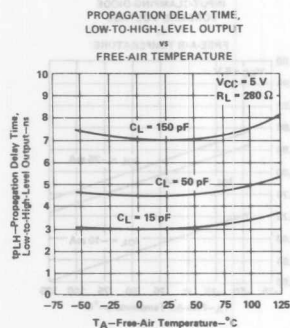
FIGURE E6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†

1

GENERAL INFORMATION



†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

SERIES 54S/74S
SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

TYPICAL CHARACTERISTICS FOR FLIP-FLOPS†

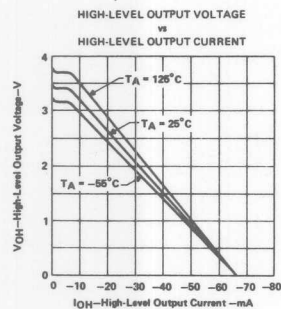


FIGURE E13

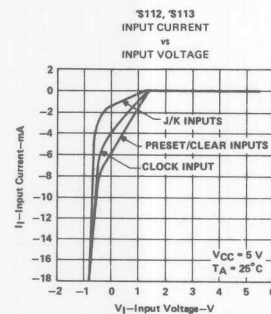


FIGURE E15

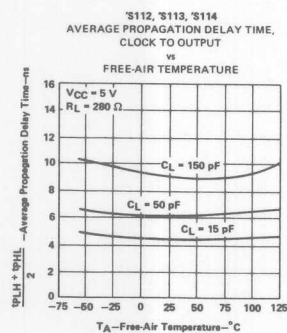


FIGURE E17

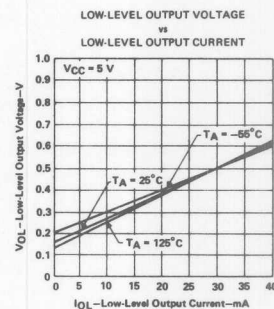


FIGURE E14

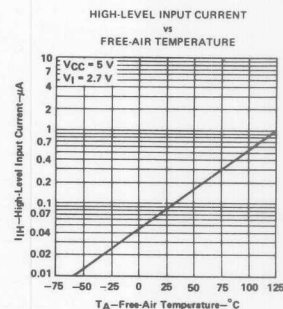


FIGURE E16

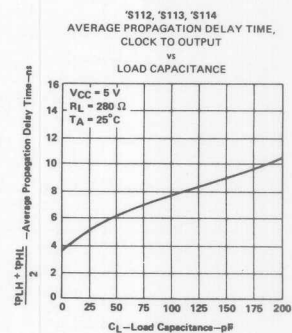


FIGURE E18

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.

General Information

1

Functional Index

2

TTL Devices

3

Mechanical Data

4

- All STD TTL, LS and Schottky Devices are included in TTL-Data Book Volume 1
- All ALS and AS Devices are included in TTL-Data Book Volume 2
- All PAL's® and Bipolar Memories are included in TTL-Data Book Volume 3

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Functional Index

FUNCTIONAL INDEX

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GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2 Input Gates	'804	•	B			
Hex Inverters	'04	•	A	•		•
	'1004	•	•			
Quadruple 2 Input Gates	'00	•	A	•		•
	'1000	•	A	•		
Triple 3 Input Gates	'10	•	A	•		•
	'1010	•	A			
Dual 4 Input Gates	'20	•	A	•		•
	'1020	•	A			
8 Input Gates	'30	•	A	•		•
13 Input Gates	'133	•				•
Dual 2 Input Gates	'8003	•				

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex Inverters	'05	•	A			•
	'1005	•				
	'01	•	•			•
Quadruple 2-Input Gates	'03	•	A			•
	'1003	•	A			
	'12	•	A			•
Triple 3-Input Gates	'12	•	A			•
	'22	•	B			•

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'808	•	•	B		•
Quadruple 2-Input Gates	'08	•	•	•		•
	'1008	•	A	•		
Triple 3-Input Gates	'11	•	A	•		•
	'1011	•	A			•
Dual 4-Input Gates	'21	•	•	•		•
Triple 4-Input AND/NAND	'800	•		•		

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quadruple 2-Input Gates	'09	•			•	•
Triple 3-Input Gates	'15	•	•		•	•
		•	A			

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'832	•	•	B		
Quadruple 2-Input Gates	'32	•	•	•		•
	'1032	•	A	•		
Triple 4-Input OR/NOR	'802	•		•		

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Gates	'805	•	•	B		
Quadruple 2-Input Gates	'02	•	•	•		•
	'1002	•	A			
Triple 3-Input Gates	'27	•	•	•		•
		•	•	•		
Dual 4-Input Gates with Strobe	'25	•				
Dual 5-Input Gates	'260	•				•

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex Inverters	'14	•				•
	'19	•				•
Octal Inverters	'619	•				•
Dual 4-Input Positive-NAND	'13	•				•
	'18	•				•
Triple 4-Input Positive-NAND	'618	•				•
	'24	•				•
Quadruple 2-Input Positive-NAND	'132	•	•			•

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY		
		ALS	AS	LS
Hex	'63			•

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY		
		ALS	AS	LS
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31			•

A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.

FUNCTIONAL INDEX

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
2-Wide 4-Input	'55				•	
4-Wide 4-2-3-2-Input	'64					•
4-Wide 2-2-3-2-Input	'54					
4-Wide 2-Input	'54	•				
4-Wide 2-3-3-2-Input	'54				•	
Dual 2-Wide 2-Input	'51	•			•	•

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
4-Wide 4-2-3-2-Input	'65					•

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Dual 4-Input Positive-NOR With Strobe	'23	•				
4-Wide AND-OR	'52					
4-Wide AND-OR-INVERT	'53	•				
2-Wide AND-OR-INVERT	'55					•
Dual 2-Wide AND-OR-INVERT	'50	•				

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Dual 4-Input	'60	•				
Triple 3-Input	'61					
3-2-2-3-Input AND-OR	'62					

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex	'07	•				
	'17	•				
	'35		•			
Hex Inverter	'1035	•				
	'06	•				
	'16	•				
Quad 2-Input Positive-NAND	'1005	•				
	'26	•			•	
	'38	•		A,B		•
	'39	•				•
	'1003	•	A			
Quad 2-Input Positive-NOR	'33	•	A			

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Noninverting Octal Buffers/Drivers	'743	•				
	'757	•	•			
	'760	•				
Inverting Octal Buffers/Drivers	'742	•				
	'756	•		•		
	'763	•	•			
Inverting and Noninverting Octal Buffers/Drivers	'762	•	•			
	'759	•				
Noninverting Quad Transceivers	'759			•		
Inverting Quad Transceivers	'758			•		

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Noninverting Octal Buffers/Drivers	'241		A	•		•
	'244		A	•		•
	'465		A		•	
	'467		A		•	
	'541		•			•
	'1241*		•			
	'1244*		A			
Inverting Octal Buffers/Drivers	'231		•	•		•
	'240		A	•		•
	'466		A		•	
	'468		A		•	
	'540		•			•
Inverting and Noninverting Octal Buffers/Drivers	'1240*		•			
	'230			•		
Octal Transceivers	'245		A	•		
	'1245		A			
Noninverting Hex Buffers/Drivers	'365		A		A	
	'367		•		A	
	'366		A		A	
Inverting Hex Buffers/Drivers	'368		A		A	
	'125	•			A	
	'126	•			A	
Quad Buffers/Drivers with Independent Output Controls	'425	•				
	'426	•				
	'243		A	•		
Noninverting Quad Transceivers	'1243*		•			
	'242		A,B	•		
	'1242*		•			
Inverting Quad Transceivers	'226					•
	'134					•

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Positive-NAND	'804			•	B	
Hex 2-Input Positive-NOR	'805			•	B	
Hex 2-Input Positive-AND	'808			•	B	
Hex 2-Input Positive-OR	'832			•	B	
Quad 2-Input Positive-NOR	'128	•				
Dual 4-Input Positive-NAND	'140					•

* Denotes very low power.
A Denotes "A" suffix version available in the technology indicated.

BUFFERS, DRIVERS, TRANSCIEVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Hex 2-Input Positive NAND	'804	●	B			
Hex 2-Input Positive NOR	'805	●	B			
Hex 2-Input Positive AND	'808	●	B			
Hex 2-Input Positive OR	'832	●	B			
Hex Inverter	'1004	●	●			
Hex Buffer	'1034	●	●			
Quad 2-Input Positive NAND	'137	●	A			●
	'1000		A	●		
Quad 2-Input Positive NOR	'28	●	A			●
	'1002		A			
	'1036		●			
Quad 2-Input Positive AND	'1008		A	●		
Quad 2-Input Positive OR	'1032		A	●		
Triple 3-Input Positive NAND	'1010		A			
Triple 3-Input Positive AND	'1011		A			
Triple 4-Input AND-NAND	'800			●		
Triple 4-Input OR-NOR	'802			●		
Dual 4-Input Positive NAND	'40	●	A			●
	'1020		A			
Line Driver/Memory Driver with Series Damping Resistor	'436					●
Line Driver/Memory Driver	'437					●

BI-/TRI-DIRECTIONAL BUS TRANSCIEVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			
			ALS	AS	LS	S
Quad with Bit Direction	3-State	'446			●	
Controls	3-State	'449			●	
	OC	'440			●	
	OC	'441			●	
Quad Tridirection	3-State	'442			●	
	3-State	'443			●	
	3-State	'444			●	
	OC	'448			●	
4-Bit with Storage	3-State	'226				●

OCTAL BUS TRANSCIEVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY			
		STD TTL	ALS	AS	S
Inverting Outputs, 3-State	'2620		●		
	'2640		●		
True Outputs, 3-State	'2623		●		
	'2645		●		

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/OUTPUT RESISTORS

DESCRIPTION	TYPE	TECHNOLOGY			
		STD TTL	ALS	AS	S
Input Resistors	Inverting Outputs	'746	●		
	Noninverting Outputs	'747	●		
Output Resistors	Inverting Outputs	'2540	●		
	Noninverting Outputs	'2541	●		

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCIEVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY		
			ALS	AS	LS
12 mA 24 mA 48 mA 64 mA Sink, True Outputs	Low Power	3-State	245	●	●
		OC	621	●	●
		3-State	623	●	●
	Very Low Power	OC, 3-State	639	●	●
		3-State	652	●	●
		OC, 3-State	654	●	●
12 mA 24 mA 48 mA 64 mA Sink, Inverting Outputs	Low Power	OC	1621	●	●
		3-State	1623	●	●
		OC, 3-State	1639	●	●
	Very Low Power	3-State	620	●	●
		OC	622	●	●
		OC, 3-State	638	●	●
12 mA 24 mA 48 mA 64 mA Sink, True Outputs	Low Power	3-State	651	●	●
		OC, 3-State	653	●	●
	Very Low Power	3-State	1620	●	●
		OC	1622	●	●
		OC, 3-State	1638	●	●
	OC	641	●	●	●
12 mA 24 mA 48 mA 64 mA Sink, Inverting Outputs	Low Power	3-State	645	●	●
	Very Low Power	OC	1641	●	●
		3-State	1645	●	●
	Low Power	3-State	640	●	●
	Very Low Power	OC	642	●	●
		3-State	1640	●	●
12 mA 24 mA 48 mA 64 mA Sink, True and Inverting Outputs	Low Power	3-State	643	●	●
	Very Low Power	OC	644	●	●
		3-State	1643	●	●
	Very Low Power	OC	1644	●	●
		3-State	646	●	●
		OC	647	●	●
Registered with Multiplexed 12 mA 24 mA 48 mA 64 mA Inverting Outputs	3-State	648	●	●	●
	OC	649	●	●	●
		977	●	●	●
Universal Transceiver Port Controllers	3-State	852	●	●	●
		856	●	●	●

A Denotes "A" suffix version available in the technology indicated.

FUNCTIONAL INDEX

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Functional Index

FLIP-FLOPS, TRANS AND CLOCK GENERATORS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Dual J K Edge Triggered	73	●			A	
	76				A	
	78				A	
	103					
	106					
	107	●			A	
	108					
	109	●			A	
			A	●		
	112		A	●		A ●
Single J K Edge Triggered	101		A			A ●
	102		A	●		A ●
	113		A	●		A ●
	114		A	●		A ●
Dual Pulse Triggered	70	●				
	73	●				
	76	●				
Single Pulse Triggered	78	●				
	107	●				
	71	●				
	72	●				
Dual J K with Data Lockout	104	●				
	105	●				
	111	●				
Single J K with Data Lockout	110	●				
	110	●				
Dual D Type	74		A	●		A ●

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
D Type	6	Q		174	●		●	●
				378				●
				171				●
	4	Q, Q̄		175	●		●	●
				379				●
				176				●
J K	4	Q		276	●			
				376	●			

OCTAL, 9 BIT, AND 10 BIT D TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
True Data	Octal	3 State		374		●	●	●
				574		●	●	●
True Data with Clear	Octal	3 State		273	●		●	●
				575		●	●	●
				874		●	●	●
				878		●	●	●
True with Enable	Octal	2 State		377			●	●
				534		●	●	●
Inverting	Octal	3 State		564		●	●	●
				576		●	●	●
Inverting with Clear	Octal	3 State		577		●	●	●
				879		●	●	●
Inverting with Preset	Octal	3 State		876		●	●	●
				876		●	●	●
True	Octal	3 State		825			●	●
Inverting	Octal	3 State		826			●	●
True	9 Bit	3 State		823			●	●
Inverting	9 Bit	3 State		824			●	●
True	10 Bit	3 State		821			●	●
Inverting	10 Bit	3 State		822			●	●

A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.

LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Dual 2 Bit	2 State	'75	•				•
Transparent	2 State	'77	•				•
	2 State	'375					•
S R	2 State	'279	•				A

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Single	'122	•				•
	'130	•				•
	422					•
Dual	'123	•				•
	423					•

D TYPE

OCTAL, 9-BIT, AND 10-BIT RAD-BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Edge Triggered Inverting and Noninverting	Octal	'996		•			
	Octal	'990		•			
Transparent True	9 Bit	'992		•			
	10 Bit	'994		•			
	Octal	'991		•			
Transparent Noninverting	9 Bit	'992		•			
	10 Bit	'994		•			
Transparent with Clear True Outputs	Octal	'666		•			
Transparent with Clear Inverting Outputs	Octal	'667		•			

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
Transparent	Octal	3 State	'268					•
			'373					•
		3 State	'573		•	•		
Dual 4 Bit Transparent	Octal	2 State	'100	•				
		2 State	'116	•				
		3 State	'873		•	•		
Inverting Transparent	Octal	3 State	'533		•	•		
		3 State	'563		•	•		
		3 State	'580		•	•		
Dual 4 Bit Inverting Transparent	Octal	3 State	'880		•	•		
		3 State	'604					•
		OC	'605					•
2 Input Multiplexed	Octal	3 State	'606					•
		OC	'607					•
		2 State	'259	•				•
Addressable	Octal	3 State	'412		•	•		•
		3 State	'945		•	•		
True	Octal	3 State	'946		•	•		
Inverting	Octal	3 State	'946		•	•		
True	9 Bit	3 State	'943		•	•		
Inverting	9 Bit	3 State	'944		•	•		
True	10 Bit	3 State	'941		•	•		
Inverting	10 Bit	3 State	'942		•	•		

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Single	'121	•				
Dual	'221	•				

8-BIT REGISTER WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•
8-Bit Register with Latches	8	3 State	'613				•
		3 State	'613				•</

FUNCTIONAL INDEX

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Functional Index

REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TECHNOLOGY					
		EN	SR	Q	LOAD	TYPE	STD TTL	ALS	AS	LS	S
		0	1	2	3						
Sign Protected		X	X	X	X	'322				A	
Parallel-In, Parallel-Out, Bidirectional	8	X	X	X	X	'298					•
		X	X	X	X	'299					•
	4	X	X	X	X	'184				A	•
Parallel-In, Parallel-Out, Registered Outputs	4	X	X	X	X	'671					•
		X	X	X	X	'672					•
	8	X	X	X	X	'199					•
	5	X	X			'96					•
		X	X			'95	A			B	
		X	X			'99					•
		X	X	X	X	'178					•
		X	X	X	X	'179					•
		X	X			'195				A	•
		X	X			'295				B	
		X	X			'395				A	
Serial-In, Parallel-Out	16	X	X	X	X	'673					•
	8	X				'164					•
	16	X	X	X	X	'674					•
Parallel-In, Serial-Out	8	X	X	X	X	'165					•
		X	X	X	X	'166				A	
Serial-In, Serial-Out	8	X				'91	A				•
	4	X	X			'94					•

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY		
				ALS	AS	LS
Parallel-In, Parallel-Out with Output Latches	4	3 State	'671			•
		3 State	'672			•
	16	2 State	'673			•
Serial-In, Parallel-Out with Output Latches		Buffered	'594			•
		3 State	'595			•
	8	OC	'596			•
		OC	'599			•
Parallel-In, Serial-Out, with Input Latches	8	2 State	'597			•
		3 State	'589			•
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3 State	'598			•

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SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	EN	SR	Q	LOAD	TYPE	ALS	AS	LS
Sign Protected Register	8	X	X	X	X	'322			A

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY			
			STD TTL	ALS	AS	LS
8 Words x 2 Bits	3 State	'172	•			
	OC	'170	•			•
4 Words x 4 Bits	3 State	'670				•
	3 State	'870				•
Dual 16 Words x 4 Bits	3 State	'871			•	

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY					
		STD TTL	ALS	AS	LS	S	
		98					
Quadruple Multiplexers with Storage		'298	•				•
		'398					•
		'399					•
8 Bit Universal Shift Registers		'299		•	•		•
Quadruple Bus Buffer Registers		'173	•				A
Octal Storage Register		'396					•

COUNTERS

SYNCHRONOUS COUNTERS - POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Decade	Sync	'160	●	B	●	A	
		'162	●	B	●	A	●
		'560		A			
	Sync	'668				●	
		'690				●	
		'692				●	
Decade Up/Down	Sync	'168		B	●		●
		'190	●			●	
		'192	●			●	
	Sync	'568		A			
		'696				●	
		'698				●	
Decade Rate Multiplier, N10	Async	Set-to-9	'167	●			
4 Bit Binary	Sync	'161	●	B	●	A	
		'163	●	B	●	A	●
		'561		A			
	Sync	'669				●	
		'691				●	
		'693				●	
4 Bit Binary Up/Down	Sync	'169		B	●		●
		'191	●			●	
		'193	●			●	
	Sync	'569		A			
		'697				●	
		'699				●	
6 Bit Binary Rate Multiplier, N2	Async CLR	'97	●				
8 Bit Up/Down	Sync CLR	'867				●	
		'869				●	

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) - NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY				
			STD TTL	ALS	AS	LS	S
Decade	Set to 9	'90	A			●	
		'68				●	
	Yes	'176	●				
		'196	●			●	●
4 Bit Binary	Set to 9	'290	●			●	
		'93	A			●	
	None	'69				●	
		'177	●			●	●
Divide by 12	None	'197	●			●	●
		'293	●			●	
Dual Decade	None	'92	A			●	
		'390	●			●	
Dual 4 Bit Binary	Set to 9	'490	●			●	
		'393	●			●	

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY		
			ALS	AS	LS
Parallel Register	3-State	'590			●
Outputs	OC	'591			●
Parallel Register Inputs	2-State	'592			●
Parallel I/O	3-State	'593			●

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY			
		STD TTL	ALS	AS	LS
50-to-1 Frequency Divider	'56				●
60-to-1 Frequency Divider	'57				●
60 Bit Binary Rate Multiplier	'97	●			
Decade Rate Multiplier	'167	●			

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FUNCTIONAL INDEX

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS									
DESCRIPTION	TYPE OF OUTPUT	TYPE	STD TTL	ALS	AS	LS	S	TECHNOLOGY	
16 To 1	2 State	150	●						
	3 State	250			●				
	3 State	850			●				
	3 State	851			●				
Dual 8 To 1	3 State	351	●						
8 To 1	2 State	151	A		●	●			
	2 State	152	A		●	●			
	3 State	251		●	●				
	3 State	354				●			
	2 State	355				●			
	3 State	356				●			
	OC	357				●			
Dual 4 To 1	2 State	153		●	●	●			
	3 State	253		●	●	●			
	2 State	352		●	●	●			
	3 State	353		●	●	●			
Octal 2 To 1 with Storage	3 State	604				●			
	OC	605				●			
	3 State	606				●			
	OC	607				●			
Quad 2 To 1 with Storage	2 State	98		●		●			
	2 State	298				●			
	2 State	398				●			
	2 State	399				●			
Quad 2 To 1	2 State	157		●	●	●			
	2 State	158		●	●	●			
	3 State	257		A	●	●	●		
	3 State	258		A	●	●	●		
6 to 1 Universal Multiplexer	3 State	857		●	●				

DECODERS/DEMULIPLEXERS									
DESCRIPTION	TYPE OF OUTPUT	TYPE	STD TTL	ALS	AS	LS	S	TECHNOLOGY	
4 To 16	3 State	154	●						
	OC	159	●						
4 To 10 BCD To Decimal	2 State	42	A				●		
4 To 10 Excess 3 To Decimal	2 State	43	A						
4 To 10 Excess 3 Gray To Decimal	2 State	44	A						
3 To 8 with Address Latches		131		●	●				
	2 State	137		●	●				
3 To 8	2 State	138		●	●				
	3 State	538		●	●				
Dual 2 To 4	2 State	139				A	●		
	2 State	155	●			A			
Dual 1 To 4 Decoders	OC	156	●			●			
	3 State	539		●	●				

CODE CONVERTERS

DESCRIPTION	TYPE	STD TTL	S	TECHNOLOGY	
6 Line BCD to 6 Line Binary- Or 4 Line to 4 Line BCD 9's BCD 10's Converters		184	●		
6 Bit Binary to 6 Bit BCD Converters		185	A		
BCD to Binary Converters		484		A	
Binary to BCD Converters		485		A	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	TECHNOLOGY	
Full BCD		147	●		●		
Cascadable Octal		148	●		●		
Cascadable Octal with 3 State Outputs		348			●		
4 Bit Cascadable with Registers		278	●		●		

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	STD TTL	ALS	AS	LS	S	TECHNOLOGY	
4 Bit Shifter	3 State	350					●		
Parallel 16 Bit Multi Mode Barrel Shifter	3 State	897			●				

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DISPLAY DECODERS/DRIVERS, MEMORY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS /DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY			
			STD TTL	ALS	AS	LS
BCD To Decimal	30 V	'45	•			
	60 V	'141	•			
	15 V	'145	•			•
	7 V	'445				•
BCD To Seven Segment	30 V	'46	A			
	15 V	'47	A			•
	5.5 V	'48	•			•
	5.5 V	'49	•			•
	30 V	'246	•			
	15 V	'247	•			•
	7 V	'347				•
	7 V	'447				•
	5.5 V	'248	•			•
	5.5 V	'249	•			•

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

DESCRIPTION	TYPE	TECHNOLOGY		
		STD TTL	ALS	AS
BCD Counter/4-Bit Latch/BCD-To-Decimal Decoder/Driver	'142	•		
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Led Driver	'143	•		
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lamp Driver	'144	•		

VOLTAGE-CONTROLLED OSCILLATORS

No. VCOs	COMP'L ZOUT	ENABLE	RANGE INPUT	R _{EXT}	f _{max} MHz	TECHNOLOGY		
						TYPE	LS	S
Single	Yes	Yes	Yes	No	20	'624	•	
Single	Yes	Yes	Yes	Yes	20	'628	•	
Dual	No	Yes	Yes	No	60	'124		•
Dual	Yes	Yes	No	No	20	'626	•	
Dual	No	No	No	No	20	'627	•	
Dual	No	Yes	Yes	No	20	'629	•	

MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION	TYPE	TECHNOLOGY			
		ALS	AS	LS	S
System Controllers, Universal or For 8881	890		•		
Memory Refresh	Transparent, 4K, 16K	600		A	
Memory Refresh	Burst Modes, 64K	601		A	
Memory Refresh	Cycle Steal, 4K, 16K	602		A	
Memory Refresh	Burst Modes, 64K	603		A	
Memory Cycle Controller		608		•	
Memory Mappers	3 State	612		•	
Memory Mappers	OC	613		•	
Memory Mappers	3 State	610		•	
With Output Latches	OC	611		•	
Multi Mode Latches (8080A Applications)		412			•

CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quadruple Complementary Output Logic Elements	'265	•				
Dual Pulse Synchronizers/Drivers	'120	•				
Crystal Controlled Oscillators	'320				•	
Crystal Controlled Oscillators	'321				•	
Digital Phase-Lock Loop	'297				•	
Programmable Frequency	'292				•	
Dividers Digital Timers	'294				•	
Triple 4-Input AND NAND Drivers	'800			•		
Triple 4-Input OR NOR Drivers	'802			•		
Dual VCO	'124					•

RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'LS47, 'LS48, 'LS49, 'LS347

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----

RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----

RESULTANT DISPLAYS USING '143, '144

0	1	2	3	4	5	6	7	8	9
---	---	---	---	---	---	---	---	---	---

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COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

DESCRIPTION					TECHNOLOGY				
P	Q	P-Q	P-Q	OUTPUT	TYPE	STD TTL	ALS	AS	S
Yes	Yes	No	2 State	No	'85	•			• •

8-BIT COMPARATORS

DESCRIPTION								TECHNOLOGY		
INPUTS	P	Q	P-Q	P-Q	OUTPUT	OUTPUT ENABLE	TYPE	ALS	AS	LS
20 kΩ Pull Up	Yes	No	No	No	OC	Yes	518	●		
	No	Yes	No	No	2 State	Yes	520	●		
	No	Yes	No	No	OC	Yes	522	●		
	Yes	No	Yes	No	2 State	No	682			●
	Yes	No	Yes	No	OC	No	683			●
Standard	Yes	No	No	No	OC	Yes	519	●		
	No	Yes	No	No	2 State	Yes	521	●		
	Yes	No	Yes	No	2 State	No	684			●
	Yes	No	Yes	No	OC	No	685			●
	Yes	No	Yes	No	2 State	Yes	686			●
	Yes	No	Yes	No	OC	Yes	687			●
	No	Yes	No	Yes	2 State	Yes	688		●	
Latched P and Q	No	Yes	No	No	OC	Yes	689		●	
	No	No	Yes	Yes	2 State	Yes	885		●	
Latched P and Q	Yes	No	Yes	Yes	Latched	Yes	866		●	

ADDRESS COMPARATORS

DESCRIPTION		OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY	
16 Bit to 4 Bit		Yes		'677	•	
			Yes	'678	•	
12 Bit to 4 Bit		Yes		'679	•	
			Yes	'680	•	

PARITY GENERATORS/CHECKERS. ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	STD TTL	TECHNOLOGY				
Odd-Even Parity Generators/Checkers		8	'180	•					
		9	'280		•				• •
		9	'286			•			
Parallel Error Detection/Correction Circuits	3 State	8	'636						•
	OC	8	'637						•
	3 State	16	'616			•	•		
	OC	16	'617			•			
	3 State	16	'630						•
	OC	16	'631						•
	3 State	32	'632		A				
	OC	32	'633						
	3 State	32	'634			•			
	OC	32	'635						

FUSE-PROGRAMMABLE COMPARATORS

DESCRIPTION		TYPE	STD TTL	TECHNOLOGY				
16 Bit Identity Comparator		'526		•				
12 Bit Identity Comparator		'528						
8 Bit Identity Comparator and 4-Bit Comparator		'527		•				

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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
1 Bit Gated	'80	•				
2-Bit	'82	•				
4-Bit	'83	A				A
	'83	•				•
Dual 1-Bit Carry-Save	'183					•

ACCUMULATORS, ARITHMETIC LOGIC UNITS,
LOOK AHEAD CARRY GENERATORS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
4 Bit parallel Binary Accumulators	'281					•
	'681					•
	'181	•				•
4 Bit Arithmetic Logic Units Function Generators	'381				A	
	'881				A	
4-Bit Arithmetic Logic Unit with Ripple Carry	'382					•
Look-Ahead Carry Generators	16-Bit '182	•				•
	'282					•
	'882					•
Quad Serial Adder-Subtractor	'385					•
8 Bit Slice Elements	'888					•

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
2-Bit-by-4-Bit Parallel Binary Multipliers	'261					•
4-Bit-by-4-Bit Parallel Binary Multipliers	'284	•				
	'285	•				
25-MHz 6-Bit Binary Rate Multipliers	'97	•				
25-MHz Decade Rate Multipliers	'167	•				
8-Bit × 1-Bit 2's Complement Multipliers	'384					•
16-Bit Multimode Multiplier	'1616		•			

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY				
		STD TTL	ALS	AS	LS	S
Quad 2-Input Exclusive-OR Gates with Totem Pole Outputs	'86	•				A
	'386					A
Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs	'136	•				•
	'266					•
Quad 2-Input Exclusive- NOR Gates	'810		•	•		
Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs	'811		•	•		
Quad Exclusive-OR/NOR Gates	'135					•
4-Bit True-Complement Element	'87					

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				
			ALS	AS	LS	S	
8 Bit Slice	Yes	888					

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MEMORIES

USER PROGRAMMABLE READ-ONLY MEMORIES (PROM's) STANDARD PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S
16K Bit Arrays	TBP28S166	2048W × 8B	3 State	●
	TBP38S165	2048W × 8B	3 State	●
	TBP38S166	2048W × 8B	3 State	●
	TBP38SA165	2048W × 8B	OC	●
	TBP38SA166	2048W × 8B	OC	●
	TBP34S162	4096W × 4B	3 State	●
8K Bit Arrays	TBP34SA162	4096W × 4B	OC	●
	TBP24S81	2048W × 4B	3 State	●
	TBP24SA81	2048W × 4B	OC	●
	TBP28S85A	1024W × 8B	3 State	●
	TBP28S86A	1024W × 8B	3 State	●
	TBP28SA86A	1024W × 8B	OC	●
4K Bit Arrays	TBP38S85	1024W × 8B	3 State	●
	TBP38S86	1024W × 8B	3 State	●
	TBP38SA85	1024W × 8B	OC	●
	TBP38SA86	1024W × 8B	OC	●
	TBP24S41	1024W × 4B	3 State	●
	TBP24SA41	1024W × 4B	OC	●
2K Bit Arrays	TBP28S42	512W × 8B	3 State	●
	TBP28SA42	512W × 8B	OC	●
	TBP28S46	512W × 8B	3 State	●
	TBP28SA46	512W × 8B	OC	●
1K Bit Arrays	TBP38S22	256W × 8B	3 State	●
	TBP38SA22	256W × 8B	OC	●
	TBP24S10	256W × 4B	3 State	●
	TBP24SA10	256W × 4B	OC	●
256 Bit Arrays	TBP34S10	256W × 4B	3 State	●
	TBP34SA10	256W × 4B	OC	●
	TBP18S030	32W × 8B	3 State	●
	TBP18SA030	32W × 8B	OC	●
	TBP38S030	32W × 8B	3 State	●
	TBP38SA030	32W × 8B	OC	●

LOW-POWER PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S
16K Bit Arrays	TBP28L166	2048W × 8B	3 State	●
	TBP38L165	2048W × 8B	3 State	●
	TBP38L166	2048W × 8B	3 State	●
	TBP34L162	4096W × 4B	3 State	●
8K Bit Arrays	TBP28L85A	1024W × 8B	3 State	●
	TBP28L86A	1024W × 8B	3 State	●
	TBP38L85	1024W × 8B	3 State	●
	TBP38L86	1024W × 8B	3 State	●
4K Bit Arrays	TBP28L42	512W × 8B	3 State	●
	TBP28L46	512W × 8B	3 State	●
2K Bit Arrays	TBP28L22	256W × 8B	3 State	●
	TBP28LA22	256W × 8B	OC	●
1K Bit Arrays	TBP38L22	256W × 8B	3 State	●
	TBP34L10	256W × 4B	3 State	●
256 Bit Arrays	TBP38L030	32W × 8B	3 State	●

REGISTERED PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S
16K Bit Arrays	TBP34R162	4096W × 4B	3 State	●
	TBP34SR165	4096W × 4B	3 State	●

RANDOM-ACCESS READ-WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				
				STD TTL	ALS	AS	LS	S
256 Bit Arrays	256 × 1	3 State	'201					●
		OC	'301					●
		OC	'89	●				
64 Bit Arrays	16 × 4	3 State	'189				A B	
		3 State	'219				A	
		OC	'289				A B	
		OC	'319				A	
16 Bit Multiple-Port Register File	8 × 2	3 State	'172	●				
16 Bit Register File	4 × 4	OC	'170	●				●
		3 State	'670					●
Dual 64 Bit Register Files	16 × 4	3 State	'870					●
			'871					●

FIRST-IN FIRST-OUT MEMORIES (FIFO'S)

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				
			ALS	AS	LS	LS	S
16 Words × 5 Bits	3 State	225					●
64 Words × 5 Bits	3 State	233	●				
64 Words × 4 Bits	3 State	232	●				

A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.

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Functional Index

PROGRAMMABLE LOGIC ARRAYS

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	NO. NO.	OUTPUTS TYPE	TYPE NO.	ALS	NO. OF PINS
Impact PAL [*] Circuits	16	8	Active-Low	*PAL16L8-15	●	20
		4		*PAL16R4-15	●	
		6	Registered	*PAL16R6-15	●	
		8		*PAL16R8-15	●	
Half-Power Impact Circuits	16	8	Active-Low	*PAL16L8-25	●	20
		4		*PAL16R4-25	●	
		6	Registered	*PAL16R6-25	●	
		8		*PAL16R8-25	●	
High-Performance PAL [*] Circuits	16	8	Active-Low	*PAL16L8A	●	20
		4		*PAL16R4A	●	
		6	Registered	*PAL16R6A	●	
		8		*PAL16R8A	●	
Half-Power PAL [*] Circuits	16	8	Active-Low	*PAL16R8A-2	●	20
		4		*PAL16R4A-2	●	
		6	Registered	*PAL16R6A-2	●	
		8		*PAL16R8A-2	●	
High-Performance PAL [*] Circuits	20	8	Active-Low	*PAL20L8A	●	24
		4		*PAL20R4A	●	
		6	Registered	*PAL20R6A	●	
		8		*PAL20R8A	●	
Half-Power PAL [*] Circuits	20	8	Active-Low	*PAL20L8A-2	●	24
		4		*PAL20R4A-2	●	
		6	Registered	*PAL20R6A-2	●	
		8		*PAL20R8A-2	●	
Exclusive OR PAL [*] Circuits	20	10	Active-Low	*PAL20L10-20	●	24
		4		*PAL20X4-20	●	
		8	Registered	*PAL20X8-20	●	
		10		*PAL20X10-20	●	
Exclusive OR PAL [*] Circuits	20	8	Active-Low	*PALR19L8-35	●	24
		4		*PAL20X4-35	●	
		8	Registered	*PAL20X8-35	●	
		10		*PAL20X10-35	●	
Registered Input PAL [*] Circuits	19	8	Active-Low	*PALR19R4-25	●	24
		4		*PALR19R6-25	●	
		6	Registered	*PALR19R6-25	●	
		8		*PALR19R8-25	●	
Registered Input PAL [*] Circuits	19	8	Active-Low	*PALR19L8-40	●	24
		4		*PALR19R4-40	●	
		6	Registered	*PALR19R6-40	●	
		8		*PALR19R8-40	●	
Latched Input PAL [*] Circuits	19	8	Active-Low	*PALT19L8-25	●	24
		4		*PALT19R4-25	●	
		6	Registered	*PALT19R6-25	●	
		8		*PALT19R8-25	●	
Latched Input PAL [*] Circuits	19	8	Active-Low	*PALT19L8-40	●	24
		4		*PALT19R4-40	●	
		6	Registered	*PALT19R6-40	●	
		8		*PALT19R8-40	●	
Field Programmable 14 × 32 × 8 Logic Arrays	14	6	3 State	FPLA839	●	24
			OC	FPLA840	●	

* PAL is a registered trademark of Monolithic Memories Incorporated.

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General Information

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TTL DEVS

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TTL Devices

TTL DEVICES

Mechanical Data

TYPES SN5400, SN54L00, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NAND gates.

The SN5400, and SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (each gate)



positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

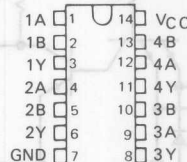
SN5400 ... J PACKAGE

SN54LS00, SN54S00 ... J OR W PACKAGE

SN7400 ... J OR N PACKAGE

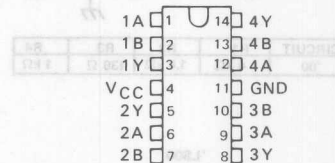
SN74LS00, SN74S00 ... D, J OR N PACKAGE

(TOP VIEW)



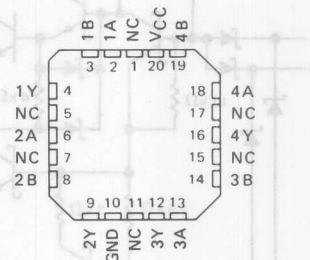
SN5400 ... W PACKAGE

(TOP VIEW)



SN54LS00, SN54S00 ... FK PACKAGE SN74LS00, SN74S00

(TOP VIEW)



NC - No internal connection

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TTL DEVICES

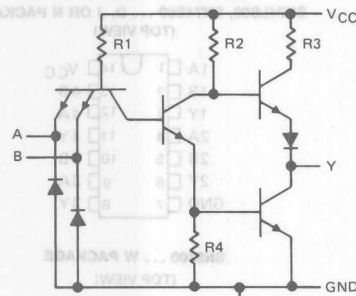
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

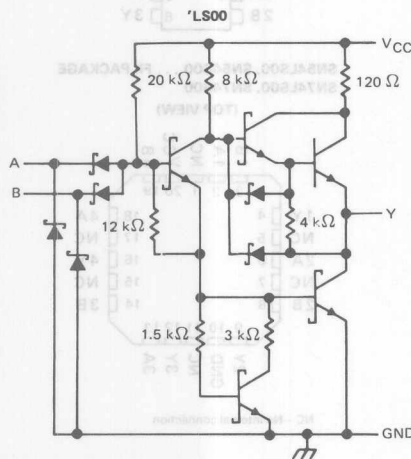
TEXAS
INSTRUMENTS

TYPES SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

schematics (each gate)



CIRCUIT	R1	R2	R3	R4
'00	4 kΩ	1.6 kΩ	130 Ω	1 kΩ



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) '00, 'LS00, 'S00	7 V
Input voltage: '00, 'S00	5.5 V
'LS00	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

- Package Options include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

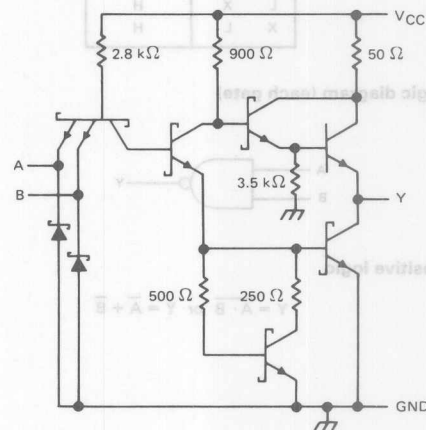
description

These devices contain four independent 2-input NAND gates.

The SN5400 and SN54LS00 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS	OUTPUT	
	A	B
Y	X	X
Y	X	X
Y	X	X
Y	X	X



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TTL DEVICES

TYPES SN5400, SN7400 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	SN5400			SN7400			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	V
V_{IH}	High-level input voltage	2					V
V_{IL}	Low-level input voltage		0.8			0.8	V
I_{OH}	High-level output current		-0.4			-0.4	mA
I_{OL}	Low-level output current		16			16	mA
T_A	Operating free-air temperature	-55	125			70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN5400			SN7400			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5			V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$			2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2	0.4		0.2	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1			mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40			μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6			mA
$I_{OS} §$	$V_{CC} = \text{MAX}$			-20			-18			mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$			4			4			mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$			12			12			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN TYP MAX			UNIT
				MIN	TYP	MAX	
t_{PLH}	A or B	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS00, SN74LS00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS00			SN74LS00			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.35	0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.8	1.6		0.8	1.6	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3 TTL DEVICES

TYPES SN54S00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

recommended operating conditions

	SN54S00			SN74S00			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S00			SN74S00			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		10	16		10	16	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		20	36		20	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 280 Ω, C _L = 15 pF		3	4.5	ns
t _{PHL}					3	5	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		4.5		ns
t _{PHL}					5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN5401, SN54LS01, SN7401, SN74LS01 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

REVISED APRIL 1985

- Package Options Include both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input-NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5401, and SN54LS01 are characterized for operation over the full military temperature ranges of -55°C to 125°C . The SN7401, and SN74LS01 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (each gate)

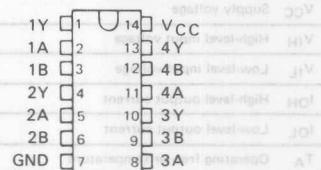


positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A + B}$$

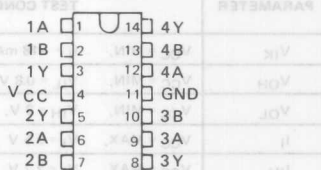
SN5401 ... J PACKAGE
SN54LS01 ... J OR W PACKAGE
SN7401 ... J OR N PACKAGE
SN74LS01 ... D, J OR N PACKAGE

(TOP VIEW)



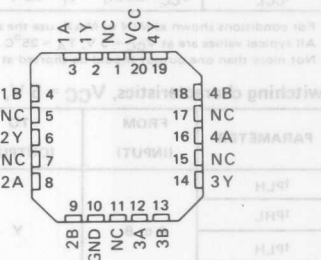
SN5401 ... W PACKAGE

(TOP VIEW)



SN54LS01 ... FK PACKAGE
SN74LS01

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

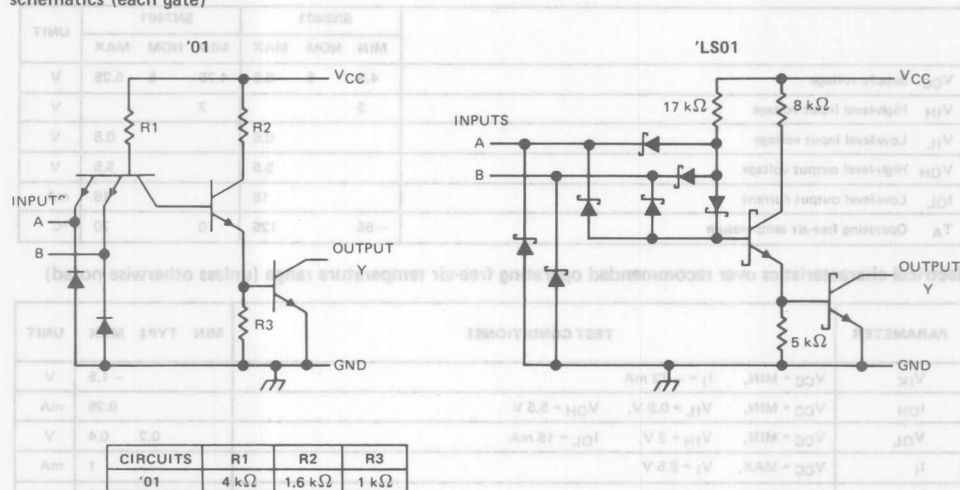
PRODUCTION DATA

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TEXAS
INSTRUMENTS

**TYPES SN5401, SN54LS01,
SN7401, SN74LS01**
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range(unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '01, 'H01, 'LS01	7 V
Input voltage: '01	5.5 V
'LS01	7 V
Off-state output voltage	7 V
Operating free-air temperature range:	
SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TTL DEVICES

TYPES SN5401, SN7401

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN5401			SN7401			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5	V
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V			0.25	mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		4	8	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 4 kΩ, C _L = 15 pF	35		55	ns
t _{PHL}			R _L = 400 Ω, C _L = 15 pF	8		15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

recommended operating conditions

	SN54LS01			SN74LS01			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS01			SN74LS01			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
I _{OH}	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		0.8	1.6		0.8	1.6	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 2 kΩ, C _L = 15 pF		17	32	ns
t _{PHL}					15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02 and SN54S02 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7402, SN74LS02 and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (each gate)



positive logic

$$Y = \overline{A + B} \text{ or } Y = \overline{A} \cdot \overline{B}$$

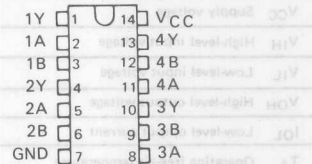
SN5402 ... J PACKAGE

SN54LS02, SN54S02 ... J OR W PACKAGE

SN7402 ... J OR N PACKAGE

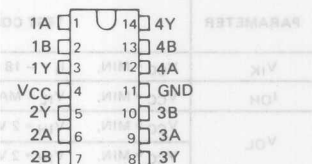
SN74LS02, SN74S02 ... D, J OR N PACKAGE

(TOP VIEW)



SN5402 ... W PACKAGE

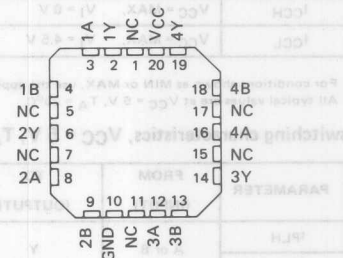
(TOP VIEW)



SN54LS02, SN54S02 ... FK PACKAGE

SN74LS02, SN74S02

(TOP VIEW)



NC - No internal connection

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TTL DEVICES

PRODUCTION DATA

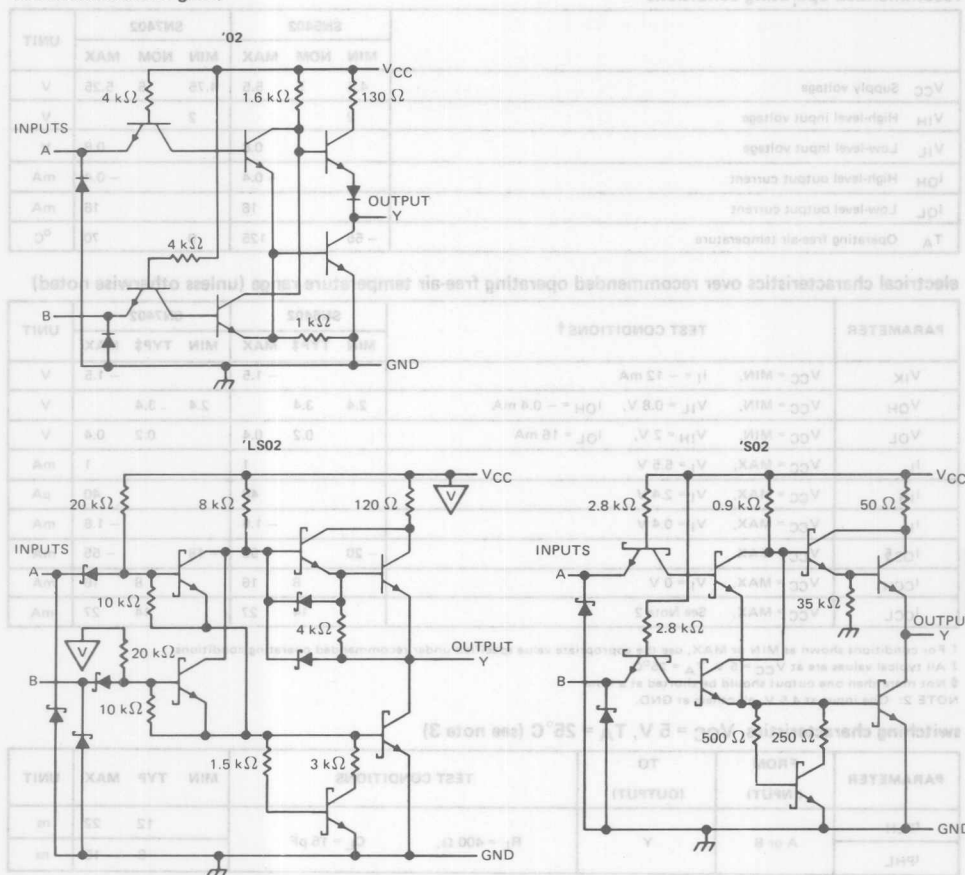
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TEXAS
INSTRUMENTS

**TYPES SN5402, SN54LS02, SN54S02,
SN7402, SN74LS02, SN74S02
QUADRUPE 2-INPUT POSITIVE-NOR GATES**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '02, 'LS02, 'S02	7 V
Input voltage: '02, 'S02	5.5 V
'LS02	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5402, SN7402 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

recommended operating conditions

	SN5402			SN7402			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5402			SN7402			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		8	16		8	16	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		14	27		14	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$	12	22		ns
t_{PHL}				8	15		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS02, SN74LS02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS02			SN74LS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS02			SN74LS02			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		-0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					-0.35	0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1				0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20				20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4				-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		1.6	3.2		1.6	3.2	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		2.8	5.4		2.8	5.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF}$		10	15	ns
t_{PHL}					10	15	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54S02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54S02			SN74S02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S02			SN74S02			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		17	29		17	29	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{See Note 2}$		26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	3.5	5.5	ns	
t_{PHL}							
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$	5	ns		
t_{PHL}							

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN5403, SN54LS03, SN54S03 SN7403, SN74LS03, SN74S03

QUADRUPL 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5403, SN54LS03 and SN54S03 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7403, SN74LS03 and SN74S03 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (each gate)



positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

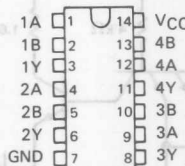
SN5403 ... J PACKAGE

SN54LS03, SN54S03 ... J OR W PACKAGE

SN7403 ... J OR N PACKAGE

SN74LS03, SN74S03 ... D, J OR N PACKAGE

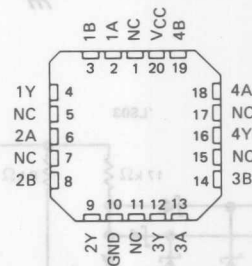
(TOP VIEW)



SN54LS03, SN54S03 ... FK PACKAGE

SN74LS03, SN74S03

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

PRODUCTION DATA

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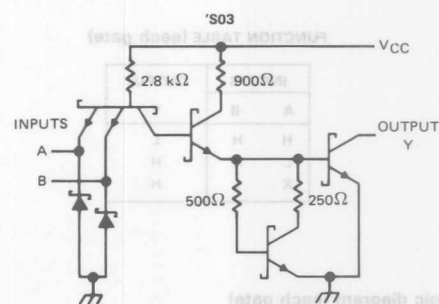
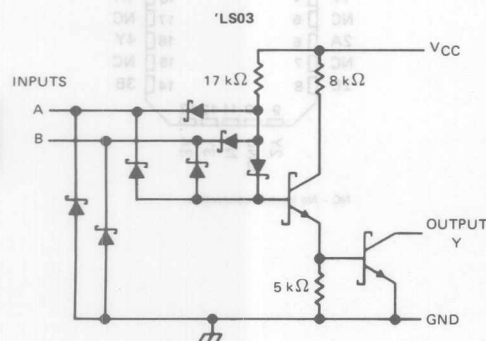
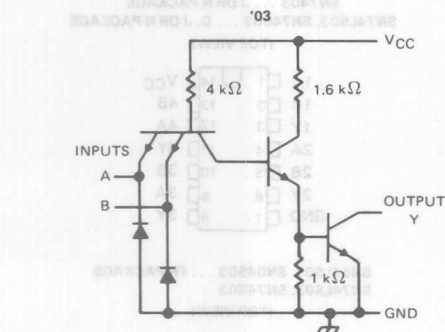
TEXAS
INSTRUMENTS

TYPES SN5403, SN54LS03, SN54S03

SN7403, SN74LS03, SN74S03

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '03, 'LS03, 'S03	7 V
Input voltage: '03, 'S03	5.5 V
'LS03	7 V
Off-state output voltage: 'LS03, 'S03	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5403, SN7403 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN5403			SN7403			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$		0.25		mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40		μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6		mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 4 \text{ k}\Omega,$	$C_L = 15 \text{ pF}$		35	45	ns
t_{PHL}			$R_L = 400 \Omega,$	$C_L = 15 \text{ pF}$		8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS03, SN74LS03 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54LS03			SN74LS03			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS03			SN74LS03			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
I _{OH}	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		0.8	1.6		0.8	1.6	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 2 kΩ, C _L = 15 pF		17	32	ns
t _{PHL}					15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S03, SN74S03 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54S03			SN74S03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.2		V
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V		0.25		mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA		0.5		V
I _I	V _{CC} = MAX, V _I = 5.5 V		1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		50		μA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V		-2		mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		6	13.2	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		20	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 280 Ω, C _L = 15 pF	2	5	7.5	ns
t _{PHL}				2	4.5	7	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		7.5		ns
t _{PHL}					7		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

QUADRALE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS TYPES SN74S03, SN74S03

recommended operating conditions

PARAMETER	SN74S03	SN74S03	UNIT
	MIN	MAX	
V _{CC} Supply voltage	4.5	5.5	V
V _{OH} High-level output voltage	2	3	V
V _{OL} Low-level output voltage	0.5	0.5	V
V _{IL} Low-level input voltage	0.5	0.5	V
V _{IH} High-level input voltage	2	3	V
I _{OL} Low-level output current	50	50	mA
T _A Operating free-air temperature	-55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IC}	V _{CC} = MIN, I _I = -15 mA	-1.5			V
I _{OH}	V _{CC} = MIN, V _{OL} = 0.5 V, V _{OH} = 2.5 V	0.25			mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA	0.5			V
I _I	V _{CC} = MAX, V _I = 2.5 V			1	mA
I _H	V _{CC} = MAX, V _I = 2.5 V			50	mA
I _L	V _{CC} = MAX, V _I = 0.5 V			-5	mA
I _{CC}	V _{CC} = MAX, V _I = 0 V		5	15.5	mA
I _{CC}	V _{CC} = MAX, V _I = 2.5 V		20	30	mA

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2 All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A to B	Y	R _L = 200 Ω, C _L = 15 pF	2	2	1.5	ns
				2	1.5	1	ns
			R _L = 200 Ω, C _L = 50 pF	1.5			ns
				1			ns

NOTE 5: See General Information Section for load circuit and voltage waveforms.

3 TTL DEVICES

TYPES SN5404, SN54LS04, SN54S04 SN7404, SN74LS04, SN74S04 HEX INVERTERS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

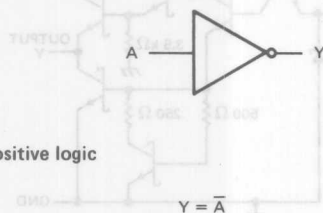
These devices contain six independent inverters.

The SN5404, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7404, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each inverter)

INPUTS	OUTPUT
A	Y
H	L
L	H

logic diagram (each inverter)



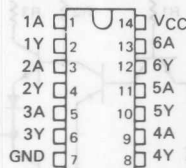
SN5404 ... J PACKAGE

SN54LS04, SN54S04 ... J OR PACKAGE

SN7404 ... J OR N PACKAGE

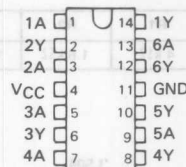
SN74LS04, SN74S04 ... D, J OR N PACKAGE

(TOP VIEW)



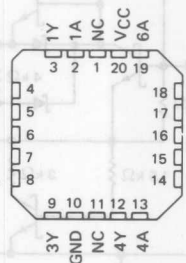
SN5404 ... W PACKAGE

(TOP VIEW)



SN54LS04, SN54S04 ... FK PACKAGE SN74LS04, SN74S04

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

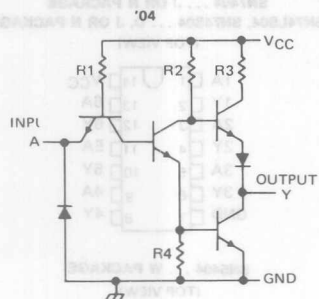
PRODUCTION DATA

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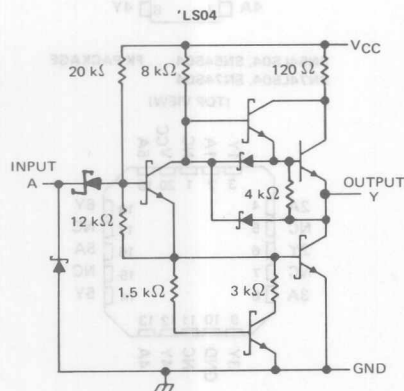
TEXAS
INSTRUMENTS

TYPES SN5404, SN54LS04, SN54S04 SN7404, SN74LS04, SN74S04 HEX INVERTERS

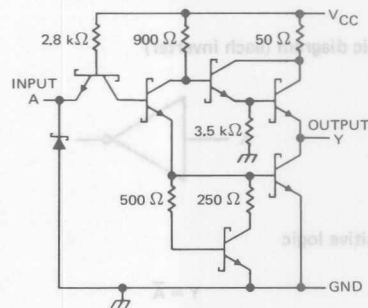
schematics (each gate)



CIRCUIT	R1	R2	R3	R4
'04	4 k Ω	1.6 k Ω	130 Ω	1 k Ω



Resistor values shown are nominal.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '04, 'LS04, 'S04	7 V
Input voltage: '04, 'S04	5.5 V
'LS04	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5404, SN7404 HEX INVERTERS

recommended operating conditions

PARAMETER	DESCRIPTION	SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5404			SN7404			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		6	12		6	12	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		18	33		18	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		12	22	ns
t_{PHL}					8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS04, SN74LS04

HEX INVERTERS

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS04			SN74LS04			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4			0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.25	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		1.2	2.4		1.2	2.4	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		9	15	ns
t_{PHL}					10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S04, SN74S04 HEX INVERTERS

recommended operating conditions

	SN54S04			SN74S04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-1			-1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S04			SN74S04			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		15	24		15	24	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		3	4.5	ns
t_{PHL}					3	5	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		4.5		ns
t_{PHL}					5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN5405, SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

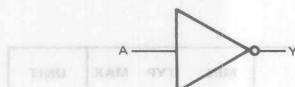
These devices contain six independent inverters. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open collector devices are often used to generate high V_{OH} levels.

The SN5405, SN54LS05 and SN54S05 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7405, SN74LS05 and SN74S05 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (each inverter)

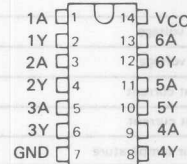


positive logic

$$Y = \overline{A}$$

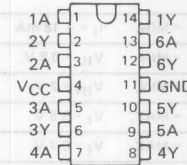
- SN5405 ... J PACKAGE
- SN54LS05, SN54S05 ... J OR W PACKAGE
- SN7405 ... J OR N PACKAGE
- SN74LS05, SN74S05 ... D, J OR N PACKAGE

(TOP VIEW)



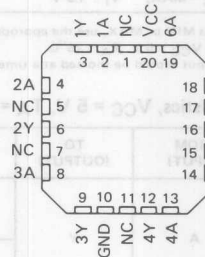
SN5405 ... W PACKAGE

(TOP VIEW)



- SN54LS05, SN54S05 ... FK PACKAGE
- SN74LS05, SN74S05

(TOP VIEW)



NC - No internal connection

3

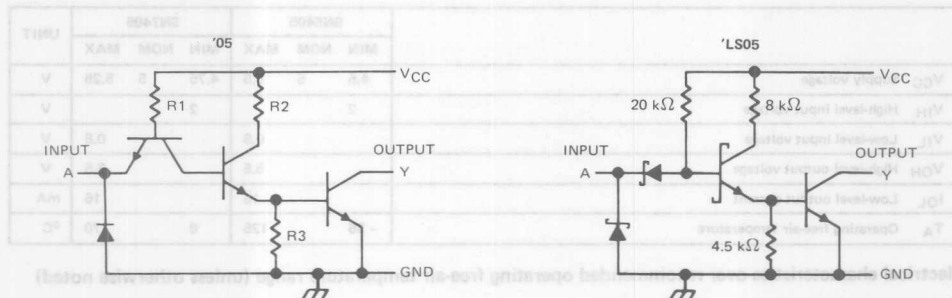
TTL DEVICES

PRODUCTION DATA

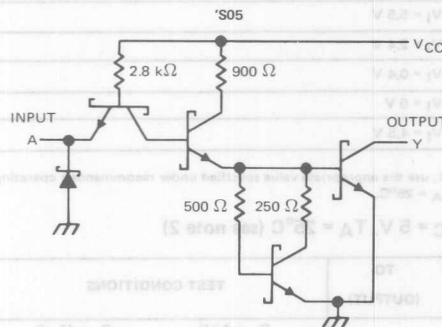
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**TYPES SN5405, SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05**
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

schematics (each inverter)



UNIT	MAX	CIRCUITS	R1	R2	R3	TEST CONDITIONS	PARAMETER
		'05	4K Ω	1.6K Ω	1K Ω		
V	2.1 -					$V_{CC} = \text{MIN.}$	V_{IH}
Am	25.0					$V_{CC} = \text{MIN.}$	I_{OH}
V	4.0					$V_{CC} = \text{MIN.}$	V_{OL}
Am	1					$V_{CC} = \text{MAX.}$	I_L
Am	08					$V_{CC} = \text{MAX.}$	I_H
Am	0.7 -					$V_{CC} = \text{MAX.}$	I_{CC}
Am	57					$V_{CC} = \text{MAX.}$	I_{OCH}
Am	22					$V_{CC} = \text{MAX.}$	I_{OCL}



UNIT	MAX	MIN	TEST CONDITIONS	PARAMETER
Am	22	40	$R_L = 1 \text{ k}\Omega$	P_{LH}
Am	22	40	$R_L = 1 \text{ k}\Omega$	P_{HL}

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '05, 'LS05, 'S05	7 V
Input voltage: '05, 'S05	5.5 V
'LS05	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5405, SN7405 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN5405			SN7405			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$		0.25		mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40		μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6		mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		6	12	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		18	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 4 \text{ k}\Omega, C_L = 15 \text{ pF}$	40	55		ns
t_{PHL}			$R_L = 400 \Omega, C_L = 15 \text{ pF}$	8	15		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS05, SN74LS05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	UNIT	SN54LS05			SN74LS05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{OH} High-level output voltage				5.5			5.5	V
I_{OL} Low-level output current				4			8	mA
T_A Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS05			SN74LS05			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25		0.4	0.25		0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35		0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	1.2		2.4	1.2		2.4	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	3.6		6.6	3.6		6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 2 \text{ k}\Omega$, $C_L = 15 \text{ pF}$		17	32	ns
t_{PHL}					15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S05, SN74S05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54S05			SN74S05			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S05			SN74S05			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.2			-1.2		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$		0.25			0.25		mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$		0.5			0.5		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50			50		µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2			-2		mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	9	19.8		9	19.8		mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	30	54		30	54		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 280 \Omega,$	$C_L = 15 \text{ pF}$	2	5	7.5	ns
t_{PHL}					2	4.5	7	ns
t_{PLH}			$R_L = 280 \Omega,$	$C_L = 50 \text{ pF}$		7.5		ns
t_{PHL}						7		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5406, SN5416, SN7406, SN7416 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

REVISED DECEMBER 1983

- Converts TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible with Most TTL Circuits

SN5406, SN5416 ... J OR W PACKAGE
SN7406, SN7416 ... J OR N PACKAGE

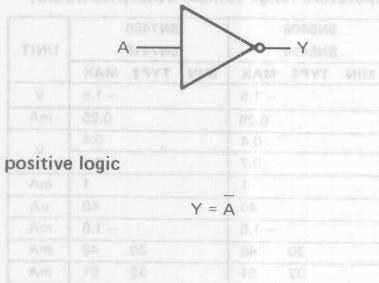
(TOP VIEW)



description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. The SN5406 and SN7406 have minimum breakdown voltages of 30 volts and the SN5416 and SN7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5406 and SN5416, and 40 milliamperes for the SN7406 and SN7416.

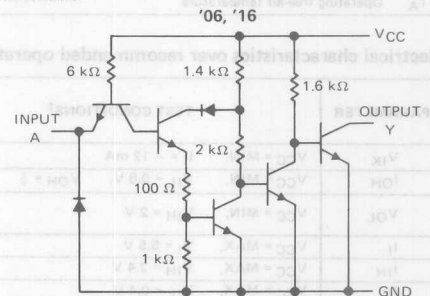
logic diagram



positive logic

$$Y = \bar{A}$$

schematic



Resistor values shown are nominal.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ \text{C}$	15	20	30	ns
t_{PLZ}	A	Y	$V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ \text{C}$	15	20	30	ns

TYPES SN5406, SN5416, SN7406, SN7416 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Output voltage (see Notes 1 and 2): SN5406, SN7406 Circuits	30 V
SN5416, SN7416 Circuits	15 V
Operating free-air temperature range: SN5406, SN5416 Circuits	–55°C to 125°C
SN7406, SN7416 Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5406 SN5416			SN7406 SN7416			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			30			30	V
				15			15	
I_{OL}	Low-level output current			30			40	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5406 SN5416			SN7406 SN7416			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5			–1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = \S$			0.25			0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$			0.4			0.4	V
	$I_{OL} = ¶$			0.7			0.7	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			–1.6			–1.6	mA
I_{CCH}	$V_{CC} = \text{MAX}$			30			30	48
I_{CCL}	$V_{CC} = \text{MAX}$			32			32	51

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ $V_{OH} = 30 \text{ V}$ for '06 and 15 V for '16.

¶ $I_{OL} = 30 \text{ mA}$ for SN54' and 40 mA for SN74'.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 110 \Omega, C_L = 15 \text{ pF}$		10	15	ns
t_{PHL}					15	23	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

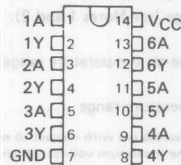
TYPES SN5407, SN5417, SN7407, SN7417 HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

REVISED DECEMBER 1983

- Converts TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible with Most TTL Circuits

SN5407, SN5417 ... J OR W PACKAGE
SN7407, SN7417 ... J OR N PACKAGE

(TOP VIEW)

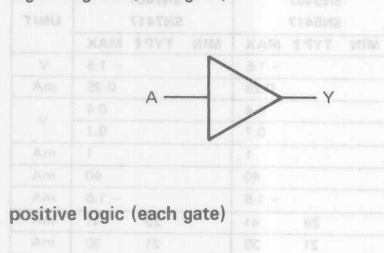


description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. The SN5407 and SN7407 have minimum breakdown voltages of 30 volts and the SN5417 and SN7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5407 and SN5417, and 40 milliamperes for the SN7407 and SN7417.

These circuits are completely compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The SN5407 and SN5417 are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN7407 and SN7417 are characterized for operation from 0°C to 70°C .

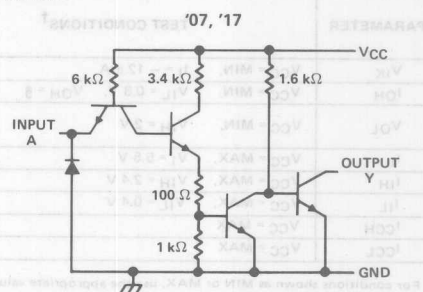
logic diagram (each gate)



positive logic (each gate)

Y = A

schematic



Resistor values shown are nominal.

3

TTL DEVICES

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROP DELAY	A	Y	$R_L = 110 \Omega$ $C_L = 50 \text{ pF}$		6	10	ns
SETUP TIME	A	Y			30	30	ns

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN5407, SN5417, SN7407, SN7417

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Output voltage (see Notes 1 and 2): SN5407, SN7407 Circuits	30 V
SN5417, SN7417 Circuits	15 V
Operating free-air temperature range: SN5407, SN5417 Circuits	–55°C to 125°C
SN7407, SN7417 Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5407 SN5417			SN7407 SN7417			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			30			30	V
				15			15	V
I_{OL}	Low-level output current			30			40	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN5407 SN5417			SN7407 SN7417			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				–1.5			–1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = §$				0.25			0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	$I_{OL} = 16 \text{ mA}$			0.4			0.4	V
		$I_{OL} = ¶$			0.7			0.7	V
I_{IH}	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$				40			40	mA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$				–1.6			–1.6	mA
I_{CCH}	$V_{CC} = \text{MAX}$		29	41		29	41		mA
I_{CCL}	$V_{CC} = \text{MAX}$		21	30		21	30		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ $V_{OH} = 30 \text{ V}$ for '07 and 15 V for '17.

¶ $I_{OL} = 30 \text{ mA}$ for SN54' and 40 mA for SN74'.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 110 \Omega, C_L = 15 \text{ pF}$	6	10	ns	
t_{PHL}				20	30	ns	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN5408, SN54LS08, SN54S08, SN7408, SN74LS08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram (each gate)



positive logic

$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

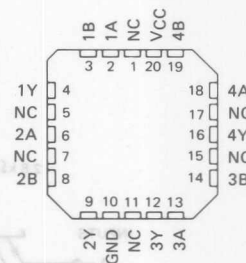
SN5408, SN54LS08, SN54S08 ... J OR W PACKAGE
SN7408 ... J OR N PACKAGE
SN74LS08, SN74S08 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS08, SN54S08 ... FK PACKAGE
SN74LS08, SN74S08

(TOP VIEW)



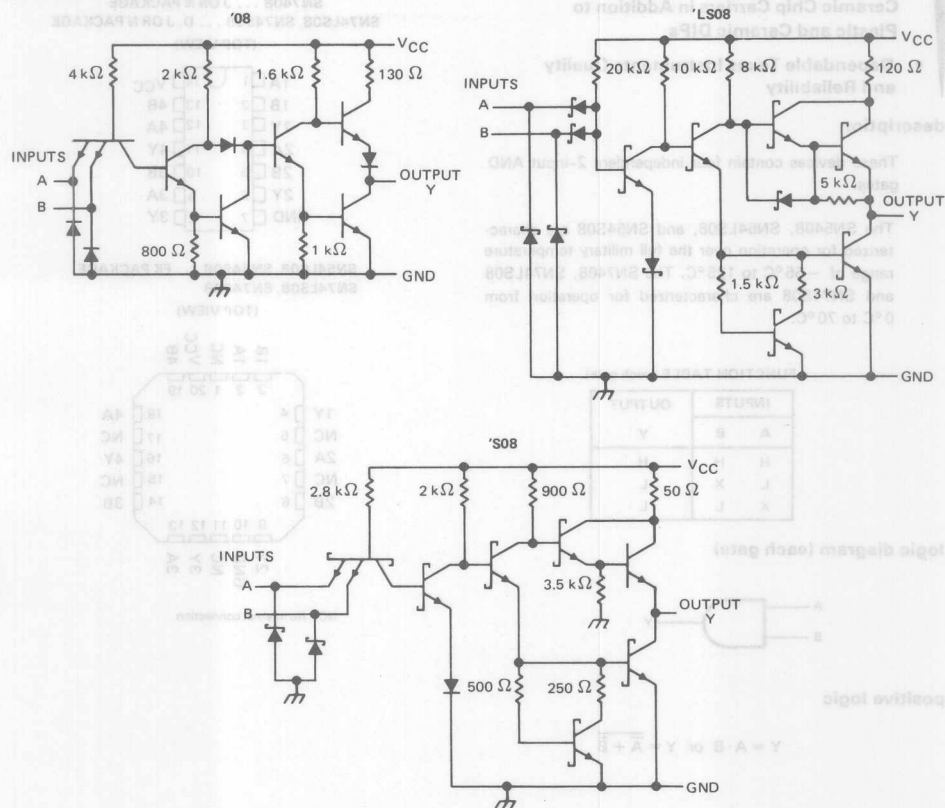
NC - No internal connection

3

TTL DEVICES

**TYPES SN5408, SN54LS08, SN54S08,
SN7408, SN74LS08, SN74S08
QUADRUPLE 2-INPUT POSITIVE-AND GATES**

schematics (each gate)



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '08, 'S08	5.5 V
'LS08	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

802J TYPES SN5408, SN7408 QUADRUPLE 2-INPUT POSITIVE-AND GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN5408			SN7408			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.8			-0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5408			SN7408			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.5			-1.5			V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -0.8 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40			40		µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6			-1.6		mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		11	21		11	21	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		20	33		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		17.5	27	ns
t_{PHL}					12	19	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS08, SN74LS08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

recommended operating conditions

	SN54LS08			SN74LS08			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS08			SN74LS08			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 8 \text{ mA}$					0.35	0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		2.4	4.8		2.4	4.8	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4.4	8.8		4.4	3.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	(INPUT)	(OUTPUT)					
t_{PLH}	A or B	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		8	15	ns
t_{PHL}					10	20	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

recommended operating conditions

	SN54S08			SN74S08			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S08			SN74S08			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V		18	32		18	32	mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V		32	57		32	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 280 Ω, C _L = 15 pF	4.5	7		ns
t _{PHL}				5	7.5		ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF	6			ns
t _{PHL}				7.5			ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

REVISED DECEMBER 1983

- description**

The SN5409, SN54LS09, and SN54S09 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7409, SN74LS09 and SN74S09 are characterized for operation from 0°C to 70°C .

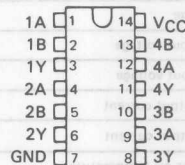
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L



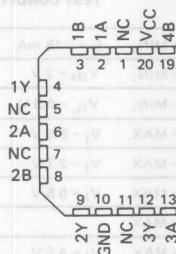
positive logic

$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

(TOP VIEW)



(TOP VIEW)



NC - No internal connection

logic diagram (each gate)



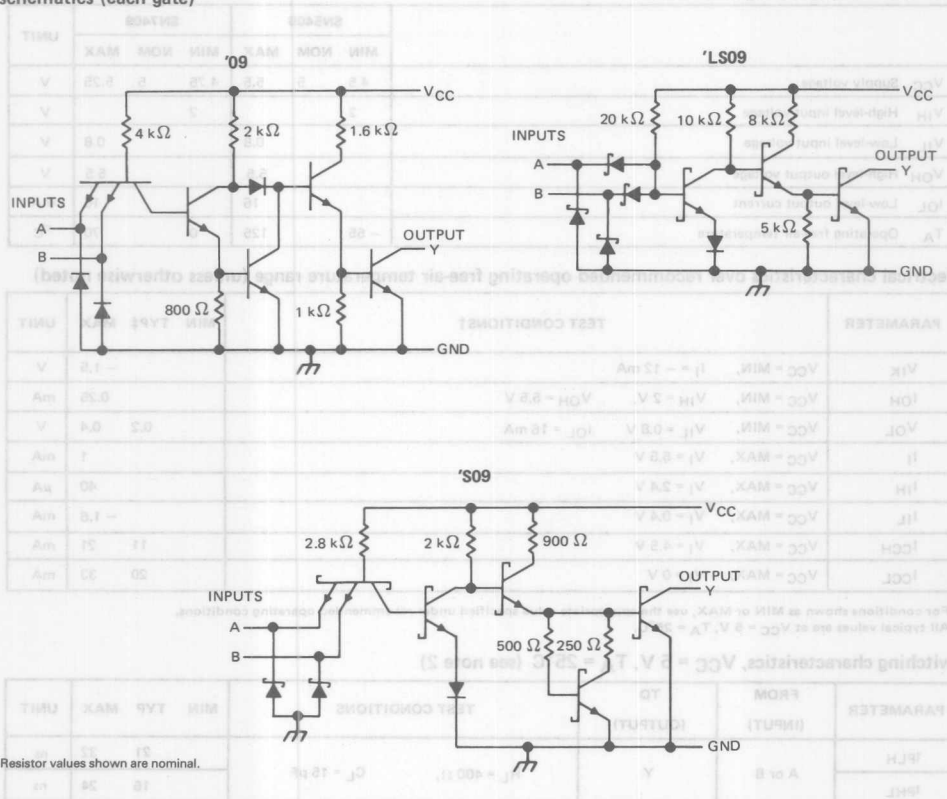
positive logic

$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TYPES SN5409, SN54LS09, SN54S09,
SN7409, SN74LS09, SN74S09
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '09, 'S09	5.5 V
'LS09	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5409, SN7409

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN5409			SN7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -12 mA		-1.5		V
I _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V		0.25		mA
V _{OL}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V		1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V		40		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-1.6		mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V		11	21	mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 400 Ω, C _L = 15 pF		21	32	ns
t _{PHL}					16	24	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS09, SN74LS09 QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54LS09			SN74LS09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS09			SN74LS09			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
I _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V		0.1			0.1		mA
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 8 mA				0.35	0.5		
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V	2.4	4.8		2.4	4.8		mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V	4.4	8.8		4.4	8.8		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 2 kΩ, C _L = 15 pF		20	35	ns
t _{PHL}					17	35	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54S09, SN74S09

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER		SN54S09			SN74S09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		18	32	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		32	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		6.5	10	ns
t_{PHL}					6.5	10	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		9		ns
t_{PHL}					9		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

**TYPES SN5410, SN54LS10, SN54S10
SN7410, SN74LS10, SN74S10
TRIPLE 3-INPUT POSITIVE-NAND GATES**

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

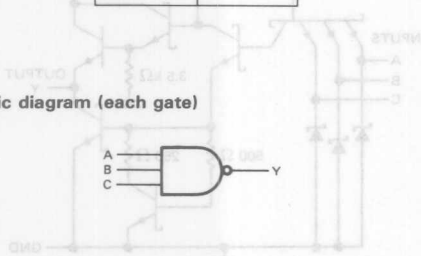
These devices contain three independent 3-input NAND gates.

The SN5410, SN54LS10 and SN54S10 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7410, SN74LS10 and SN74S10 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

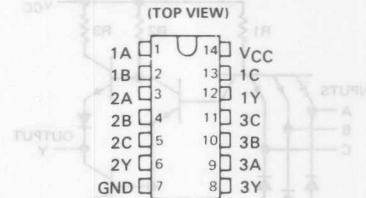
logic diagram (each gate)



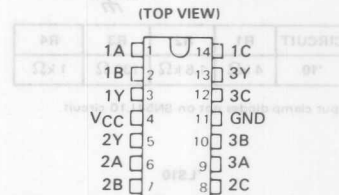
positive logic

$$Y = \overline{A \cdot B \cdot C} \text{ or } Y = \overline{A} + \overline{B} + \overline{C}$$

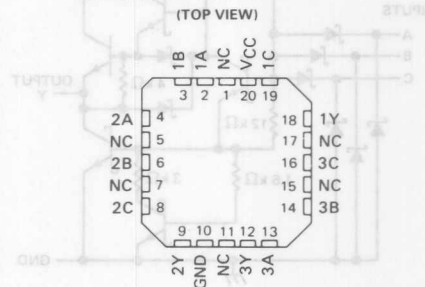
SN5410 ... J PACKAGE
SN54LS10, SN54S10 ... J OR W PACKAGE
SN7410 ... J OR N PACKAGE
SN74LS10, SN74S10 ... D, J OR N PACKAGE



SN5410 ... W PACKAGE



SN54LS10, SN54S10 ... FK PACKAGE
SN74LS10, SN74S10



NC - No internal connection

3

TTL DEVICES

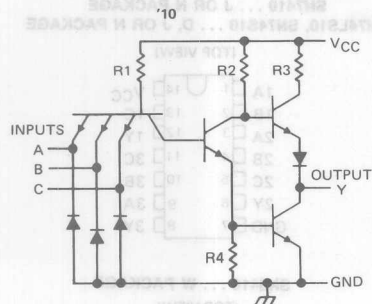
PRODUCTION DATA

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**TEXAS
INSTRUMENTS**

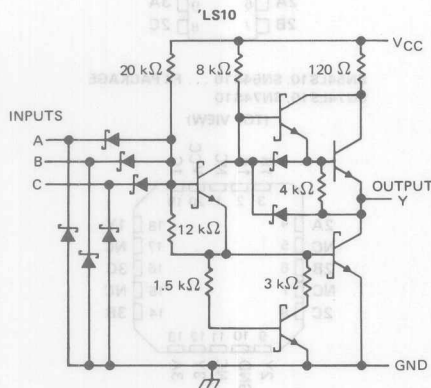
**TYPES SN5410, SN54LS10, SN54S10
SN7410, SN74LS10, SN74S10
TRIPLE 3-INPUT POSITIVE-NAND GATES**

schematics (each gate)



CIRCUIT	R1	R2	R3	R4
'10	4 k Ω	1.6 k Ω	130 Ω	1 k Ω

Input clamp diodes not on SN54L10 circuit.



Resistor values shown are nominal.

- Package Options include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

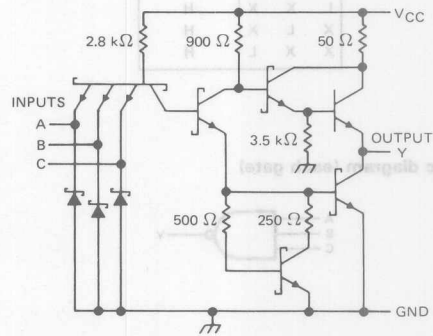
description

These devices contain three independent 3-input NAND gates.

The SN5410, SN54LS10 and SN54S10 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7410, SN74LS10 and SN74S10 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
H	H	L	H
H	L	H	H
H	L	L	H
L	H	H	H
L	H	L	H
L	L	H	H
L	L	L	H



positive logic

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '10, 'LS10, 'S10	7 V
Input voltage: '10, 'S10	5.5 V
'LS10	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

012J TYPES SN5410, SN7410 TRIPLE 3-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN5410			SN7410			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5410			SN7410			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$			3			3	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$			9			9	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 400 \Omega,$ $C_L = 15 \text{ pF}$		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPE SN54LS10, SN74LS10 TRIPLE 3-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS10			SN74LS10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS10			SN74LS10			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4			0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.25	0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.6	1.2		0.6	1.2	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		1.8	3.3		1.8	3.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 2 \text{ k}\Omega,$	$C_L = 15 \text{ pF}$		9	15	ns
t_{PHL}						10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S10, SN74S10

TRIPLE 3-INPUT POSITIVE-NAND GATES

recommended operating conditions

	SN54S10			SN74S10			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S10			SN74S10			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		7.5	12		7.5	12	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		15	27		15	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 280 Ω, C _L = 15 pF		3	4.5	ns
t _{PHL}					3	5	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		4.5		ns
t _{PHL}					5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

**TYPES SN54LS11, SN54S11
SN74LS11, SN74S11
TRIPLE 3-INPUT POSITIVE-AND GATES**

REVISED APRIL 1985

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

SN54LS11, SN54S11 ... J OR W PACKAGE

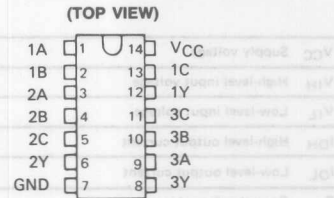
SN74LS11, SN74S11 ... D, J OR N PACKAGE

- Dependable Texas Instruments Quality and Reliability

description

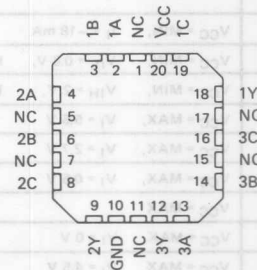
These devices contain three independent 3-input AND gates.

The SN54LS11 and SN54S11 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS11, and SN74S11 are characterized for operation from 0°C to 70°C.



SN54LS11, SN54S11 ... FK PACKAGE
SN74LS11, SN74S11

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

3

logic diagram (each gate)



positive logic

$$Y = A \cdot B \cdot C \text{ or } Y = \overline{\overline{A} + \overline{B} + \overline{C}}$$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B, C	Y	R _L = 200 Ω, C _L = 15 pF	0	2	4.5	ns
				0	2	5	ns
t _{PHL}	A, B, C	Y	R _L = 200 Ω, C _L = 15 pF	0	2	4.5	ns
				0	2	5	ns

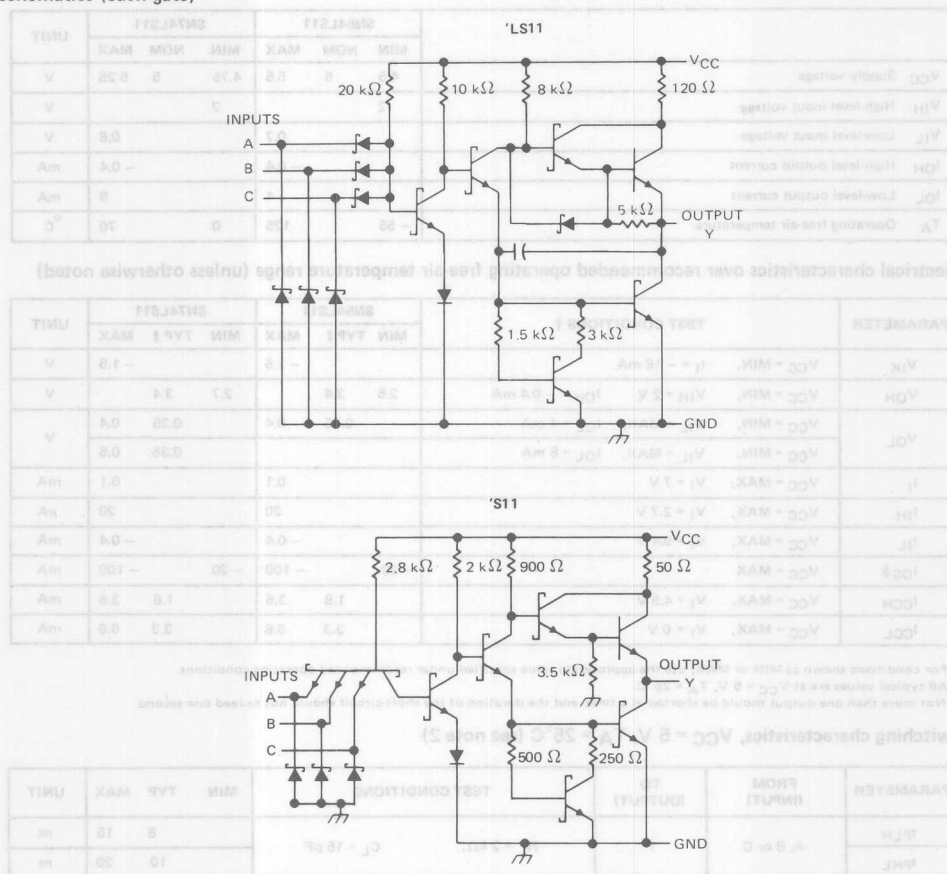
PRODUCTION DATA

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**TEXAS
INSTRUMENTS**

**TYPES SN54LS11, SN54S11
SN74LS11, SN74S11
TRIPLE 3-INPUT POSITIVE-AND GATES**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'S11	5.5 V
'LS11	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS11, SN74LS11

TRIPLE 3-INPUT POSITIVE-AND GATES

recommended operating conditions

	SN54LS11			SN74LS11			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			− 0.4			− 0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS11			SN74LS11			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = − 18 mA			− 1.5			− 1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = − 0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 8 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			− 0.4			− 0.4	mA
I _{OS} §	V _{CC} = MAX	− 20		− 100	− 20		− 100	mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V		1.8	3.6		1.8	3.6	mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V		3.3	6.6		3.3	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 2 kΩ,	C _L = 15 pF		8	15	ns
t _{PHL}						10	20	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S11, SN74S11 TRIPLE 3-INPUT POSITIVE-AND GATES

recommended operating conditions

	SN54S11			SN74S11			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S11			SN74S11			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V		13.5	24		13.5	24	mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V		24	42		24	42	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 280 Ω, C _L = 15 pF	4.5	7		ns
t _{PHL}				5	7.5		ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF	6			ns
t _{PHL}				7.5			ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN5412, SN54LS12 SN7412, SN74LS12 TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

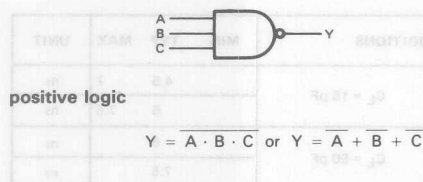
These devices contain three independent 3-input NAND gates with open-collector outputs. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5412 and SN54LS12 are characterized for operation over the full military range of -55°C to 125°C . The SN7412 and SN74LS12 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

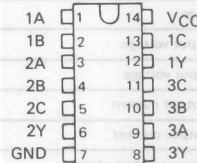
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic diagram (each gate)



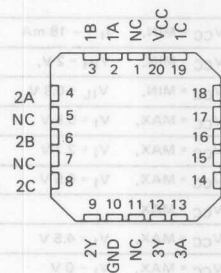
SN5412, SN54LS12 ... J OR W PACKAGE
SN7412 ... J OR N PACKAGE
SN74LS12 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS12 ... FK PACKAGE
SN74LS12

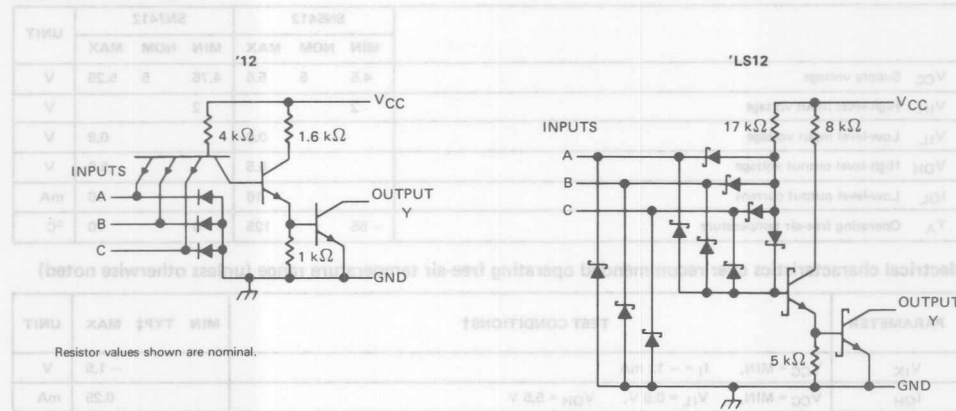
(TOP VIEW)



NC - No internal connection

**TYPES SN5412, SN54LS12
SN7412, SN74LS12
TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '12	5.5 V
'LS12	7 V
Off-state output voltage	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A-B-C	Y	$R_L = 400 \Omega$ $C_L = 15 \text{ pF}$		30	45	ns
t_{FHL}	A-B-C	Y	$R_L = 400 \Omega$ $C_L = 15 \text{ pF}$		8	10	ns

NOTE 2: See General Information Section for test circuit and voltage waveforms.

3

TTL DEVICES

TYPES SN5412, SN7412

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN5412			SN7412			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$		0.25		mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6		mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		3	6	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		9	16.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 4 \text{ k}\Omega, C_L = 15 \text{ pF}$	35	45		ns
t_{PHL}			$R_L = 400 \Omega, C_L = 15 \text{ pF}$	8	15		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS12, SN74LS12 TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS12			SN74LS12			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS12			SN74LS12			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	0.7	1.4		0.7	1.4		mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	1.8	3.3		1.8	3.3		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		17	32	ns
t_{PHL}					15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS TYPICAL CHARACTERISTICS

recommended operating conditions

UNIT	SUPPLY		INPUT		OUTPUT		
	MIN	MAX	MIN	MAX	MIN	MAX	
V	4.5	5.5	2	3	2	3	Supply voltage
V	2	3	2	3	2	3	High-level input voltage
V	0.3	0.3	0.3	0.3	0.3	0.3	Low-level input voltage
V	5.0	5.0	5.0	5.0	5.0	5.0	High-level output voltage
mA	4	4	4	4	4	4	Low-level output current
°C	-55	70	-55	70	-55	70	Operating free-air temperature

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

UNIT	SWAP72		SWAP72		TEST CONDITIONS	PARAMETER
	MIN	MAX	MIN	MAX		
V	1.8	—	1.8	—	$V_{CC} = \text{MIN}, I_I = -10 \text{ mA}$	V_{IK}
mA	0.0	—	0.1	—	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 2.5 \text{ V}$	I_{OH}
V	0.0	0.25	0.0	0.25	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	V_{OL}
	0.0	0.25	—	—	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 5 \text{ mA}$	
nA	0.1	—	0.1	—	$V_{CC} = \text{MAX}, V_I = 1 \text{ V}$	ρ
ns	20	—	20	—	$V_{CC} = \text{MAX}, V_I = 2 \text{ V}$	t_{PH}
ns	—	0.4	—	0.4	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$	t_{PL}
mA	0.3	—	0.3	—	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	I_{CCH}
mA	2.3	—	2.3	—	$V_{CC} = \text{MAX}, V_I = 2.5 \text{ V}$	I_{CCL}

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or C	Y	$R_L = 2\text{k}\Omega$	$C_L = 15\text{pF}$	15	17	30	ns
t_{PML}					18	30	ns	

NOTE 2: See General Information Section for load circuit and voltage waveform.

TYPES SN5413, SN54LS13, SN7413, SN74LS13

DUAL 4-INPUT

POSITIVE-NAND SCHMITT TRIGGERS

REVISED DECEMBER 1983

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

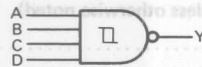
description

Each circuit functions as a 4-input NAND gate, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative (V_{T-}) signals.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

The SN5413 and SN54LS13 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7413 and SN74LS13 are characterized for operation from 0°C to 70°C .

logic diagram



positive logic

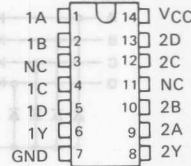
$$Y = \overline{ABCD}$$

SN5413, SN54LS13 ... J OR W PACKAGE

SN7413 ... J OR N PACKAGE

SN74LS13 ... D, J OR N PACKAGE

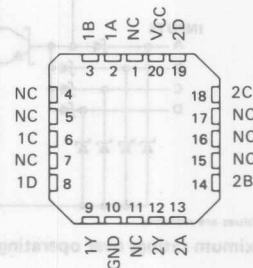
(TOP VIEW)



SN54LS13 ... FK PACKAGE

SN74LS13

(TOP VIEW)



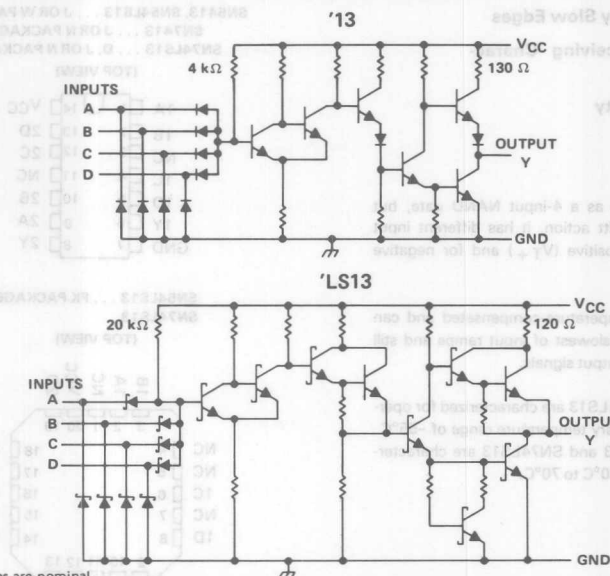
NC - No internal connection

3

TTL DEVICES

TYPES SN5413, SN54LS13, SN7413, SN74LS13 DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

schematics



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '13	5.5 V
'LS13	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3
TTL DEVICES

TYPES SN5413, SN7413 DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN5413			SN7413			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-0.8			-0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	-40		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V _{T+}	V _{CC} = 5 V			1.5	1.7	2	V
V _{T−}	V _{CC} = 5 V			0.6	0.9	1.1	V
Hysteresis (V _{T+} − V _{T−})	V _{CC} = 5 V			0.4	0.8		V
V _{IK}	V _{CC} = MIN,	I _I = − 12 mA				− 1.5	V
V _{OH}	V _{CC} = MIN,	V _I = 0.6 V,	I _{OH} = − 0.8 mA	2.4	3.4		V
V _{OL}	V _{CC} = MIN,	V _I = 2 V,	I _{OL} = 16 mA		0.2	0.4	V
I _{T+}	V _{CC} = 5 V,	V _I = V _{T+}			− 0.65		mA
I _{T−}	V _{CC} = 5 V,	V _I = V _{T−}			− 0.85		mA
I _I	V _{CC} = MAX,	V _I = 5.5 V				1	mA
I _{IH}	V _{CC} = MAX,	V _{IH} = 2.4 V				40	μA
I _{IL}	V _{CC} = MAX,	V _{IL} = 0.4 V			− 1	− 1.6	mA
I _{OS} §	V _{CC} = MAX,			− 18		− 55	mA
I _{CCH}	V _{CC} = MAX				14	23	mA
I _{CCL}	V _{CC} = MAX				20	32	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400\ \Omega$, $C_L = 15\text{ pF}$		18	27	ns
t_{PHL}					15	22	ns

3

TTL DEVICES

TYPES SN54LS13, SN74LS13 DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS13			SN74LS13			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS13			SN74LS13			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	$V_{CC} = 5\text{ V}$		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	$V_{CC} = 5\text{ V}$		0.5	0.8	1	0.5	0.8	1	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$		0.4	0.8		0.4	0.8		V
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$				-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_I = 0.5\text{ V}, I_{OH} = -0.4\text{ mA}$		2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_I = 1.9\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8\text{ mA}$					0.35	0.5	
I_{T+}	$V_{CC} = 5\text{ V}, V_I = V_{T+}$			-0.14			-0.14		mA
I_{T-}	$V_{CC} = 5\text{ V}, V_I = V_{T-}$			-0.18			-0.18		mA
I_I	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.7\text{ V}$				20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4\text{ V}$				-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$		-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}$			2.9	6		2.9	6	mA
I_{CCL}	$V_{CC} = \text{MAX}$			4.1	7		4.1	7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

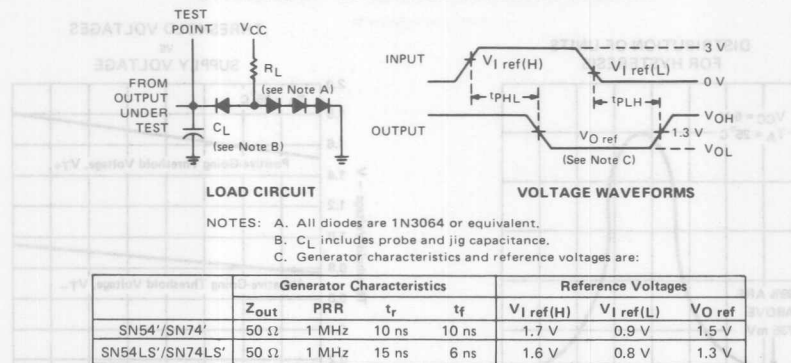
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	15	22		ns
t_{PHL}				18	27		ns

3

TTL DEVICES

TYPES SN5413, SN54LS13, SN7413, SN74LS13 DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS OF '13 CIRCUITS

POSITIVE-GOING THRESHOLD VOLTAGE

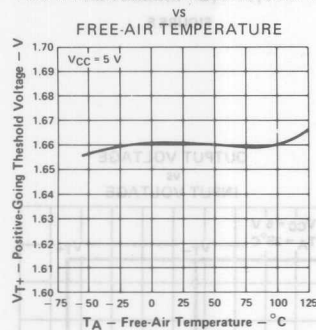


FIGURE 1

NEGATIVE-GOING THRESHOLD VOLTAGE

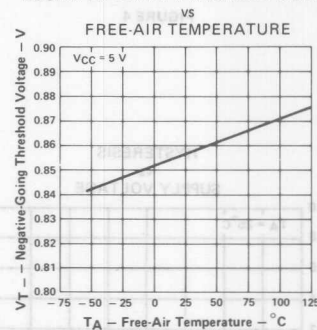


FIGURE 2

HYSTERESIS

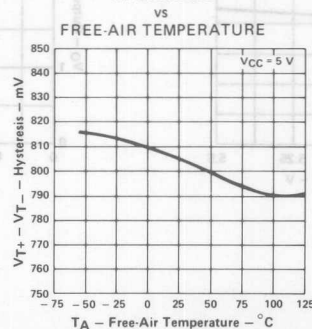


FIGURE 3

Data for temperatures below 0°C and 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN5413 only.

TYPES SN5413, SN7413
DUAL 4-INPUT
POSITIVE-NAND SCHMITT TRIGGERS

TYPICAL CHARACTERISTICS OF '13 CIRCUITS

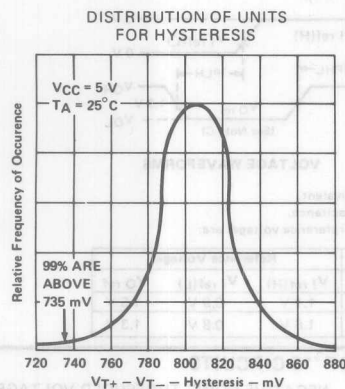


FIGURE 4

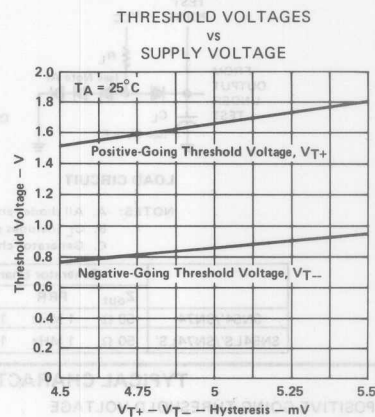


FIGURE 5

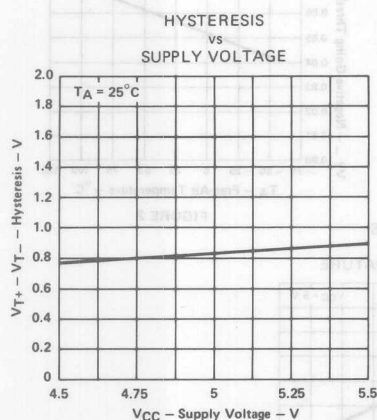


FIGURE 6

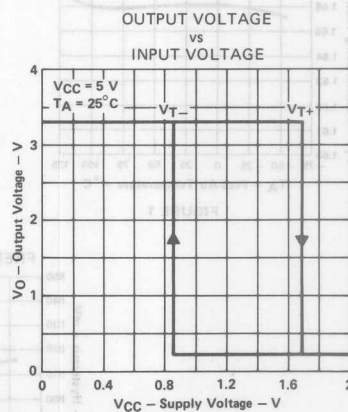
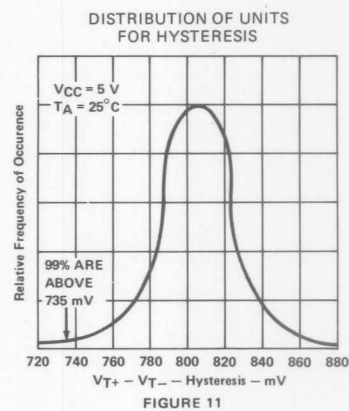
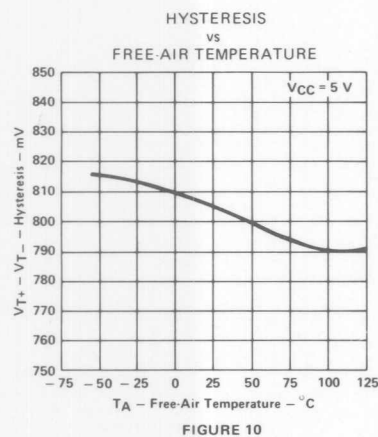
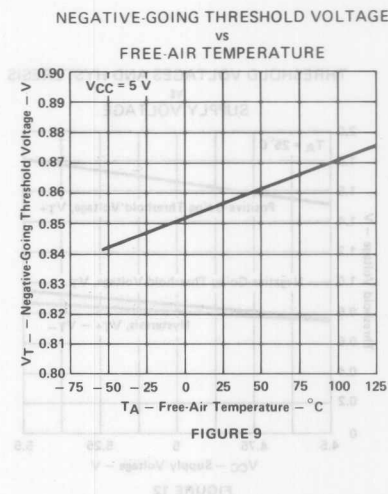
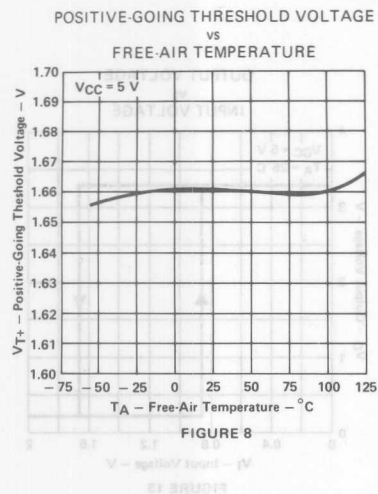


FIGURE 7

Data for temperatures below 0°C and 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN5413 only.

TYPES SN54LS13, SN74LS13
DUAL 4-INPUT
POSITIVE-NAND SCHMITT TRIGGERS

TYPICAL CHARACTERISTICS OF 'LS13 CIRCUITS



Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS13 only.

TYPES SN54LS13, SN74LS13
DUAL 4-INPUT
POSITIVE-NAND SCHMITT TRIGGERS

TYPICAL CHARACTERISTICS OF 'LS13 CIRCUITS

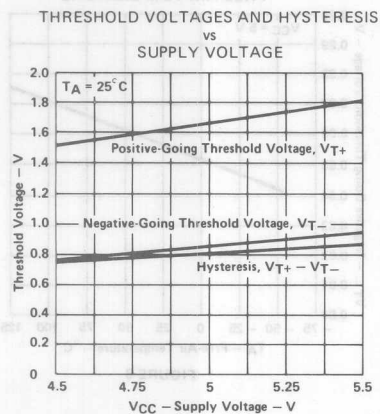


FIGURE 12

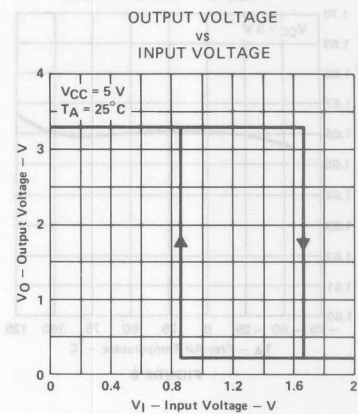


FIGURE 13

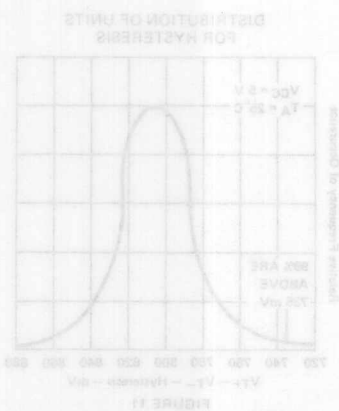


FIGURE 14

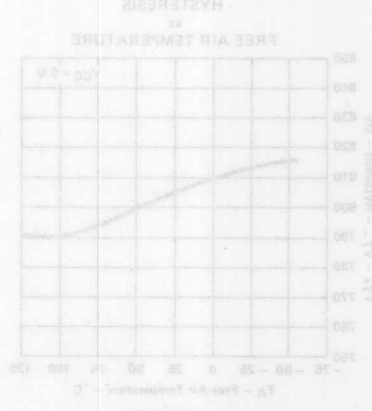
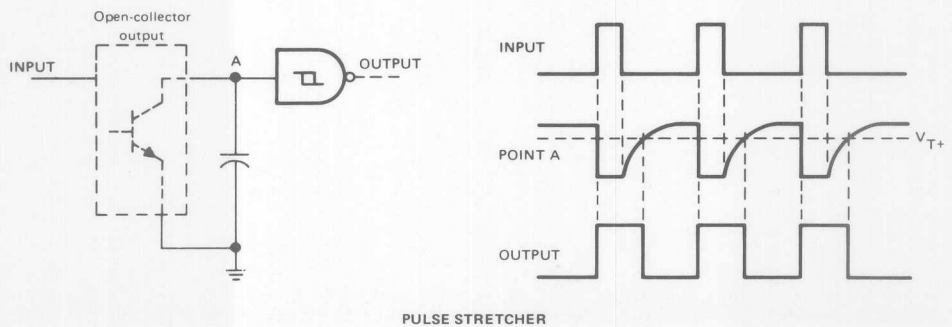
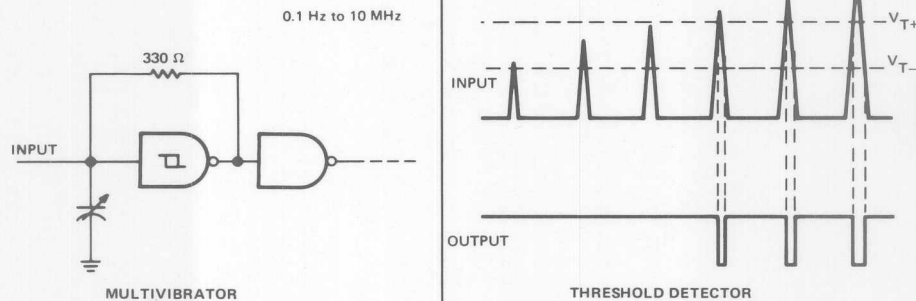
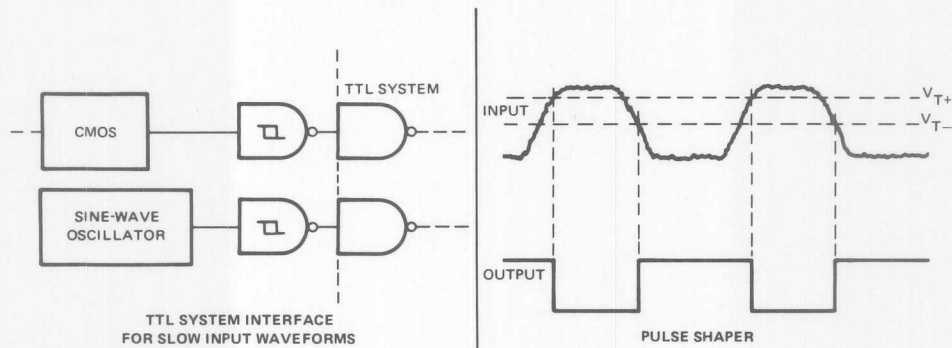


FIGURE 15

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS13 only.

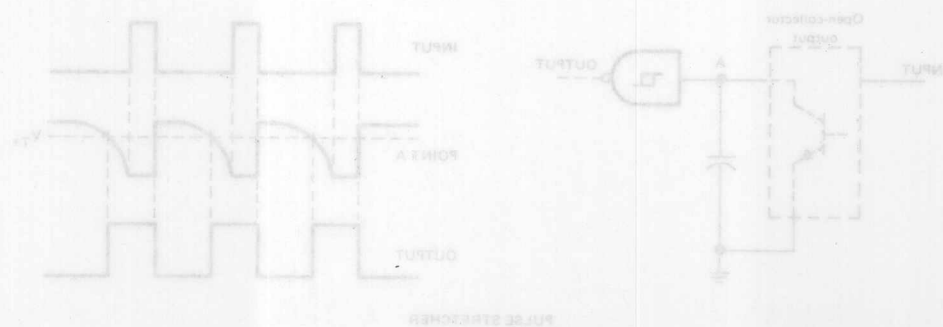
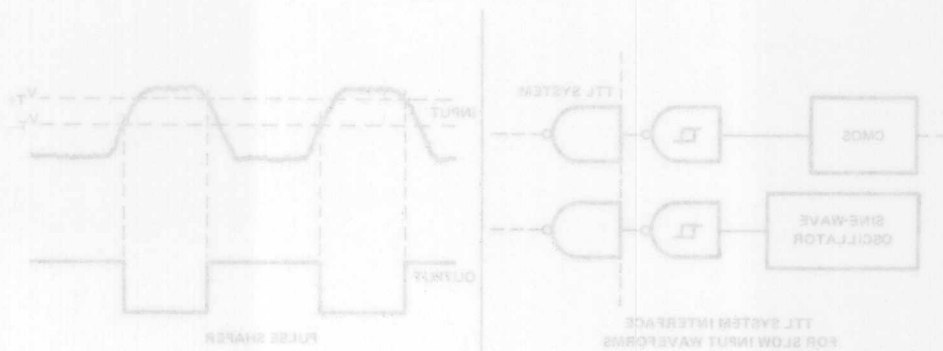
TYPES SN5413, SN54LS13, SN7413, SN74LS13
DUAL 4-INPUT
POSITIVE-NAND SCHMITT TRIGGERS

TYPICAL APPLICATION DATA



3
TTL DEVICES

TYPICAL APPLICATION DATA



TYPES SN5414, SN54LS14, SN7414, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

REVISED DECEMBER 1983

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

description

Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

The SN5414 and SN54LS14 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7414 and the SN74LS14 are characterized for operation from 0°C to 70°C .

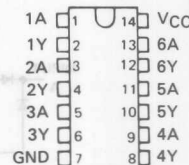
logic diagram



positive logic

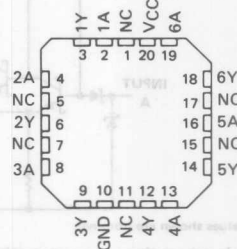
$$Y = \bar{A}$$

SN5414, SN54LS14 ... J OR W PACKAGE
SN7414 ... J OR N PACKAGE
SN74LS14 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS14 ... FK PACKAGE
SN74LS14

(TOP VIEW)



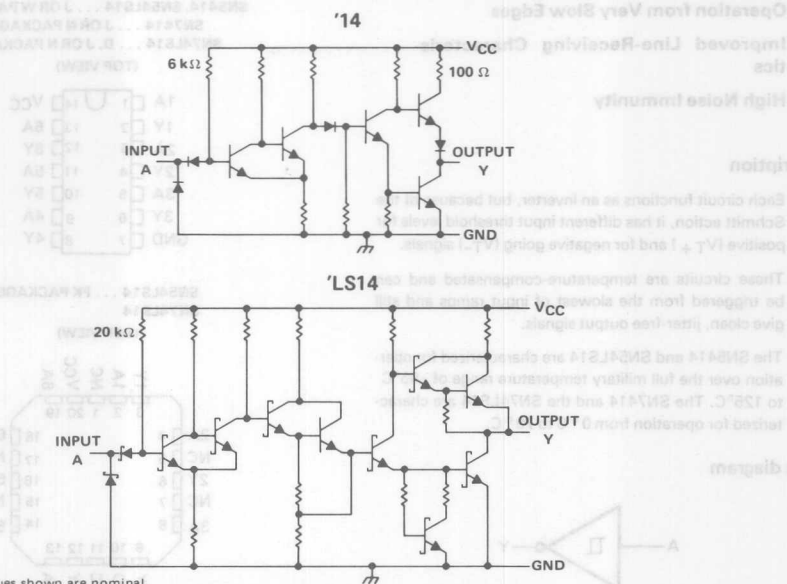
NC - No internal connection

3

TTL DEVICES

TYPES SN5414, SN54LS14, SN7414, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

schematics



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '14	5.5 V
'LS14	7 V
Operating free-air temperature: SN54'	–55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5414, SN7414 HEX SCHMITT-TRIGGER INVERTERS

recommended operating conditions

PARAMETER	DESCRIPTION	SN5414			SN7414			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-0.8			-0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{T+}	$V_{CC} = 5\text{ V}$			1.5	1.7	2	V
V_{T-}	$V_{CC} = 5\text{ V}$			0.6	0.9	1.1	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$			0.4	0.8		V
V_{IK}	$V_{CC} = \text{MIN},$ $I_I = -12\text{ mA}$					-1.5	V
V_{OH}	$V_{CC} = \text{MIN},$ $V_I = 0.6\text{ V},$ $I_{OH} = -0.8\text{ mA}$			2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN},$ $V_I = 2\text{ V},$ $I_{OL} = 16\text{ mA}$				0.2	0.4	V
I_{T+}	$V_{CC} = 5\text{ V},$ $V_I = V_{T+}$				-0.43		mA
I_{T-}	$V_{CC} = 5\text{ V},$ $V_I = V_{T-}$				-0.56		mA
I_I	$V_{CC} = \text{MAX},$ $V_I = 5.5\text{ V}$					1	mA
I_{IH}	$V_{CC} = \text{MAX},$ $V_{IH} = 2.4\text{ V}$					40	μA
I_{IL}	$V_{CC} = \text{MAX},$ $V_{IL} = 0.4\text{ V}$				-0.8	-1.2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$			-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}$				22	36	mA
I_{CCL}	$V_{CC} = \text{MAX}$				39	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 400\ \Omega$, $C_L = 15\text{ pF}$		15	22	ns
t_{PHL}	A	Y	$R_L = 400\ \Omega$, $C_L = 15\text{ pF}$		15	22	ns

3
TTL DEVICES

TYPES SN54LS14, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS14			SN74LS14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS14			SN74LS14			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	$V_{CC} = 5\text{ V}$	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	$V_{CC} = 5\text{ V}$	0.5	0.8	1	0.5	0.8	1	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$	0.4	0.8		0.4	0.8		V
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_I = 0.5\text{ V}, I_{OH} = -0.4\text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_I = 1.9\text{ V}, I_{OL} = 4\text{ mA}$ $I_{OL} = 8\text{ mA}$		0.25	0.4		0.25	0.4	V
I_{T+}	$V_{CC} = 5\text{ V}, V_I = V_{T+}$	-0.14			-0.14			mA
I_{T-}	$V_{CC} = 5\text{ V}, V_I = V_{T-}$	-0.18			-0.18			mA
I_I	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.7\text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4\text{ V}$			-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CCH}	$V_{CC} = \text{MAX}$		8.6	16		8.6	16	mA
I_{CCL}	$V_{CC} = \text{MAX}$		12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

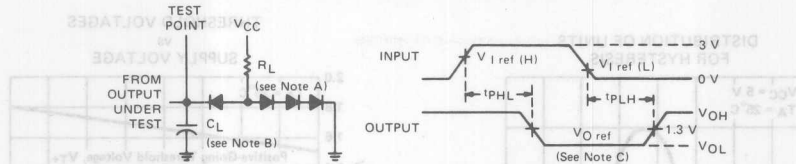
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$		15	22	ns
t_{PHL}	A	Y	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$		15	22	ns

TYPES SN5414, SN54LS14, SN7414, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

- NOTES: A. All diodes are 1N3064 or equivalent.
B. C_L includes probe and jig capacitance.
C. Generator characteristics and reference voltage are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I ref (H)}$	$V_{I ref (L)}$	$V_{O ref}$
SN54'/SN74'	50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50 Ω	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V

TYPICAL CHARACTERISTICS OF '14 CIRCUITS

POSITIVE-GOING THRESHOLD VOLTAGE

NEGATIVE-GOING THRESHOLD VOLTAGE

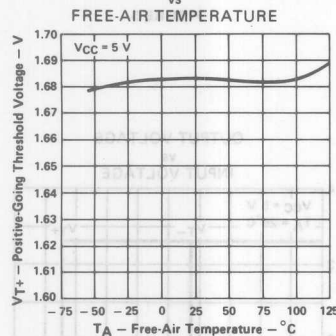


FIGURE 1

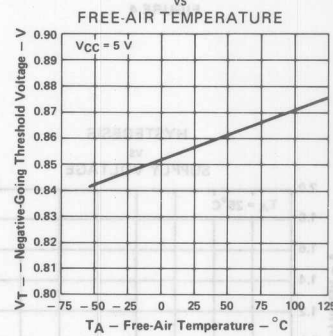


FIGURE 2

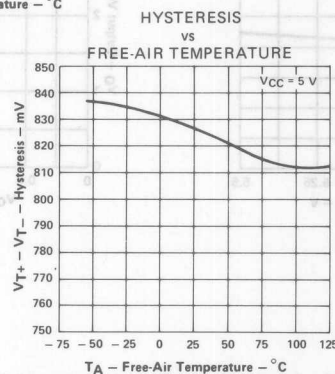


FIGURE 3

Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5414 only.

TYPES SN5414, SN7414 HEX SCHMITT-TRIGGER INVERTERS

TYPICAL CHARACTERISTICS OF '14 CIRCUITS

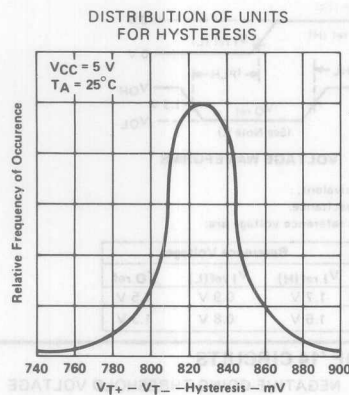


FIGURE 4

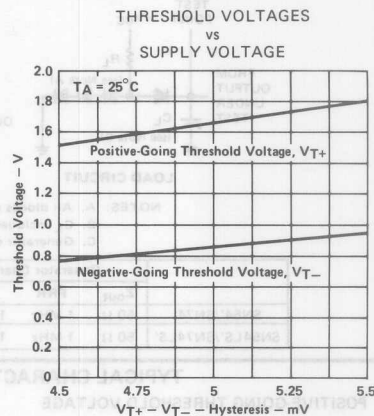


FIGURE 5

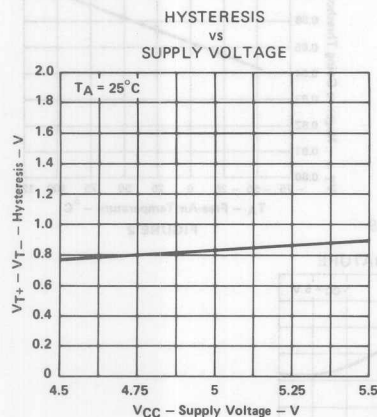


FIGURE 6

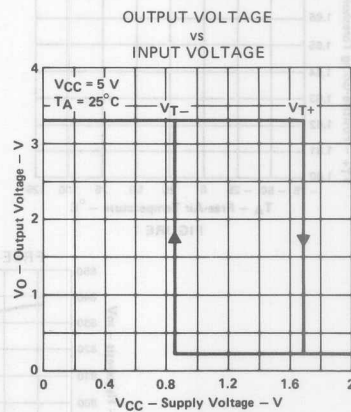


FIGURE 7

Data for temperatures below 0°C and 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN5414 only.

3

TTL DEVICES

TYPES SN54LS14, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS

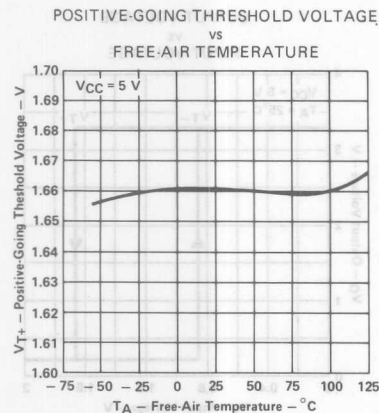


FIGURE 8

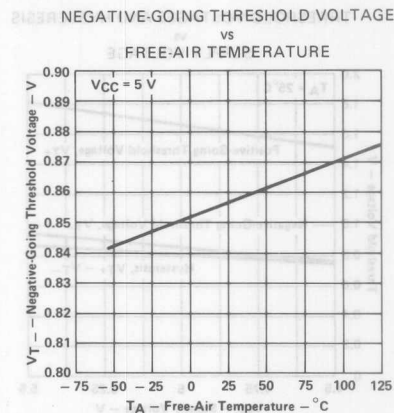


FIGURE 9

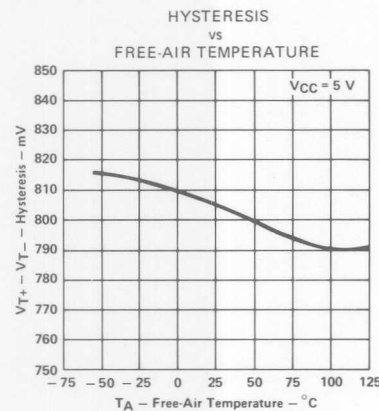


FIGURE 10

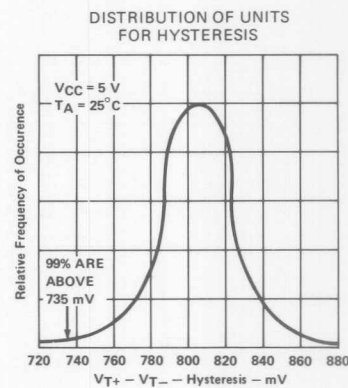


FIGURE 11

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS14 only.

3

TTL DEVICES

TYPES SN54LS14, SN74LS14 HEX SCHMITT-TRIGGER INVERTERS

TYPICAL CHARACTERISTICS OF 'LS14 CIRCUITS

THRESHOLD VOLTAGES AND HYSTERESIS

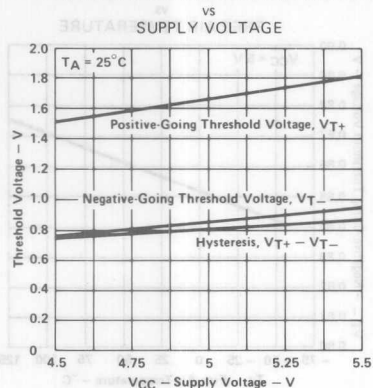


FIGURE 12

OUTPUT VOLTAGE

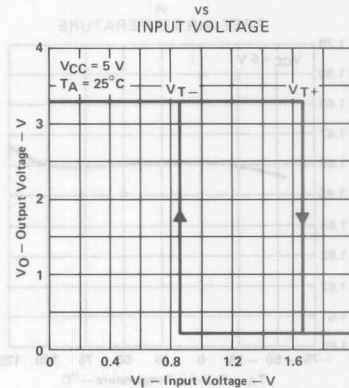


FIGURE 13

Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS14 only.

3

TTL DEVICES

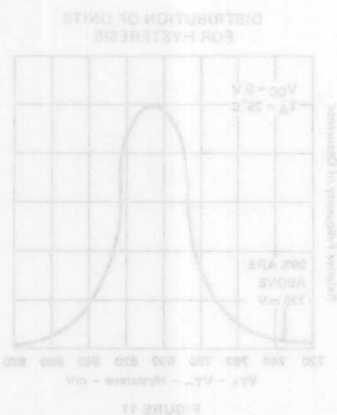
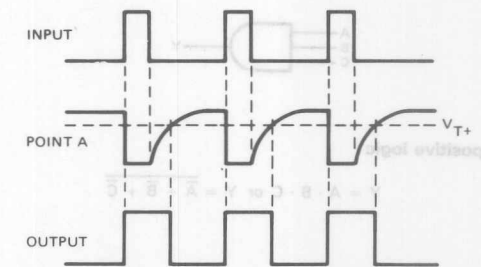
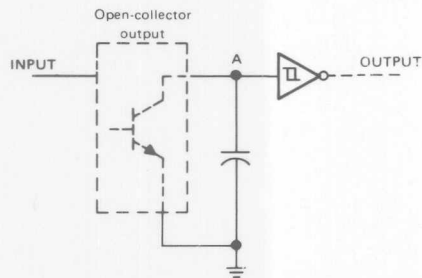
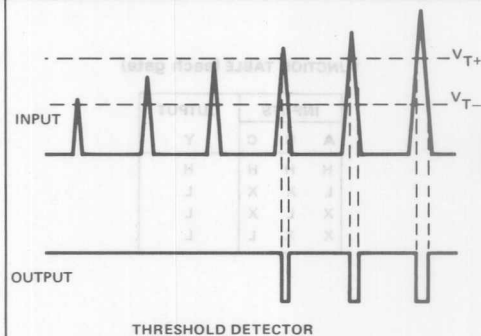
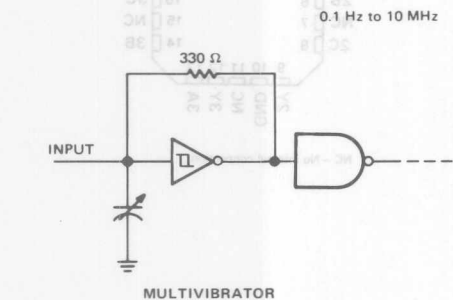
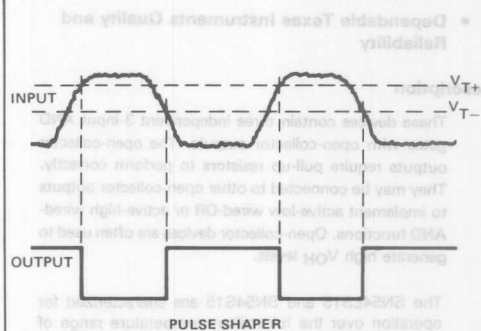
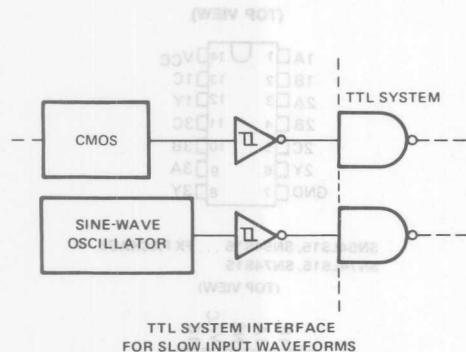


FIGURE 14



FIGURE 15

TYPICAL APPLICATION DATA



3

TTL DEVICES

TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

REVISED APRIL 1985

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain three independent 3-input AND gates with open-collector outputs. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate high V_{OH} levels.

The SN54LS15 and SN54S15 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS15, and SN74S15 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic diagram (each gate)



positive logic

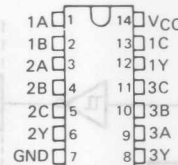
$$Y = A \cdot B \cdot C \text{ or } Y = \overline{\overline{A} + \overline{B} + \overline{C}}$$

TYPES SN54LS15, SN54S15 SN74LS15, SN74S15

SN54LS15, SN54S15 ... J OR W PACKAGE

SN74LS15, SN74S15 ... D, J OR N PACKAGE

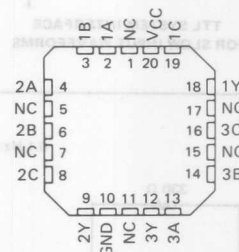
(TOP VIEW)



SN54LS15, SN54S15 ... FK PACKAGE

SN74LS15, SN74S15

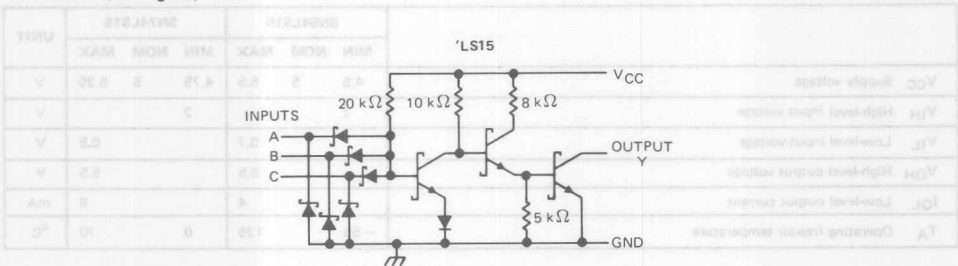
(TOP VIEW)



NC - No internal connection

TYPES SN54LS15, SN54S15
 SN74LS15, SN74S15
 TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'S15	UNIT
V_{CC} = MIN.		2.8 kΩ	V
V_{OH} = MIN.		2 kΩ	V
V_{OL} = MIN.		900 Ω	V
I_H		500 Ω	mA
I_L		250 Ω	mA
I_{OCH}			mA
I_{OCL}			mA

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1):	7 V
Input voltage: 'S15	5.5 V
'LS15	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS15, SN74LS15 TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS15			SN74LS15			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS15			SN74LS15			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
I _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA				0.35	0.5		
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V	1.8	3.6		1.8	3.6		mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V	3.3	6.6		3.3	6.6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A, B, or C	Y	R _L = 2 kΩ,	C _L = 15 pF		20	35	ns
t _{PHL}						17	35	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S15, SN74S15

TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54S15			SN74S15			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.2		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 5.5 \text{ V}$		0.25		mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.5		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50		μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		2		mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	10.5	19.5		mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	24	42		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	5.5	8.5		ns
t_{PHL}				6	9		ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$	8.5			ns
t_{PHL}				8			ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

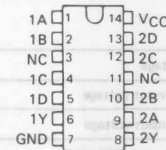
TTL DEVICES

TYPES SN74LS18, SN74LS19, SN74LS24 SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

JANUARY 1981—REVISED DECEMBER 1983

- Functionally and Mechanically Identical To 'LS13, 'LS14, and 'LS132, Respectively
- Improved Line-Receiving Characteristics
- P-N-P Inputs Reduce System Loading
- Excellent Noise Immunity With Typical Hysteresis of 0.7 V

SN74LS18 . . . D, J OR N PACKAGE
(TOP VIEW)

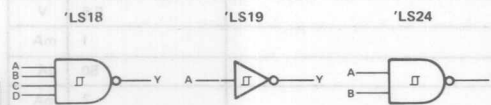


description

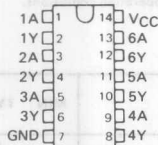
Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative (V_{T-}) signals. The hysteresis or backlash, which is the difference between the two threshold levels ($V_{T+} - V_{T-}$), is typically 900 millivolts.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

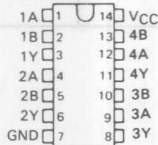
logic diagram (each gate or inverter)



SN74LS19 . . . D, J OR N PACKAGE
(TOP VIEW)



SN74LS24 . . . D, J OR N PACKAGE
(TOP VIEW)



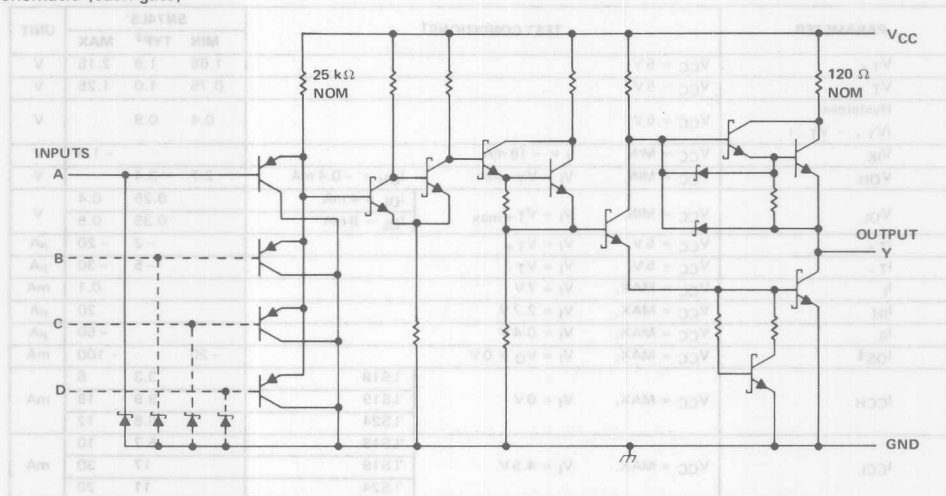
3 TTL DEVICES

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN74LS18, SN74LS19, SN74LS24 SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN74LS'			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

3

TTL DEVICES

TYPES SN74LS18, SN74LS19, SN74LS24 SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN74LS*			UNIT
		MIN	TYP†	MAX	
V_{T+}	$V_{CC} = 5\text{ V}$	1.65	1.9	2.15	V
V_{T-}	$V_{CC} = 5\text{ V}$	0.75	1.0	1.25	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$	0.4	0.9		V
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_I = V_{T-} - \text{min}, I_{OH} = -0.4\text{ mA}$	2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_I = V_{T+} + \text{max}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V
		$I_{OL} = 8\text{ mA}$	0.35	0.5	
I_{T+}	$V_{CC} = 5\text{ V}, V_I = V_{T+}$	-2	-20		μA
I_{T-}	$V_{CC} = 5\text{ V}, V_I = V_{T-}$	-5	-30		μA
I_I	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{ V}$			-50	μA
$I_{OS}§$	$V_{CC} = \text{MAX}, V_I = V_O = 0\text{ V}$	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0\text{ V}$	'LS18	3.3	6	mA
		'LS19	9.9	18	
		'LS24	6.6	12	
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5\text{ V}$	'LS18	5.7	10	mA
		'LS19	17	30	
		'LS24	11	20	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

†All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

3

TTL DEVICES

switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$, see figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS18			'LS19			'LS24			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Any	Y	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$	13	20		13	20		13	20		ns
t_{PHL}	Any	Y		37	55		18	30		25	40		ns

t_{PLH} - Propagation delay time, low to high-level output

t_{PHL} - Propagation delay time, high to low-level output

TYPES SN74LS18, SN74LS19, SN74LS24
SCHMITT-TRIGGER POSITIVE-NAND GATES
AND INVERTERS WITH TOTEM-POLE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

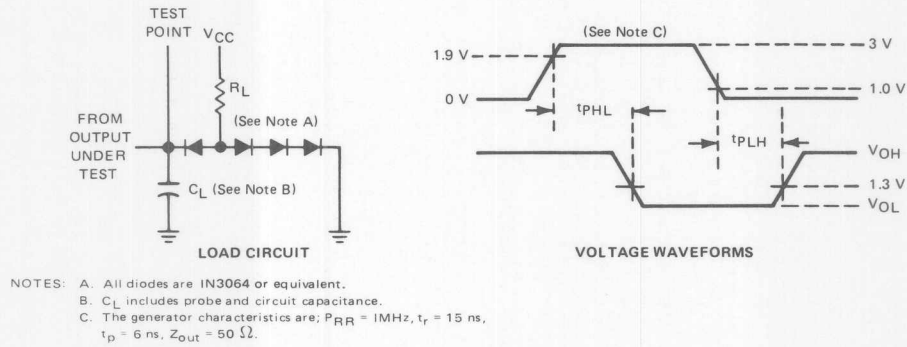
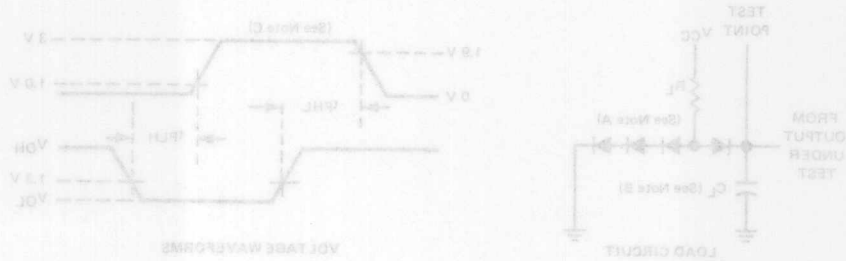


FIGURE 1

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All signals are IN300 or equivalent.
B. C_1 includes probe and device capacitance.
C. The generator resistance is $R_{out} = 50 \Omega$.
D. $t_{p} = 5 \text{ ns}$, $f_{max} = 50 \text{ MHz}$.

FIGURE 7

TYPES SN5420, SN54LS20, SN54S20 SN7420, SN74S20 DUAL 4-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 4-input NAND gates.

The SN5420, SN54LS20 and SN54S20 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7420, SN74LS20 and SN74S20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (each gate)



positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D} \text{ or } Y = \overline{A + B + C + D}$$

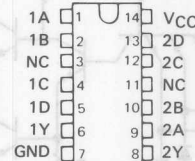
SN5420 ... J PACKAGE

SN54LS20, SN54S20 ... J OR W PACKAGE

SN7420 ... J OR N PACKAGE

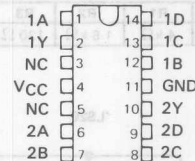
SN74LS20, SN74S20 ... D, J OR N PACKAGE

(TOP VIEW)



SN5420 ... W PACKAGE

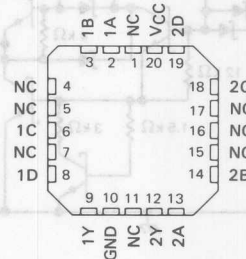
(TOP VIEW)



SN54LS20, SN54S20 ... FK PACKAGE

SN74LS20, SN74S20

(TOP VIEW)



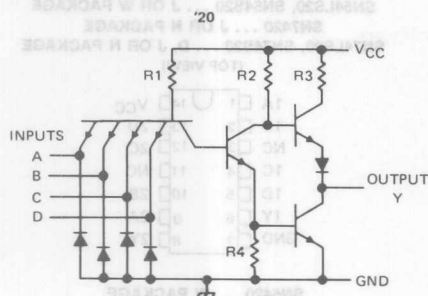
NC - No internal connection

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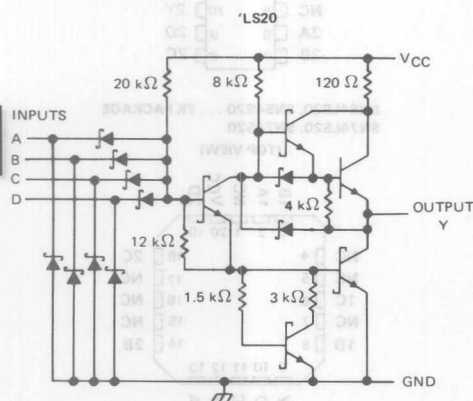
TTL DEVICES

TYPES SN5420, SN54LS20, SN54S20 **SN7420, SN74LS20, SN74S20** **DUAL 4-INPUT POSITIVE-NAND GATES**

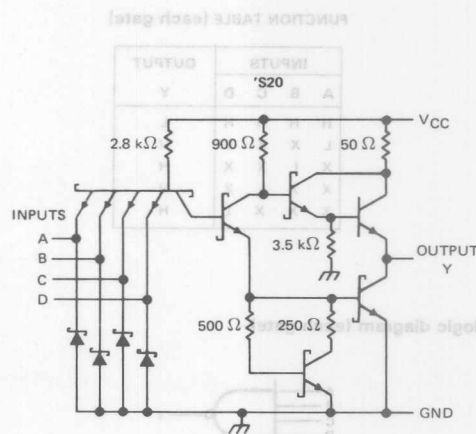
schematics (each gate)



CIRCUIT	R1	R2	R3	R4
'20	4 k Ω	1.6 k Ω	130 Ω	1 k Ω



Resistor values shown are nominal.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '20, 'LS20, 'S20	7 V
Input voltage: '20, 'S20	5.5 V
'LS20	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5420, SN7420 DUAL 4-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN5420			SN7420			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5420			SN7420			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		2	4		2	4	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		6	11		6	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		12	22	ns
t_{PHL}					8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS20, SN74LS20 DUAL 4-INPUT POSITIVE-NAND GATES

recommended operating conditions

UNIT	SN54LS20			SN74LS20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	V
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.8	V
I _{OH}	High-level output current					-0.4	mA
I _{OL}	Low-level output current					8	mA
T _A	Operating free-air temperature			-55	125	0	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS20			SN74LS20			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4			0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.25	0.5	V
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS} §	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		0.4	0.8		0.4	0.8	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		1.2	2.2		1.2	2.2	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 2 kΩ, C _L = 15 pF		9	15	ns
t _{PHL}					10	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S20, SN74S20 DUAL 4-INPUT POSITIVE-NAND GATES

recommended operating conditions

		SN54S20			SN74S20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-1			-1	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S20			SN74S20			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		5	8		5	8	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		10	18		10	18	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B, C or D	Y	R _L = 280 Ω, C _L = 15 pF		3	4.5	ns
t _{PHL}					3	5	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		4.5		ns
t _{PHL}					5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS21, SN74LS21 DUAL 4-INPUT POSITIVE-AND GATES

REVISED APRIL 1985

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

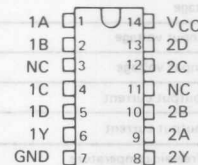
description

These devices contain two independent 4-input AND gates.

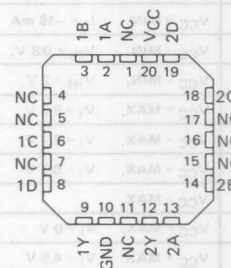
The SN54LS21 is characterized for operation over the full military temperature range of -55°C to 125°C. The

SN74LS21 is characterized for operation from 0°C to 70°C.

SN54LS21 ... J OR W PACKAGE SN74LS21 ... D, J OR N PACKAGE (TOP VIEW)



SN54LS21 ... FK PACKAGE SN74LS21 (TOP VIEW)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

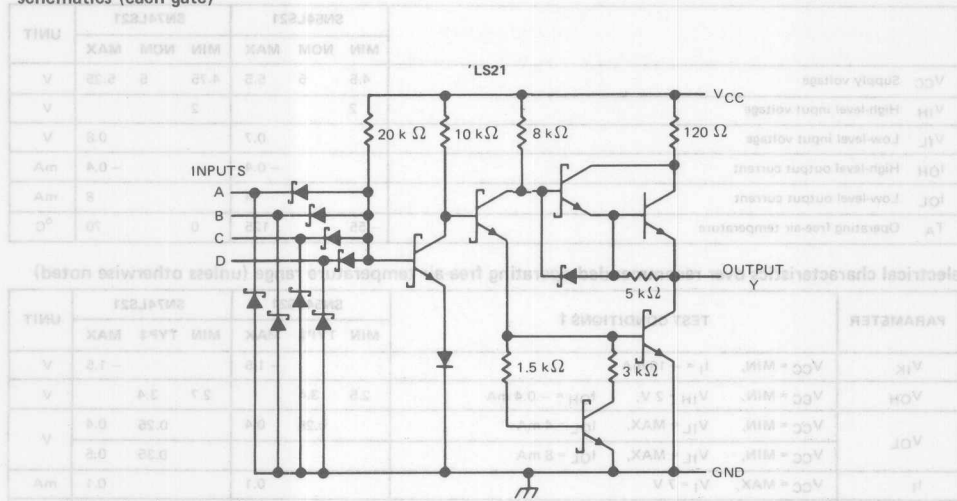
logic diagram (each gate)



PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN. TYP. MAX. UNIT
t_{PLH}	A, B, C, D	Y	$R_L = 300 \Omega$ $C_L = 15 \text{ pF}$ $R_T = 200 \Omega$ $C_T = 50 \text{ pF}$	3 ns
t_{PLL}				3 ns
t_{PLH}				3 ns
t_{PLL}				3 ns
positive logic				
$Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A + B + C + D}$				

TYPES SN54LS21, SN74LS21 DUAL 4-INPUT POSITIVE-AND GATES

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS21	7 V
Operating temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$C_L = 15 \text{ pF}$			10	ns
t_{PHL}	$C_L = 15 \text{ pF}$			10	ns

NOTE 2: See General Information Section for load circuit and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS21, SN74LS21 DUAL 4-INPUT POSITIVE-AND GATES

recommended operating conditions

	SN54LS21			SN74LS21			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS21			SN74LS21			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 8 mA				0.35	0.5		
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS} §	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 4.5 V		1.2	2.4		1.2	2.4	mA
I _{CCL}	V _{CC} = MAX, V _I = 0 V		2.2	4.4		2.2	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 2 kΩ, C _L = 15 pF		8	15	ns
t _{PHL}					10	20	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN5422, SN54LS22, SN54S22, SN7422, SN74LS22, SN74S22 DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 4-input NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5422, SN54LS22 and SN54S22 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7422, SN74LS22 and SN74S22 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (each gate)



positive logic

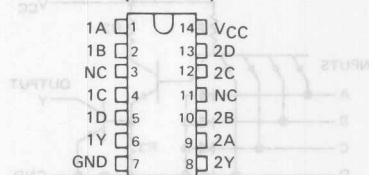
$$Y = A \cdot B \cdot C \cdot D \text{ or } Y = \overline{A + B + C + D}$$

SN5422, SN54LS22, SN54S22 ... J OR W PACKAGE

SN7422 ... J OR N PACKAGE

SN74LS22, SN74S22 ... D, J OR N PACKAGE

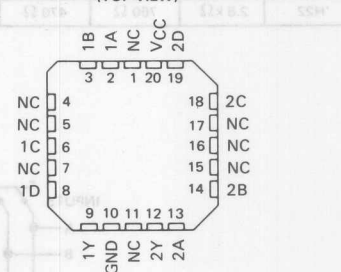
(TOP VIEW)



SN54LS22, SN54S22 ... FK PACKAGE

SN74LS22, SN74S22

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

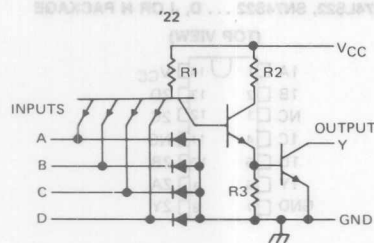
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

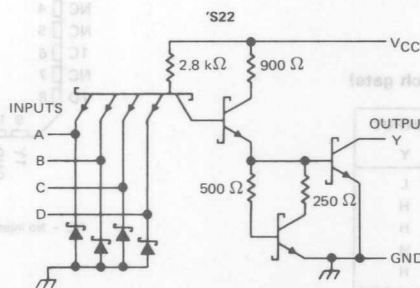
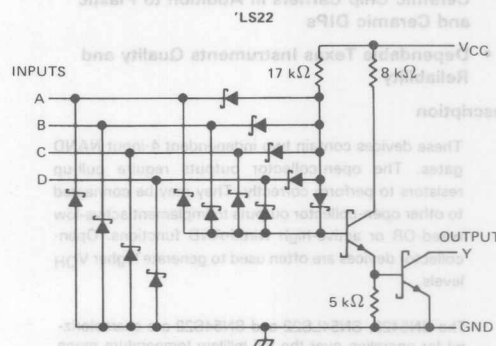
TEXAS
INSTRUMENTS

**TYPES SN5422, SN54LS22, SN54S22
SN7422, SN74LS22, SN74S22
DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

schematics (each gate)



CIRCUIT	R1	R2	R3
'22	4 k Ω	1.6 k Ω	1 k Ω
'H22	2.8 k Ω	760 Ω	470 Ω



Resistor values shown are nominal.

logic diagram (each gate)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '22, 'S22	5.5 V
'LS22	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

recommended operating conditions

UNIT	SN5422			SN7422			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -12 mA		-1.5		V
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V		0.25		mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V		1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V		40		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-1.6		mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		2	4	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		6	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 4 k Ω, C _L = 15 pF		35	45	ns
t _{PHL}			R _L = 400 Ω, C _L = 15 pF		8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS22			SN74LS22			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS22			SN74LS22			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1				0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20				20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4				-0.4	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.4	0.8		0.4	0.8	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		1.2	2.2		1.2	2.2	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		17	32	ns
t_{PHL}					15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S22, SN74S22 DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54S22			SN74S22			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2	V
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V			0.25	mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50	μA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		3	6.6	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		10	18	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	2	5	7.5	ns
t_{PHL}				2	4.5	7	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		7.5		ns
t_{PHL}					7		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S22, SN74S22 DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	SN54S22		SN74S22		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5	4.75	5	V
V_{IH} High-level input voltage	3		3		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_{OH} High-level output voltage		2.5		2.5	V
I_{OL} Low-level output current		20		20	mA
T_A Operating free-air temperature	-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -15 \text{ nA}$			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 0.8 \text{ V}$, $V_{OL} = 0.2 \text{ V}$			-25	mA
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 3 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5	V
I_I	$V_{CC} = \text{MAX}$, $V_I = 0.8 \text{ V}$			1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 3 \text{ V}$			50	nA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.8 \text{ V}$			-2	mA
I_{OCH}	$V_{CC} = \text{MAX}$, $V_I = 0.8 \text{ V}$			5	mA
I_{OCL}	$V_{CC} = \text{MAX}$, $V_I = 4.5 \text{ V}$			15	mA

1 For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
2 All test values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 200 \Omega$	2	2.5	ns	
t_{PLL}					4.5	ns	
t_{PHL}			$R_L = 200 \Omega$	2	2.5	ns	
t_{PLL}				4	ns		

NOTE 2: See General Information Section for load circuit and voltage waveforms.

3 TTL DEVICES

TYPES SN5423, SN5425, SN7423, SN7425 DUAL 4-INPUT NOR GATES WITH STROBE

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain dual 4-input positive NOR gates with strobe. The SN5423 and SN7423 are expandable, and perform the Boolean functions:

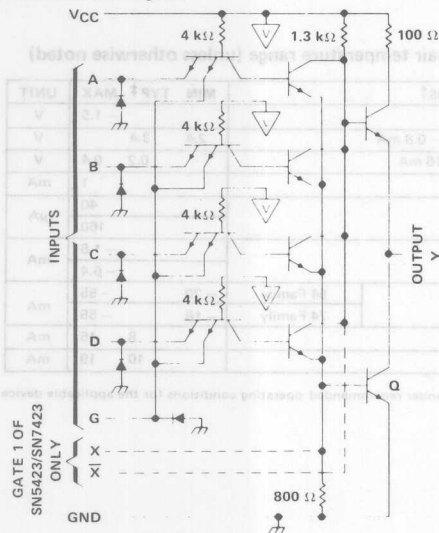
$$1Y = 1G(1A \cdot 1B \cdot 1C \cdot 1D) \cdot X \text{ and} \\ 2Y = 2G(2A \cdot 2B \cdot 2C \cdot 2D)$$

with X output of SN5460/SN7460. The SN5425 and SN7425 perform the Boolean function:

$$Y = G(A \cdot B \cdot C \cdot D)$$

The SN5423 and the SN5425 are characterized for operation over the full military temperature range of 55°C to 125°C. The SN7423 and the SN7425 are characterized for operation from 0°C to 70°C.

schematic (each gate)

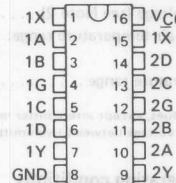


- Notes:
- Component values shown are nominal.
 - Both expander inputs are used simultaneously for expanding.
 - If expander is not used leave X and X open.
 - A total of four expander gates can be connected to the expander inputs.

VCC bus

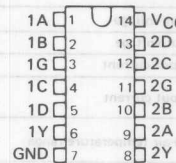
SN5423 ... J OR W PACKAGE
SN7423 ... J OR N PACKAGE

(TOP VIEW)

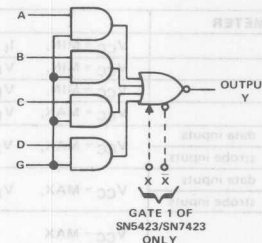


SN5425 ... J OR W PACKAGE
SN7425 ... J OR N PACKAGE

(TOP VIEW)



logic diagram



TRUTH TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H
X	X	X	X	H

Expander inputs are open.

H = high level, L = low level, X = irrelevant

3

TTL DEVICES

TYPES SN5423, SN5425, SN7423, SN7425 DUAL 4-INPUT NOR GATES WITH STROBE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5423, SN5425 Circuits	– 55°C to 125°C
SN7423, SN7425 Circuits	0°C to 70°C
Storage temperature range	– 65°C to 150°C

- NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		'23, '25			UNIT
		MIN	NOM	MAX	
V_{CC} Supply voltage	54 Family	4.5	5	5.5	V
	74 Family	4.75	5	5.25	
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
I_{OH} High-level output current				– 0.8	mA
I_{OL} Low-level output current	54 Family			16	mA
	74 Family			16	
T_A Operating free-air temperature range	54 Family	– 55		125	°C
	74 Family	0		70	

The '23 is designed for use with up to four '60 expanders.

3

TTL DEVICES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_I		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				– 1.5	V
V_{OH}		$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.8 \text{ mA}$		2.4	3.4		V
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	data inputs	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40	μA
	strobe inputs					160	
I_{IL}	data inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				– 1.6	mA
	strobe inputs					– 6.4	
$I_{OS}\S$		$V_{CC} = \text{MAX}$	54 Family	– 20		– 55	mA
			74 Family	– 18		– 55	
I_{CCH}		$V_{CC} = \text{MAX}, \text{ All inputs at } 0 \text{ V}$			8	16	mA
I_{CCL}		$V_{CC} = \text{MAX}, \text{ All inputs at } 5 \text{ V}$			10	19	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and \bar{X} are open.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

TYPES SN5423, SN5425, SN7423, SN7425 DUAL 4-INPUT NOR GATES WITH STROBE

electrical characteristics (SN5423 circuits) using expander inputs, $V_{CC} = 4.5 \text{ V}$, $T_A = -55^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I_{\bar{X}}$ Expander current	$V_{X\bar{X}} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$			-3.5	mA
$V_{BE(Q)}$ Base-Emitter voltage of output transistor (Q)	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.41 \text{ mA}$, $R_{X\bar{X}} = 0$			1.1	V
V_{OH} High-level output voltage	$I_{OH} = -0.4 \text{ mA}$, $I_X = 0.15 \text{ mA}$, $I_{\bar{X}} = -0.15 \text{ mA}$	2.4	3.4		V
V_{OL} Low-level output voltage	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.3 \text{ mA}$, $R_{X\bar{X}} = 114 \Omega$	0.2	0.4		V

electrical characteristics (SN7423 circuits) using expander inputs, $V_{CC} = 4.75 \text{ V}$, $T_A = 0^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I_{\bar{X}}$ Expander current	$V_{X\bar{X}} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$			-3.8	mA
$V_{BE(Q)}$ Base-Emitter voltage of output transistor (Q)	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.62 \text{ mA}$, $R_{X\bar{X}} = 0$			1	V
V_{OH} High-level output voltage	$I_{OH} = -0.4 \text{ mA}$, $I_X = 0.27 \text{ mA}$, $I_{\bar{X}} = -0.27 \text{ mA}$	2.4	3.4		V
V_{OL} Low-level output voltage	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.43 \text{ mA}$, $R_{X\bar{X}} = 130 \Omega$	0.2	0.4		V

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$, (see note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$		13	22	ns
t_{PHL}	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$		8	15	ns

NOTE 3: Switching characteristics of the SN5423 and SN7424 are tested with the expander pins open.

3

TTL DEVICES

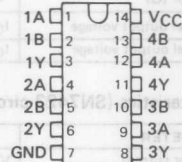
TYPES SN5426, SN54LS26, SN7426, SN74LS26 QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

REVISED DECEMBER 1983

- For Driving Low-Threshold-Voltage MOS Inputs

SN5426 ... J PACKAGE
 SN54LS26 ... J OR W PACKAGE
 SN7426 ... J OR N PACKAGE
 SN74LS26 ... D, J OR N PACKAGE

(TOP VIEW)



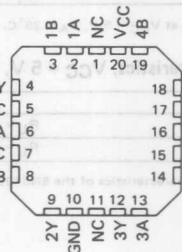
description

These 2-input open-collector NAND gates feature high-output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source.

The SN5426 and SN54LS26 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7426 and SN74LS26 are characterized for operation from 0°C to 70°C.

SN54LS26 ... FK PACKAGE
 SN74LS26

(TOP VIEW)



logic diagram (each gate)



NC - No internal connection

positive logic

$$Y = \overline{AB}$$

3

TTL DEVICES

PRODUCTION DATA

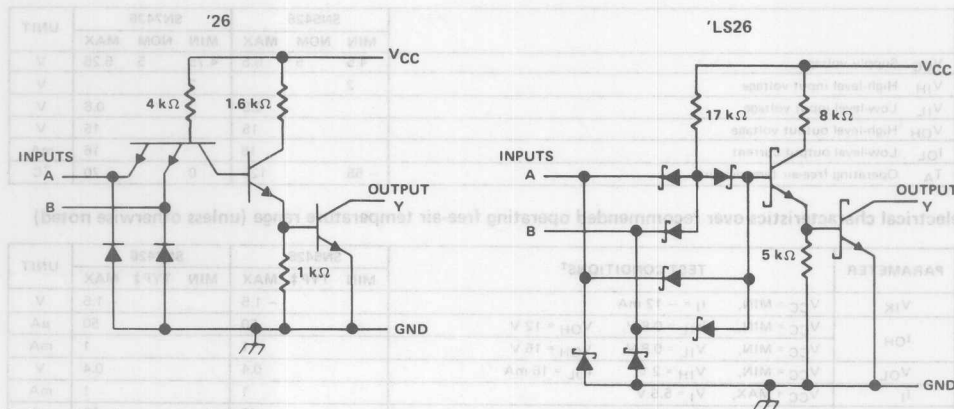
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS
 INSTRUMENTS

TYPES SN5426, SN54LS26, SN7426, SN74LS26
QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

schematics



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '26	5.5 V
'LS26	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5426, SN7426
QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

recommended operating conditions

	SN5426			SN7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_{OH} High-level output voltage			15			15	V
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5426			SN7426			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5			-1.5		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 12 \text{ V}$			50			50	μA
	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 15 \text{ V}$			1			1	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$			0.4			0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$			4			4	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$			12			12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}$		16	24	ns
t_{PHL}					11	17	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS26, SN74LS26 QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

recommended operating conditions

	SN54LS26			SN74LS26			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
V _{OH} High-level output voltage			15			15	V
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS26			SN74LS26			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
I _{OH}	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 12 V			50			50	μA
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 15 V			1			1	mA
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	V
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _{IH} = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _{IL} = 0.4 V		-0.4			-0.4		mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		0.8	1.6		0.8	1.6	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 2 kΩ, C _L = 15 pF		17	32	ns
t _{PHL}					15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5427, SN54LS27, SN7427, SN74LS27 TRIPLE 3-INPUT POSITIVE-NOR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain three independent 3-input NOR gates.

The SN5427 and SN54LS27 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7427 and SN74LS27 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic diagram (each gate)

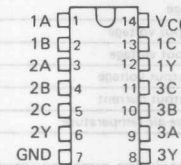


positive logic

$$Y = \overline{A + B + C} \text{ or } Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

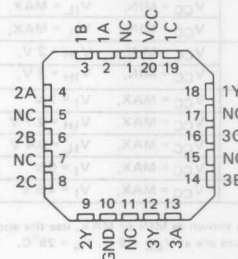
SN5427, SN54LS27 ... J OR W PACKAGE
SN7427 ... J OR N PACKAGE
SN74LS27 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS27 ... FK PACKAGE
SN74LS27

(TOP VIEW)



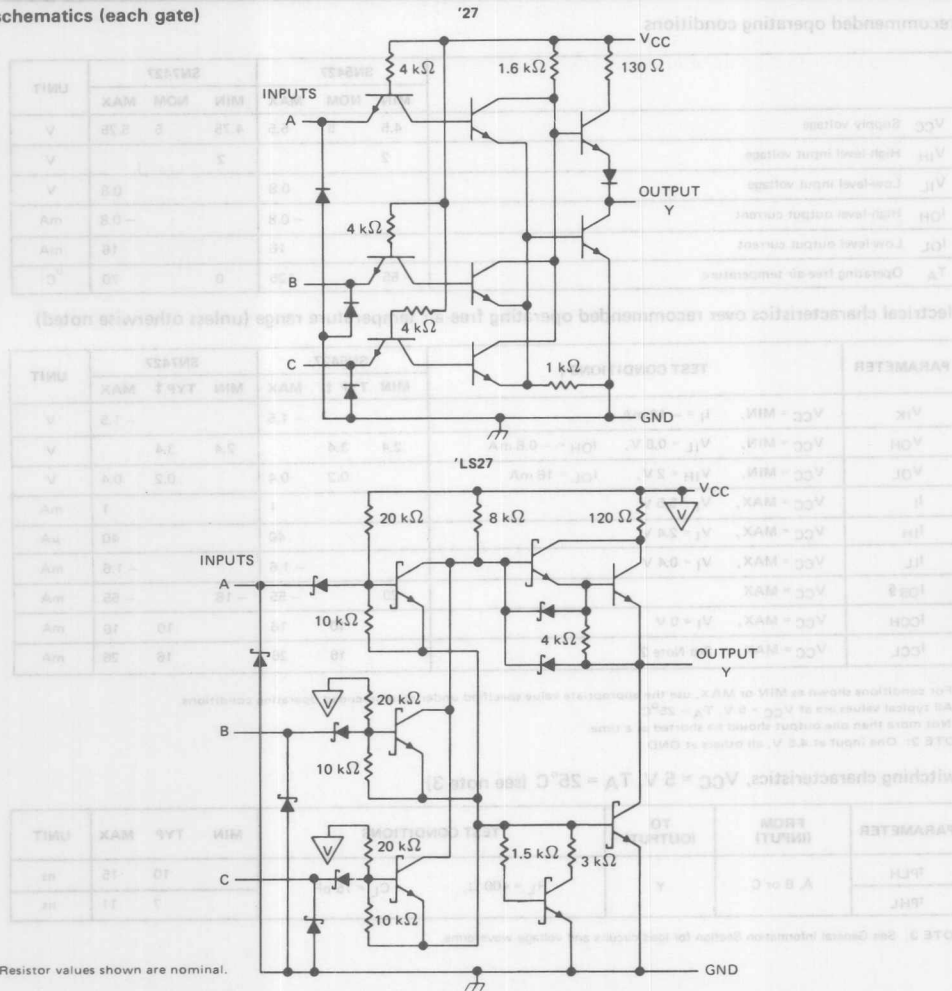
NC - No internal connection

3

TTL DEVICES

TYPES SN5427, SN54LS27, SN7427, SN74LS27 TRIPLE 3-INPUT POSITIVE-NOR GATES

schematics (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '27	5.5 V
'LS27	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5427, SN7427
TRIPLE 3-INPUT POSITIVE-NOR GATES

recommended operating conditions

	SN5427			SN7427			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-0.8			-0.8	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5427		SN7427		UNIT
		MIN	TYP ‡	MIN	TYP ‡	
V _{IK}	V _{CC} = MIN, I _I = -12 mA		-1.5		-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -0.8 mA	2.4	3.4	2.4	3.4	V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2		0.2	V
I _I	V _{CC} = MAX, V _I = 5.5 V		1		1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V		40		40	µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-1.6		-1.6	mA
I _{OS} §	V _{CC} = MAX	-20	-55	-18	-55	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		10		10	mA
I _{CCL}	V _{CC} = MAX, See Note 2		16		16	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 400 Ω, C _L = 15 pF		10	15	ns
t _{PHL}					7	11	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS27, SN74LS27 TRIPLE 3-INPUT POSITIVE-NOR GATES

recommended operating conditions

	SN54LS27			SN74LS27			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS27		SN74LS27		UNIT
		MIN	TYP ‡	MIN	TYP ‡	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4	2.7	3.4	V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$			0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1		0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20		20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4		-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20	-100	-20	-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	2	4	2	4	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$	3.4	6.8	3.4	6.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B or C	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		10	15	ns
t_{PHL}					10	15	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN5428, SN54LS28, SN7428, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NOR buffer gates.

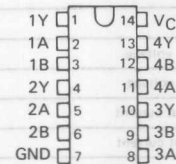
The SN5428, and SN54LS28 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7428, and SN74LS28 are characterized for operation from 0°C to 70°C.

SN5428, SN54LS28 ... J OR W PACKAGE

SN7428 ... J OR N PACKAGE

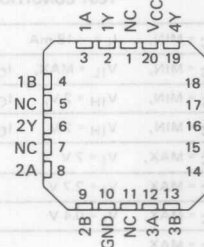
SN74LS28 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS28 ... FK PACKAGE
SN74LS28

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

3

logic diagram (each gate)



positive logic

$$Y = \overline{A + B} \text{ or } Y = \overline{A} \cdot \overline{B}$$

TTL DEVICES

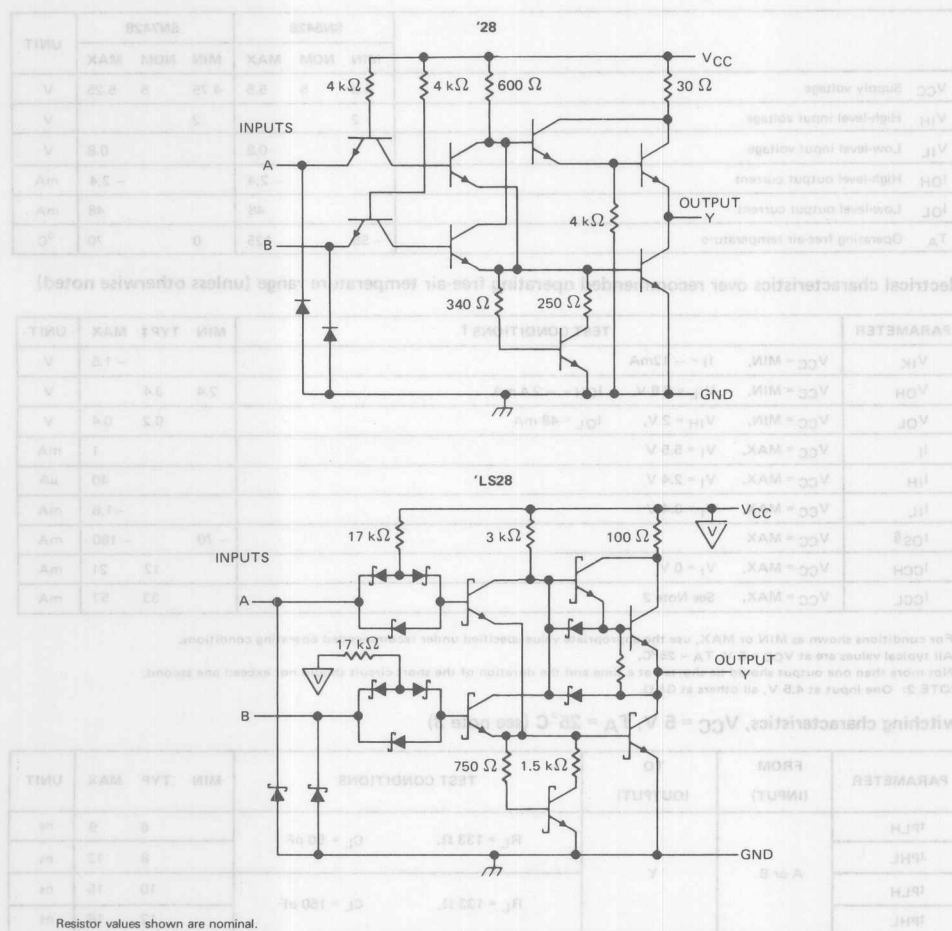
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	A, B = 0	Y	V _{CC} = 5V, T _A = 25°C	0	10	15	mV
				0	10	15	mV

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TYPES SN5428, SN54LS28, SN7428, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

schematics (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '28	5.5 V
'LS28	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5428, SN7428 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

recommended operating conditions

	SN5428			SN7428			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-2.4			-2.4	mA
I _{OL} Low-level output current			48			48	mA
T _A Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -12mA		-1.5		V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -2.4 mA	2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 48 mA		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40	µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6	mA
I _{OS} §	V _{CC} = MAX	-70		-180	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		12	21	mA
I _{CCL}	V _{CC} = MAX, See Note 2		33	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 133 Ω, C _L = 50 pF		6	9	ns
t _{PHL}					8	12	ns
t _{PLH}			R _L = 133 Ω, C _L = 150 pF		10	15	ns
t _{PHL}					12	18	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS28, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

recommended operating conditions

	SN54LS28			SN74LS28			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-1.2			-1.2	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS28			SN74LS28			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -1.2 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.24	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-30		-130	-30		-130	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		1.8	3.6		1.8	3.6	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		6.9	13.8		6.9	13.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{FLH}	A or B	Y	$R_L = 667 \Omega, C_L = 45 \text{ pF}$		12	24	ns
t_{PHL}					12	24	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

recommended operating conditions

PARAMETER	SN74L258		SN74L258	
	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	3			V
V_{IL} Low-level input voltage	0.7			V
I_{OH} High-level output current	-1.5			mA
I_{OL} Low-level output current	15			mA
T_A Operating free-air temperature	-55	125	0	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74L258		SN74L258	
			MIN	TYP	MAX	UNIT
V_{IC}	$V_{CC} = \text{MIN}$	$I_C = -15 \text{ mA}$	-1.5			V
V_{OH}	$V_{CC} = \text{MIN}$	$I_{OH} = -1.5 \text{ mA}$	3.5	3.8	4.0	V
V_{OL}	$V_{CC} = \text{MIN}$	$I_{OL} = 15 \text{ mA}$	0.5	0.6	0.7	V
	$V_{CC} = \text{MIN}$	$I_{OL} = 15 \text{ mA}$	0.5	0.6	0.7	V
I_I	$V_{CC} = \text{MAX}$	$V_I = 1 \text{ V}$	0.1			mA
I_{IH}	$V_{CC} = \text{MAX}$	$V_I = 1 \text{ V}$	20			mA
I_{IL}	$V_{CC} = \text{MAX}$	$V_I = 0 \text{ V}$	-0.4			mA
I_{OZ}	$V_{CC} = \text{MAX}$		-20	-100	-150	mA
I_{OCH}	$V_{CC} = \text{MAX}$	$V_I = 0 \text{ V}$	1.5	3.5	5.5	mA
I_{OCL}	$V_{CC} = \text{MAX}$	See Note 2	5.5	15.5	25	mA

1. All conditions shown at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise specified.
2. All test conditions are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.
3. Load capacitance $C_L = 50 \text{ pF}$ unless otherwise specified.
4. Input transition time $t_{tr} = 10 \text{ ns}$ unless otherwise specified.
5. Input signal is 50% duty cycle square wave.
6. Output signal is 50% duty cycle square wave.
7. Output signal is 50% duty cycle square wave.
8. Output signal is 50% duty cycle square wave.
9. Output signal is 50% duty cycle square wave.
10. Output signal is 50% duty cycle square wave.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		UNIT
			MIN	TYP	
t_{PLH}	A or B	Y		13	ns
t_{PLL}	A or B	Y		13	ns

NOTE 3: See General Information Section for load circuit and voltage waveform.

TYPES SN5430, SN54LS30, SN54S30, SN7430, SN74LS30, SN74S30 8-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

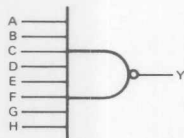
These devices contain a single 8-input NAND gate.

The SN5430, SN54LS30, and SN54S30 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7430, SN74LS30, and SN74S30 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

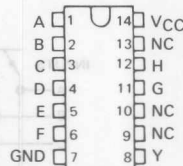
logic diagram



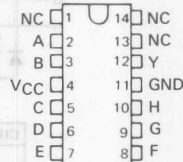
positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{or} \\ Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

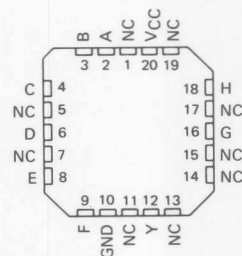
SN5430 ... J PACKAGE
SN54LS30, SN54S30 ... J OR W PACKAGE
SN7430 ... J OR N PACKAGE
SN74LS30, SN74S30 ... D, J OR N PACKAGE
(TOP VIEW)



SN5430 ... W PACKAGE
(TOP VIEW)



SN54LS30, SN54S30 ... FK PACKAGE
SN74LS30, SN74S30
(TOP VIEW)



NC - No internal connection

3

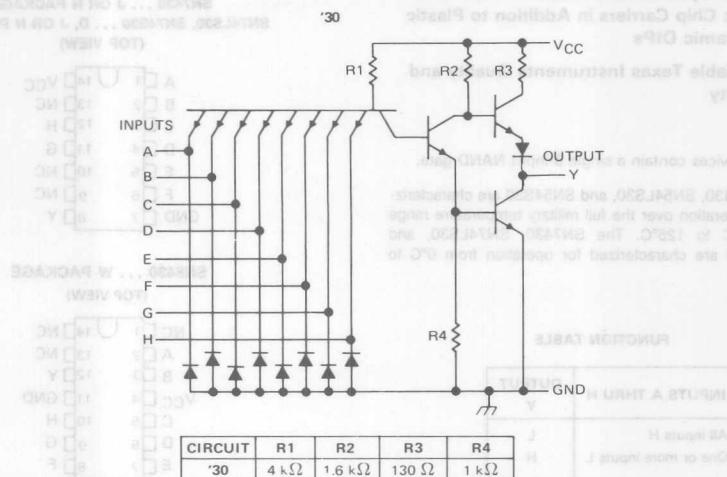
TTL DEVICES

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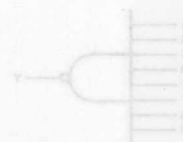
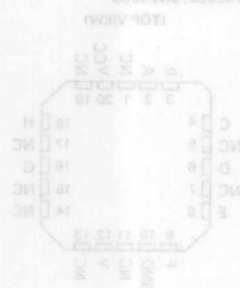
TEXAS
INSTRUMENTS

TYPES SN5430, SN7430 8-INPUT POSITIVE-NAND GATES

schematics (each gate)



Input clamp diodes not on SN54L30 circuit.



$$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$$

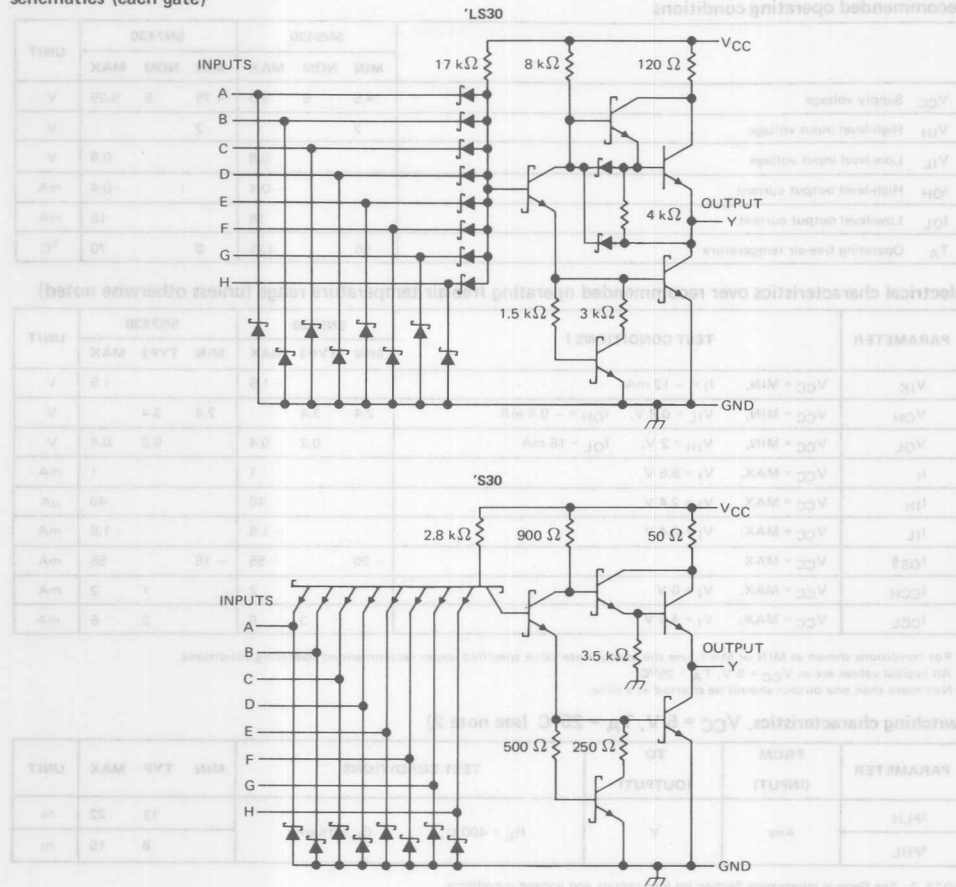
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

3

TTL DEVICES

**TYPES SN5430, SN54LS30, SN54S30
SN7430, SN74LS30, SN74S30
8-INPUT POSITIVE-NAND GATES**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '30, 'LS30, 'S30	7 V
Input voltage: '30, 'S30	5.5 V
'LS30	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5430, SN7430

8-INPUT POSITIVE-NAND GATES

recommended operating conditions

	SN5430			SN7430			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5430			SN7430			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6	mA
I _{OS} §	V _{CC} = MAX	-20		-55	-18		-55	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		1	2		1	2	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		3	6		3	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 400 Ω, C _L = 15 pF		13	22	ns
t _{PHL}					8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS30, SN74LS30 8-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS30			SN74LS30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55	125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS30			SN74LS30			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.5	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$							
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.35	0.5		0.35	0.5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		0.6	1.1		0.6	1.1	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		8	15	ns
t_{PHL}					13	20	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54S30, SN74S30 8-INPUT POSITIVE-NAND GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54S30			SN74S30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S30			SN74S30			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		3	5		3	5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		5.5	10		5.5	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		4	6	ns
t_{PHL}					4.5	7	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		5.5		ns
t_{PHL}					6.5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS31, SN74LS31 DELAY ELEMENTS

REVISED DECEMBER 1983

- Delay Elements for Generating Delay Lines
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at IOL of 12/24 mA
- PNP Inputs Reduce Fan-In ($I_{IL} = -0.2$ mA MAX)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Ranges

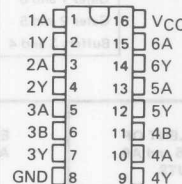
description

These 'LS31 delay elements are intended to provide well-defined delays across both temperature and V_{CC} ranges. Used in cascade, a limitless range of delay gating is possible.

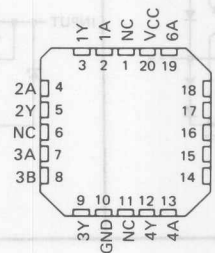
All inputs are PNP with I_{IL} MAX of -0.2 mA. Gates 1, 2, 5, and 6 have standard Low-Power Schottky output sink current capability of 4 and 8 mA IOL. Buffers 3 and 4 are rated at 12 and 24 mA.

The SN54LS31 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS31 is characterized for operation from 0°C to 70°C .

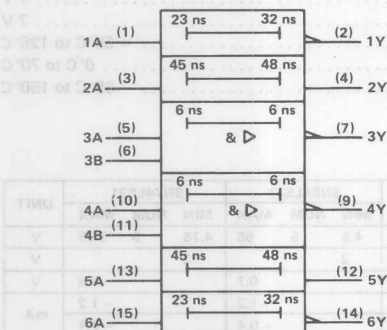
SN54LS31 ... J OR W PACKAGE
SN74LS31 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS31 ... FK PACKAGE
SN74LS31
(TOP VIEW)



logic symbol†



† Pin numbers shown on logic notation are for D, J and N packages only.

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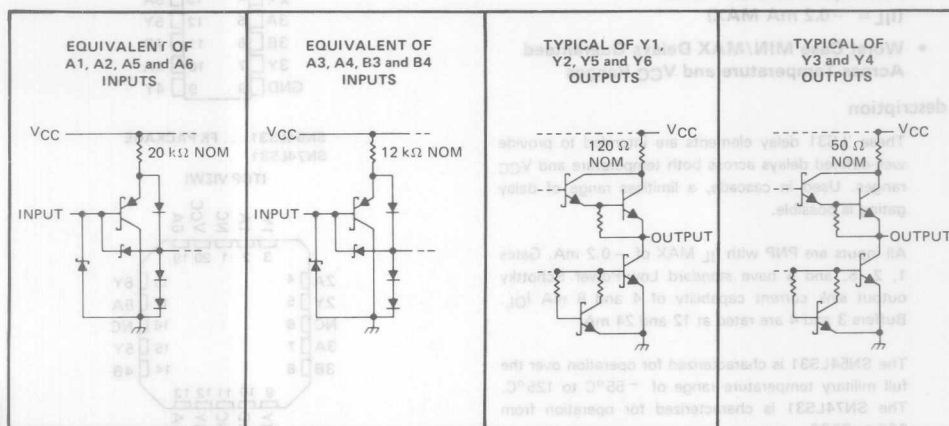


3

TTL DEVICES

TYPES SN54LS31, SN74LS31 DELAY ELEMENTS

Delay Element	Logic	Typical Delays			Rated I _{OL}
		t _{PLH}	t _{PHL}	AVG.	
Gates 1 and 6	Inverting	32 ns	23 ns	27.5 ns	4 and 8 mA
Gates 2 and 5	Non-Inverting	45 ns	48 ns	46.5 ns	4 and 8 mA
Buffers 3 and 4	2-Input NAND	6 ns	6 ns	6 ns	12 and 24 mA



3

TTL DEVICES

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (See Note 1)	7 V
Input voltage, V _I : All inputs	7 V
Operating free-air temperature range: SN54LS31	–55°C to 125°C
SN74LS31	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS31			SN74LS31			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			–1.2			–1.2	mA
	Y3, Y4 outputs			–1.2			–1.2	
	All other outputs			–0.4			–0.4	
I _{OL}	Low-level output current			12			24	mA
	Y3, Y4 outputs			12			24	
	All other outputs			4			8	
T _A	Operating free-air temperature	–55		125	0		70	°C

TYPES SN54LS31, SN74LS31 DELAY ELEMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†				SN54LS31			SN74LS31			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$						-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	Y3, Y4	$I_{OH} = -1.2 \text{ mA}$		2.4	3.1		2.4	3.1		V
		Others	$I_{OH} = -0.4 \text{ mA}$		2.5	3.1		2.7	3.1		
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	Y3, Y4	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4		V
			$I_{OL} = 24 \text{ mA}$					0.35	0.5		
		Others	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4		
			$I_{OL} = 8 \text{ mA}$					0.35	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$						0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$						20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$						-0.2			-0.2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}, A3, A4, B3, B4 = 0 \text{ V}$	Y3, Y4			-30	-130		-30	-130		mA
	$V_{CC} = \text{MAX}, A1, A6 = 0 \text{ V}, A2, A5 = 4.5 \text{ V}$	Y1, Y2, Y5, Y6			-20	-100		-20	-100		
I_{CC}	I_{CCH}	$V_{CC} = \text{MAX}, A2, A5 = 4.5 \text{ V},$	all other inputs 0 V		2.3	4		2.3	4		mA
	I_{CCL}	$V_{CC} = \text{MAX}, A2, A5 = 0 \text{ V},$	all other inputs 4.5 V		13	20		13	20		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LS31			SN74LS31			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A1, A6	Y1, Y6	15		70	22		65	ns
t_{PHL}			9		50	13		45	ns
t_{PLH}	A2, A5	Y2, Y5	22		90	31		80	ns
t_{PHL}			20		105	30		95	ns
t_{PLH}	A3, B3, A4, Y4	Y3, Y4	2		20	2		15	ns
t_{PHL}			2		20	2		15	ns

NOTE 2: $V_{CC} = \text{MIN to MAX}$

$R_L = 667 \Omega, C_L = 45 \text{ pF}$ for Y3 and Y4.

$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$ for Y1, Y2, Y5 and Y6.

$T_A = \text{MIN to MAX}$

See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹				52A1531		52A1532		UNIT
					MIN TYPE MAX		MIN TYPE MAX		
V_{CC}	$V_{CC} = \text{MIN.}$	$I = -10 \text{ mA}$			-1.8				V
	$V_{CC} = \text{MAX.}$	$V_{IH} = 3 \text{ V}$			-1.8				V
V_{OH}	$V_{OH} = \text{MIN.}$	$V_{IH} = 3 \text{ V}$			2.4				V
	$V_{OH} = \text{MAX.}$	$V_{IH} = 3 \text{ V}$			2.4				V
V_{OL}	$V_{OL} = \text{MIN.}$	$V_{IH} = 3 \text{ V}$			0.25				V
	$V_{OL} = \text{MAX.}$	$V_{IH} = 3 \text{ V}$			0.25				V
I_L	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.1				mA
	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.1				mA
I_{IH}	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
I_{IL}	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
I_{OS}	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
I_{CC}	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA
	$V_{CC} = \text{MAX.}$	$V_I = 3 \text{ V}$			-0.2				mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.
3. Test waveforms should be applied as shown and the duration of the test should be as specified.

Switching characteristics (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	52A1531			52A1532		
			MIN	TYPE	MAX	MIN	TYPE	MAX
t_{PLH}	A1, A2	Y1, Y2	10		10	10		10
t_{PHL}	A1, A2	Y1, Y2	10		10	10		10
t_{PLH}	A2, A3	Y2, Y3	10		10	10		10
t_{PHL}	A2, A3	Y2, Y3	10		10	10		10
t_{PLH}	A3, B3, A4	Y3, Y4	10		10	10		10
t_{PHL}	A3, B3, A4	Y3, Y4	10		10	10		10

NOTE 2: $V_{CC} = \text{MIN to MAX}$
 $R_L = 20 \text{ k}\Omega$, $C_L = 45 \text{ pF}$ for Y1 and Y2
 $R_L = 20 \text{ k}\Omega$, $C_L = 15 \text{ pF}$ for Y3 and Y4
 $T_A = \text{MIN to MAX}$
See General Information Section for test circuit and voltage waveforms

3 TTL DEVICES

TYPES SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C . The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram (each gate)



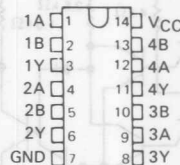
positive logic

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

SN5432, SN54LS32, SN54S32 ... J OR W PACKAGE
SN7432 ... J OR N PACKAGE

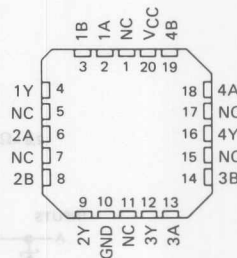
SN74LS32, SN74S32 ... D, J or N PACKAGE

(TOP VIEW)



SN54LS32, SN54S32 ... FK PACKAGE
SN74LS32, SN74S32

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

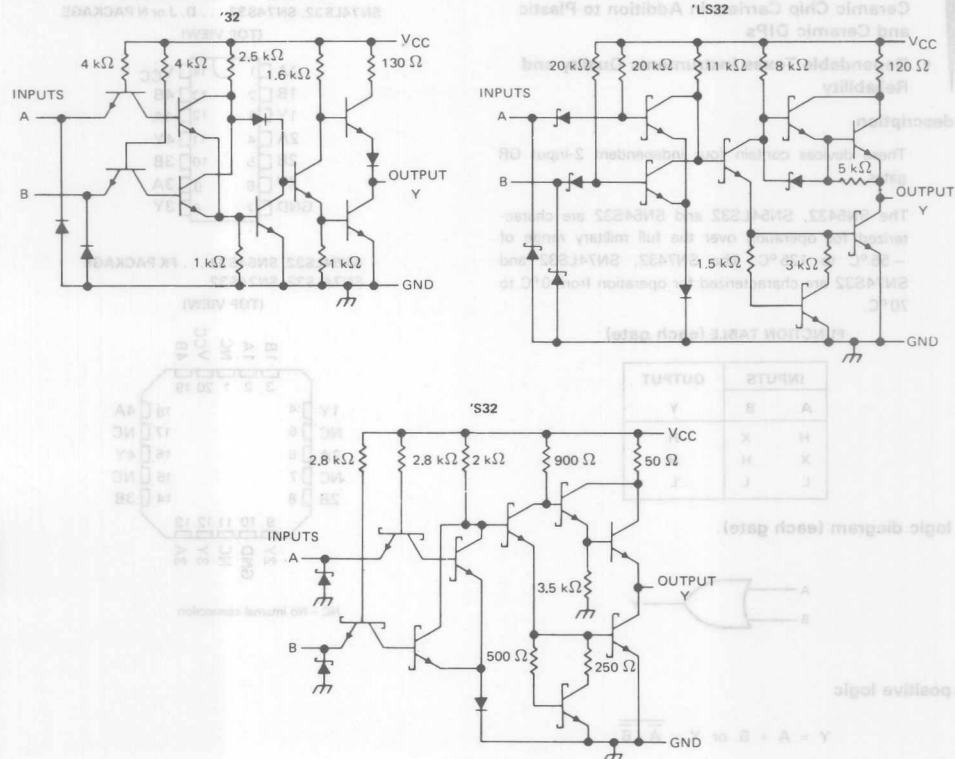
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '32, 'S32	5.5 V
'LS32	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5432, SN7432 QUADRUPLE 2-INPUT POSITIVE-OR GATES

recommended operating conditions

		SN5432			SN7432			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.8			-0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5432			SN7432			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -0.8 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		15	22		15	22	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		23	38		23	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 400 \Omega,$	$C_L = 15 \text{ pF}$		10	15	ns
t_{PHL}						14	22	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS32, SN74LS32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS32			SN74LS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS32			SN74LS32			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 8 \text{ mA}$				0.35	0.5		V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		3.1	6.2		3.1	6.2	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4.9	9.8		4.9	9.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		14	22	ns
t_{PHL}					14	22	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S32, SN74S32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

recommended operating conditions

	SN54S32			SN74S32			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-1			-1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S32			SN74S32			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}$, See Note 2		18	32		18	32	mA
I_{CCL}	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		38	68		38	68	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 280 \Omega$, $C_L = 15 \text{ pF}$			4	7	ns
t_{PHL}						4	7	ns
t_{PLH}	A or B	Y	$R_L = 280 \Omega$, $C_L = 50 \text{ pF}$			5		ns
t_{PHL}						5		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5433, SN54LS33, SN7433, SN74LS33 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

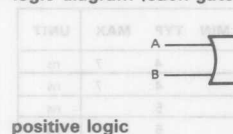
These devices contain four independent 2-input NOR buffer gates with open-collector outputs. Open-collector outputs require resistive pull-up to perform logically but can deliver higher V_{OH} levels and are commonly used in wired-AND applications.

The SN5433, and SN54LS33 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7433, and SN74LS33 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (each gate)



positive logic

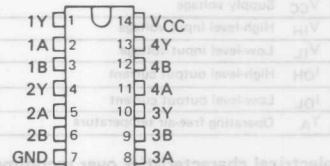
$$Y = \overline{A + B} \text{ or } Y = \overline{A} \cdot \overline{B}$$

SN5433, SN54LS33 ... J OR W PACKAGE

SN7433 ... J OR N PACKAGE

SN74LS33 ... D, J OR N PACKAGE

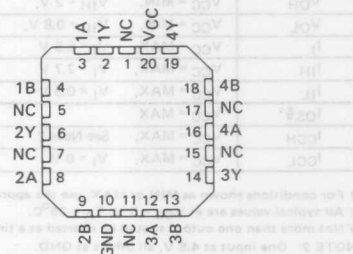
(TOP VIEW)



SN54LS33 ... FK PACKAGE

SN74LS33

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

PRODUCTION DATA

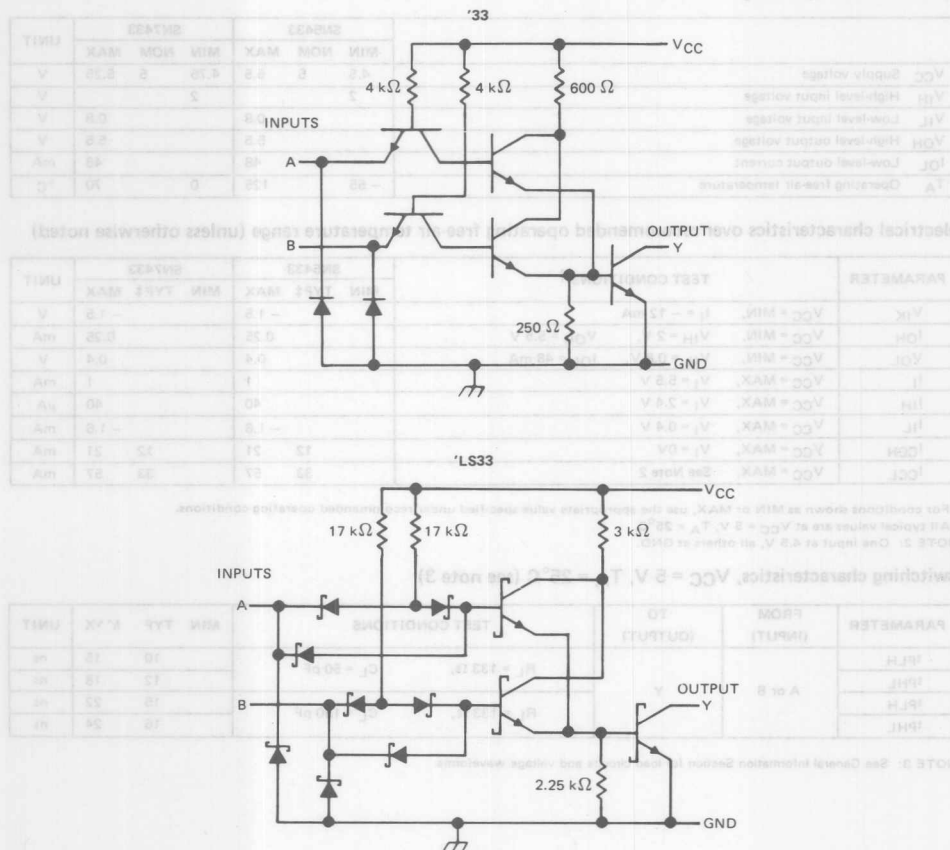
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TEXAS
INSTRUMENTS

TYPES SN5433, SN54LS33, SN7433, SN74LS33 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '33	5.5 V
'LS33	7 V
Off-state output voltage	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5433, SN7433 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN5433			SN7433			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			48			48	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5433			SN7433			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA		-1.5			-1.5		V
I _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V		0.25			0.25		mA
V _{OL}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 48 mA		0.4			0.4		V
I _I	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V		40			40		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-1.6			-1.6		mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		12	21		12	21	mA
I _{CCL}	V _{CC} = MAX, See Note 2		33	57		33	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 133 Ω,	C _L = 50 pF	10	15		ns
t _{PHL}					12	18		ns
t _{PLH}			R _L = 133 Ω,	C _L = 150 pF	15	22		ns
t _{PHL}					16	24		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS33, SN74LS33 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS33			SN74LS33			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS33			SN74LS33			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25			0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		1.8	3.6		1.8	3.6	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		6.9	13.8		6.9	13.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 667 \Omega, C_L = 45 \text{ pF}$		20	32	ns
t_{PHL}					18	28	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

QUADRUPEL 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS TYPES SN64LS33, SN74LS33

recommended operating conditions

PARAMETER	SN64LS33		SN74LS33	
	MIN	MAX	MIN	MAX
V_{CC} Supply voltage	4.5	5.5	4.5	5.5
V_{IH} High-level input voltage	3		3	
V_{IL} Low-level input voltage	0.5		0.5	
V_{OH} High-level output voltage	0.5		0.5	
I_{OL} Low-level output current	24		24	
T_A Operating free-air temperature	0	70	0	70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN64LS33		SN74LS33	
			MIN	MAX	MIN	MAX
V_{CC}	$V_{CC} = \text{MIN.}$	$I_L = -18 \text{ mA}$	-1.5		-1.5	
I_{OL}	$V_{CC} = \text{MIN.}$ $V_{IH} = 3 \text{ V}$	$V_{OH} = 2.5 \text{ V}$	0.5		0.5	
V_{OL}	$V_{CC} = \text{MIN.}$ $V_{IL} = \text{MAX.}$	$I_{OL} = 15 \text{ mA}$	0.5	0.4	0.5	0.4
V_{CC}	$V_{CC} = \text{MIN.}$ $V_{IL} = \text{MAX.}$	$I_{OL} = 24 \text{ mA}$	0.5	0.4	0.5	0.4
I_L	$V_{CC} = \text{MAX.}$ $V_I = 3 \text{ V}$		0.7		0.7	
I_{IH}	$V_{CC} = \text{MAX.}$ $V_I = 3 \text{ V}$		20		20	
I_{IL}	$V_{CC} = \text{MAX.}$ $V_I = 0 \text{ V}$		-0.4		-0.4	
I_{OCH}	$V_{CC} = \text{MAX.}$ $V_I = 0 \text{ V}$		1.5	3.5	1.5	3.5
I_{OCL}	$V_{CC} = \text{MAX.}$ $V_I = 3 \text{ V}$		0.5	13.5	0.5	13.5

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 ‡At typical values for $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
 NOTE 2: One input is 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 800 \Omega$			20	ns
t_{PHL}	A or B	Y	$C_L = 45 \text{ pF}$			15	ns

NOTE 3: See General Information Section for load circuit and voltage waveform.

3
 TTL DEVICES

TYPES SN5437, SN54LS37, SN54S37, SN7437, SN74LS37, SN74S37 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NAND buffer gates.

The SN5437, SN54LS37 and SN54S37 are characterized for operation over the full military range of -55°C to 125°C . The SN7437, SN74LS37 and SN74S37 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (each gate)



positive logic

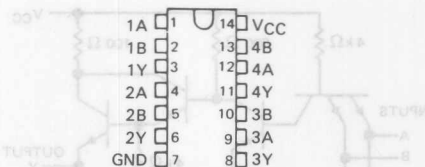
$$Y = A \cdot B \text{ or } Y = \overline{A + B}$$

SN5437, SN54LS37, SN54S37 ... J OR W PACKAGE

SN7437 ... J OR N PACKAGE

SN74LS37, SN74S37 ... D, J OR N PACKAGE

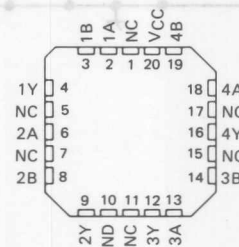
(TOP VIEW)



SN54LS37, SN54S37 ... FK PACKAGE

SN74LS37, SN74S37

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

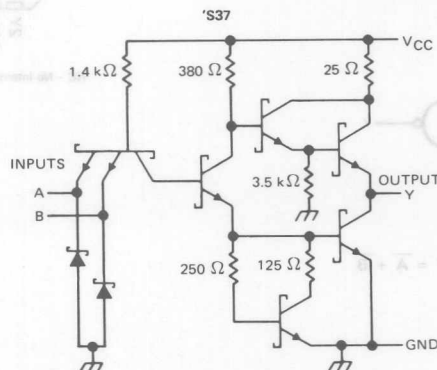
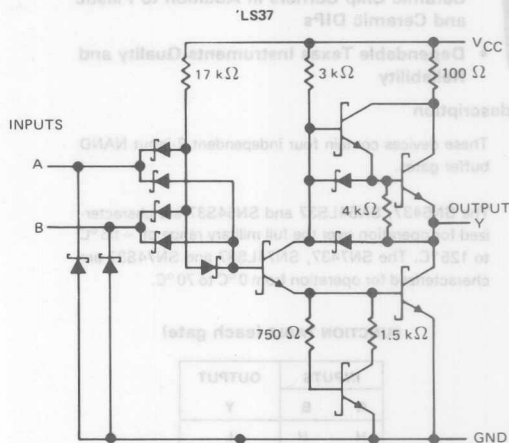
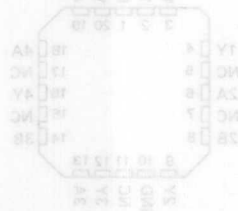
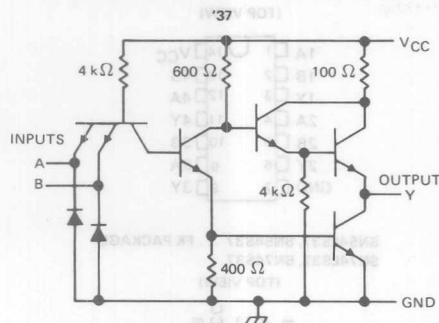
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

**TYPES SN5437, SN54LS37, SN54S37,
SN7437, SN74LS37, SN74S37
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '37, 'S37	5.5 V
'LS37	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5437, SN7437

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

PARAMETER	DESCRIPTION	SN5437			SN7437			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-1.2			-1.2	mA
I_{OL}	Low-level output current			48			48	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5437			SN7437			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1.2 \text{ mA}$	2.4	3.3		2.4	3.3		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 48 \text{ mA}$		0.2			0.2		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-70	-18		-70	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		9	15.5		9	15.5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		34	54		34	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 133 \Omega,$	$C_L = 45 \text{ pF}$		13	22	ns
t_{PHL}						8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS37, SN74LS37 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS37			SN74LS37			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1.2			-1.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS37			SN74LS37			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -1.2 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}$				0.35	0.5		V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-30		-130	-30		-130	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$			0.9			0.9	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$			6			12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 667 \Omega,$	$C_L = 45 \text{ pF}$	12		24	ns
t_{PHL}					12		24	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S37, SN74S37 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

	SN54S37			SN74S37			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-3			-3	mA
I_{OL} Low-level output current			60			60	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S37			SN74S37			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -3 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 60 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			0.1			0.1	mA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-4			-4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-50		-225	-50		-225	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		20	36		20	36	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5$		46	80		46	80	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 100 milliseconds.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 93 \Omega, C_L = 50 \text{ pF}$		4	6.5	ns
t_{PHL}					4	6.5	ns
t_{PLH}			$R_L = 93 \Omega, C_L = 150 \text{ pF}$		6		ns
t_{PHL}					6		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

QUADRUPEL 2-INPUT POSITIVE-NAND BUFFERS TYPES SN4523T, SN7423T

recommended operating conditions

PARAMETER	SN4523T	SN7423T
V _{CC} Supply voltage	4.5	4.5
V _{OH} High-level output voltage	2.0	2.0
V _{OL} Low-level output voltage	0.5	0.5
I _{OH} High-level output current	80	80
I _{OL} Low-level output current	120	120
T _A Operating free-air temperature	0	0

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN4523T	SN7423T
V _{IK}	V _{CC} = MIN, I _K = -10 mA	-1.2	-1.2
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -3 mA	2.0	2.0
V _{OL}	V _{CC} = MIN, V _{IH} = 3 V, I _{OL} = 80 mA	0.5	0.5
I _I	V _{CC} = MAX, V _I = 0.8 V	1	1
I _{ih}	V _{CC} = MAX, V _I = 3 V	0.1	0.1
I _{ic}	V _{CC} = MAX, V _I = 0.8 V	-4	-4
I _{is}	V _{CC} = MAX	-80	-80
I _{OH}	V _{CC} = MAX, V _I = 0 V	80	80
I _{OL}	V _{CC} = MAX, V _I = 4.5 V	120	120

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

2 All typical values are at V_{CC} = 5 V, T_A = 25°C.

3 For more than one output shown as forced at a time, add the current of the other output(s) to the forced output(s).

Switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX
t _{PLH}	A or B	Y	R _L = 83 Ω, C _L = 50 pF	4	8.5	10
t _{PHL}	A or B	Y	R _L = 83 Ω, C _L = 50 pF	4	8.5	10
t _{PLH}	A or B	Y	R _L = 83 Ω, C _L = 150 pF	8	15	20
t _{PHL}	A or B	Y	R _L = 83 Ω, C _L = 150 pF	8	15	20

NOTES: 1. See General Information section for load circuit and voltage waveform.

3 TTL DEVICES

REVISED DECEMBER 1983

- SN5438, SN54LS38, SN54S38 ... J OR W PACKAGE
SN7438 ... J OR N PACKAGE
SN74LS38, SN74S38 ... D, J OR N PACKAGE

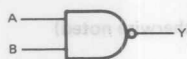
(TOP VIEW)

1A	1	14	VCC
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

SN54LS38, SN54S38 ... FK PACKAGE
SN74LS38, SN74S38

(TOP VIEW)

logic diagram (each gate)

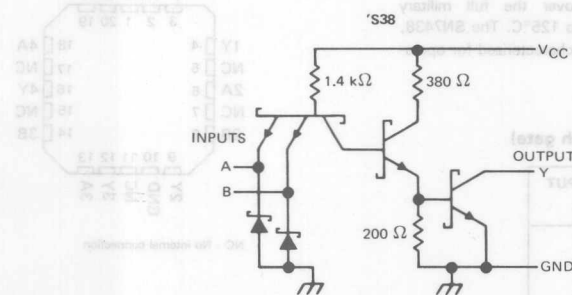
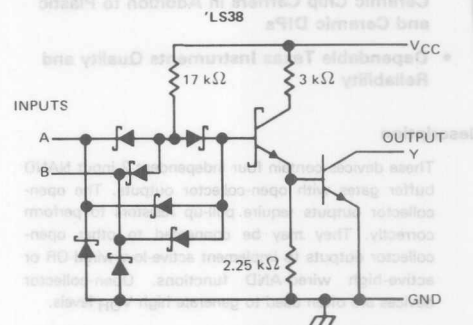
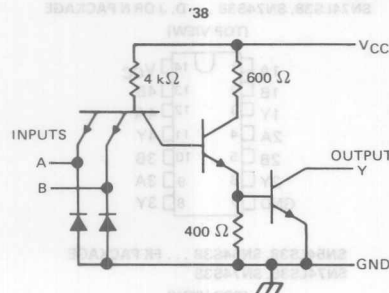

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

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TEXAS
INSTRUMENTS

**TYPES SN5438, SN54LS38, SN54S38,
SN7438, SN74LS38, SN74S38
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '38	5.5 V
LS38	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5438, SN7438 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	DESCRIPTION	SN5438			SN7438			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			48	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$			0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		5	8.5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		34	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 133 \Omega, C_L = 45 \text{ pF}$		14	22	ns
t_{PHL}					11	18	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS38, SN74LS38 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS38			SN74LS38			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS38			SN74LS38			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.25			0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$	0.25		0.4	0.25		0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}$				0.35		0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$	0.9		2	0.9		2	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	6		12	6		12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 667 \Omega, C_L = 45 \text{ pF}$		20	32	ns
t_{PHL}					18	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S38, SN74S38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54S38			SN74S38			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			60			60	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.2		V
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V		0.25		mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 60 mA		0.5		V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			0.1	mA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-4	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		20	36	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		46	80	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 93 Ω, C _L = 50 pF		6.5	10	ns
t _{PHL}					6.5	10	ns
t _{PLH}			R _L = 93 Ω, C _L = 150 pF		9		ns
t _{PHL}					8.5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.



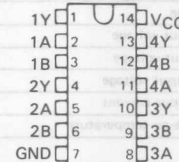
3
TTL DEVICES

TYPES SN5439, SN7439 QUADRUPLE 2-INPUT POSITIVE NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

REVISED MAY 1983

- Current Sinking Capability up to 80 mA
- Guaranteed Fan-Out of 30 Series 54/74 Loads
- Dependable Texas Instruments Quality and Reliability

SN5439 ... J PACKAGE
SN7439 ... J OR N PACKAGE
(TOP VIEW)



description

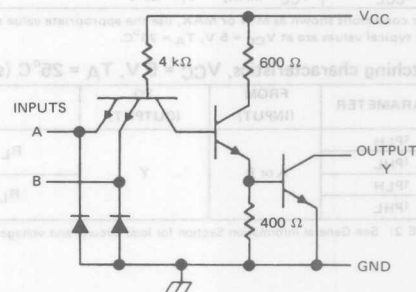
These devices contain four independent 2-input NAND buffers. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5439 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7439 is characterized for operation from 0°C to 70°C .

positive logic

$$Y = A \cdot B \text{ or } Y = \overline{A} + \overline{B}$$

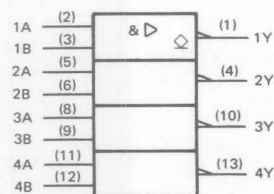
schematics (each gate)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol †



Pin numbers shown on logic notation are for J or N packages.

PRODUCTION DATA

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TEXAS
INSTRUMENTS

TYPES SN5439, SN7439 QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7V
Input voltage	7V
Off-state output voltage	7V
Operating free-air temperature range: SN5439	-55°C to 125°C
SN7439	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5439			SN7439			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output voltage			60			60	mA
							80†	
T_A	Operating free-air temperature	-55		125	0		70	°C

† The extended limit applies only if V_{CC} is maintained between 4.75 and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5439			SN7439			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
I_{OH}	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}$			-0.25			-0.25	mA
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 48 \text{ mA}$			0.4			0.4	V
	$V_{CC} = \text{MIN}, I_{OL} = 60 \text{ mA}$			0.5			0.5	
	$V_{CC} = 4.75 \text{ V}, I_{OL} = 80 \text{ mA}$						0.6	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$			54			54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5439		SN7439		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$R_L = 133 \Omega, C_L = 45 \text{ pF}$		22		22	ns
t_{PHL}					18		18	

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN5440, SN54LS40, SN54S40, SN7440, SN74LS40, SN74S40 DUAL 4-INPUT POSITIVE-NAND BUFFERS

REVISED APRIL 1985

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 4-input NAND buffer gates.

The SN5440, SN54LS40, and SN54S40 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7440, SN74LS40 and SN74S40 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (each gate)



positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D} \text{ or } Y = \overline{A + B + C + D}$$

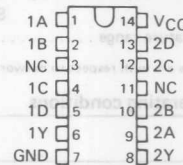
SN5440 ... J PACKAGE

SN54LS40, SN54S40 ... J OR W PACKAGE

SN7440 ... J OR N PACKAGE

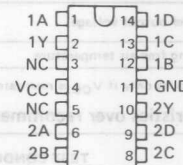
SN74LS40, SN74S40 ... D, J OR N PACKAGE

(TOP VIEW)



SN5440 ... W PACKAGE

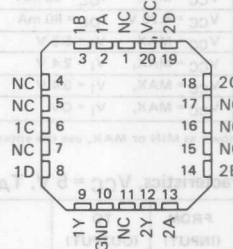
(TOP VIEW)



SN54LS40, SN54S40 ... FK PACKAGE

SN74LS40, SN74S40

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

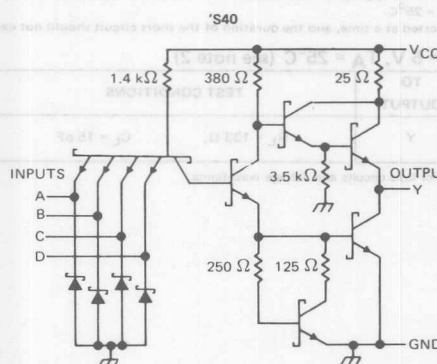
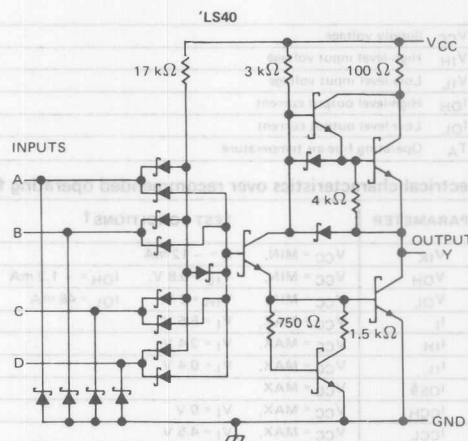
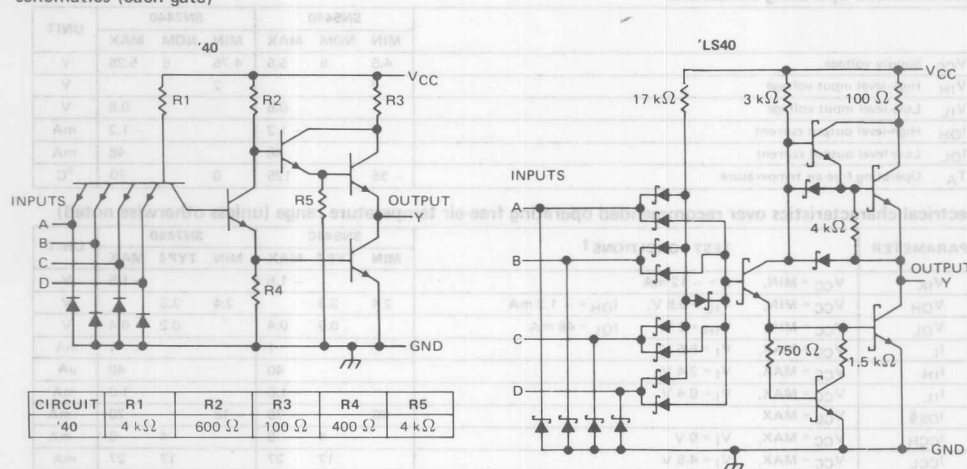
PRODUCTION DATA

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TEXAS
INSTRUMENTS

**TYPES SN5440, SN54LS40, SN54S40
SN7440, SN74LS40, SN74S40
DUAL 4-INPUT POSITIVE-NAND BUFFERS**

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '40, 'S40	5.5 V
'LS40	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5440, SN7440 DUAL 4-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

	SN5440			SN7440			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-1.2			-1.2	mA
I_{OL} Low-level output current			48			48	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5440			SN7440			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN.}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN.}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -1.2 \text{ mA}$	2.4	3.3		2.4	3.3		V
V_{OL}	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 48 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX.}$, $V_I = 5.5 \text{ V}$			1			-1	mA
I_{IH}	$V_{CC} = \text{MAX.}$, $V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX.}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX.}$	-20		-70	-18		-70	mA
I_{CCH}	$V_{CC} = \text{MAX.}$, $V_I = 0 \text{ V}$		4	8		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX.}$, $V_I = 4.5 \text{ V}$		17	27		17	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 100 milliseconds.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 133 \Omega$, $C_L = 15 \text{ pF}$		13	22	ns
t_{PHL}					8	15	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS40, SN74LS40 DUAL 4-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

		SN54LS40			SN74LS40			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-1.2			-1.2	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS40			SN74LS40			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -1.2 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 12 mA	0.25	0.4		0.25	0.4		V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 24 mA				0.35	0.5		V
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS} §	V _{CC} = MAX	-30		-130	-30		-130	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V	0.45		1	0.45		1	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V	3		6	3		6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 667 Ω, C _L = 45 pF		12	24	ns
t _{PHL}					12	24	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S40, SN74S40 DUAL 4-INPUT POSITIVE-NAND BUFFERS

recommended operating conditions

		SN54S40			SN74S40			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-3			-3	mA
I _{OL}	Low-level output current			60			60	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54S40			SN74S40			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN.	I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN.	V _{IL} = 0.8 V, I _{OH} = -3 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN.	V _{IH} = 2 V, I _{OL} = 60 mA			0.5			0.5	V
I _I	V _{CC} = MAX.	V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX.	V _I = 2.7 V			0.1			0.1	mA
I _{IL}	V _{CC} = MAX.	V _I = 0.5 V			-4			-4	mA
I _{OS} §	V _{CC} = MAX.		-50		-225	-50		-225	mA
I _{CCH}	V _{CC} = MAX.	V _I = 0 V		10	18		10	18	mA
I _{CCL}	V _{CC} = MAX.	V _I = 4.5 V		25	44		25	44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 100 milliseconds.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 93 Ω,	C _L = 50 pF		4	6.5	ns
t _{PHL}						4	6.5	ns
t _{PLH}			R _L = 93 Ω,	C _L = 150 pF		6		ns
t _{PHL}						6		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

SN5442A, SN54LS42, SN7442A, SN74LS42
4-LINE TO 10-LINE DECODERS (1-OF-10)

MARCH 1974 — REVISED APRIL 1985

'42A, 'LS42 ... BCD-TO-DECIMAL
EXCESS-3-TO-DECIMAL
GRAY-TO-DECIMAL

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
4-Line-to-16-Line Decoders
3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A	140 mW	17 ns
'LS42	35 mW	17 ns

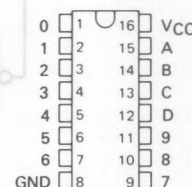
description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, and 'LS42 BCD-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

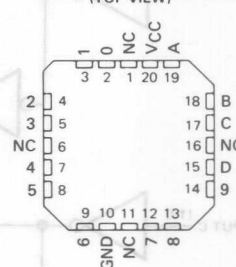
Series 54, and 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74, and 74LS circuits are characterized for operation from 0°C to 70°C .

SN5442A, SN54LS42 ... J OR W PACKAGE
SN7442A ... J OR N PACKAGE
SN74LS42 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS42 ... FK PACKAGE
SN74LS42

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

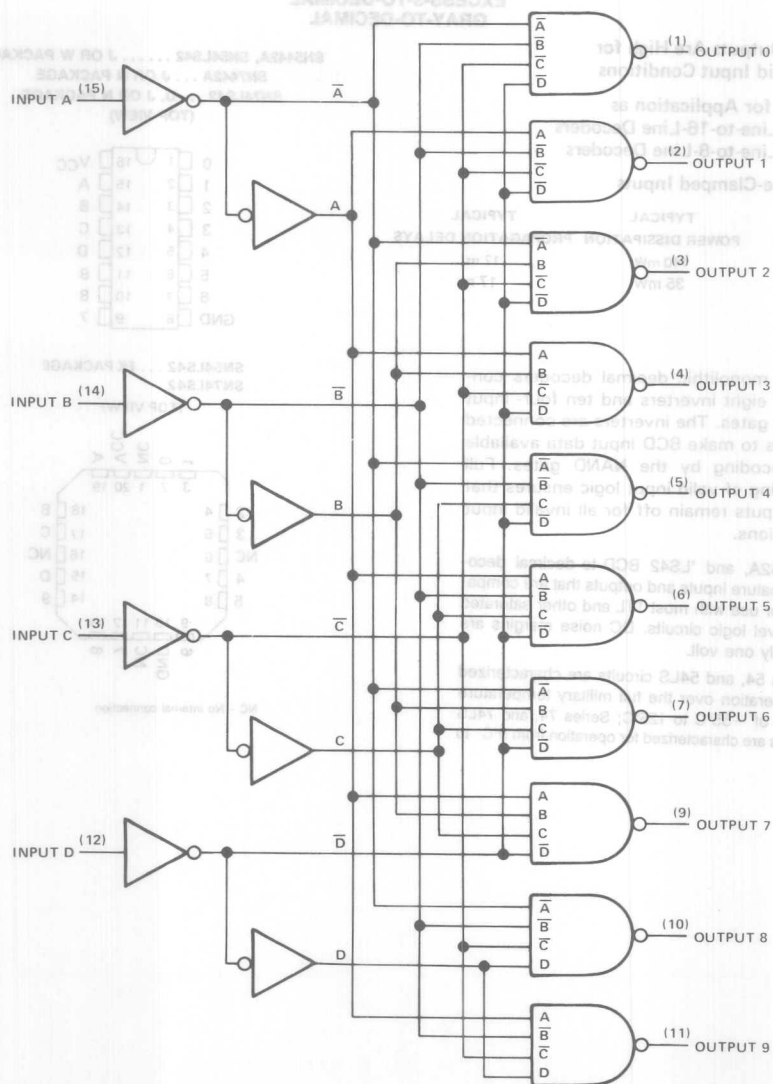
PRODUCTION DATA

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TEXAS
INSTRUMENTS

TYPES SN5442A, SN54LS42, SN7442A, SN74LS42
4-LINE TO 10-LINE DECODERS (1-OF-10)

logic diagrams



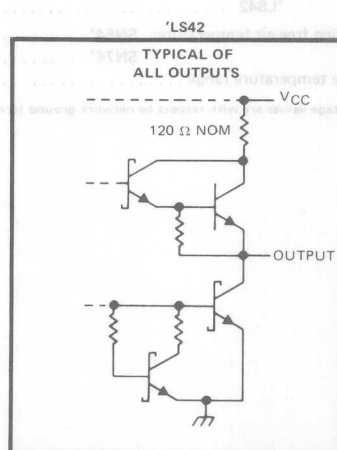
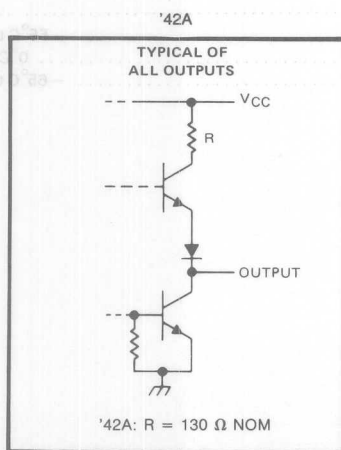
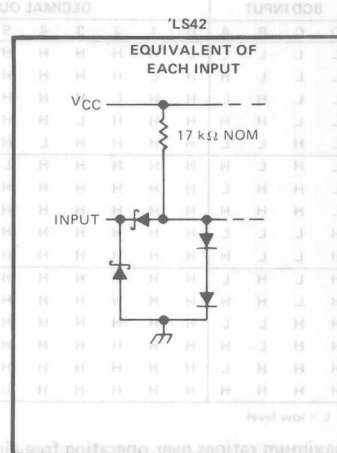
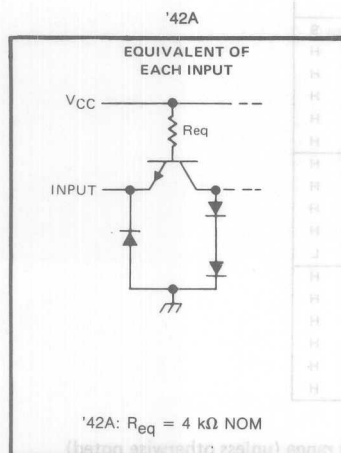
Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

TYPES SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE TO 10-LINE DECODERS (1-OF-10)

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN5442A, SN54LS42, SN7442A, SN74LS42
4-LINE TO 10-LINE DECODERS (1-OF-10)

FUNCTION TABLE

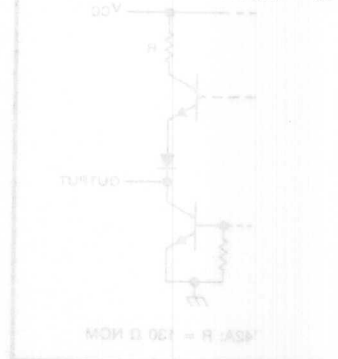
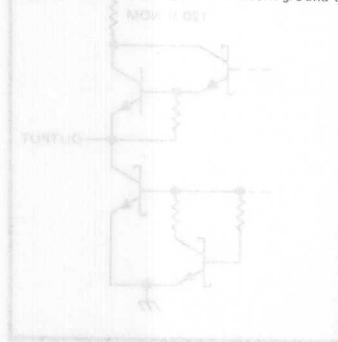
NO.	'42A, 'LS42 BCD INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	H	H	H	H
5	L	H	L	H	L	H	H	H	H	L	H	H	H	H
6	L	H	H	L	L	H	H	H	H	H	L	H	H	H
7	L	H	H	H	L	H	H	H	H	H	H	L	H	H
8	H	L	L	L	L	H	H	H	H	H	H	H	L	H
9	H	L	L	H	L	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	L	H	H	H	H	H	H	H	H	H
	H	L	H	H	L	H	H	H	H	H	H	H	H	H
	H	H	L	L	L	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	H	H	H	H	H	H	H	H	H

H = high level, L = low level

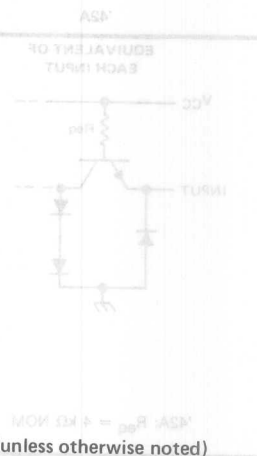
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '42A	5.5 V
'LS42	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



schematic of inputs and outputs



3

TTL DEVICES

TYPES SN5442A, SN7442A
4-LINE TO 10-LINE DECODERS (1-OF-10)

recommended operating conditions

	SN5442A			SN7442A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN5442A			SN7442A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-55		-18	-55		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		28	41		28	56	mA

[†]For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Note 3}$	14		25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic		17		30	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic		10		25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic		17		30	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

recommended operating conditions

PARAMETER	SN54LS42			SN74LS42			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55	125		0	70		$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS42			SN74LS42			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 4 \text{ mA}$ $V_{IL} = V_{IL} \text{ max}$, $I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	7	13		7	13		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.
[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
 NOTE 2: I_{CC} is measured with all outputs open and inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic			15	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$		20	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic	See Note 3		15	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			20	30	ns

Note 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5445, SN7445 BCD-TO-DECIMAL DECODERS/DRIVERS

DECEMBER 1972—REVISED DECEMBER 1983

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

logic

FUNCTION TABLE														
NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	H	L	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	L	H	H	H	H	H	H
5	L	H	L	H	L	H	H	L	H	H	H	H	H	H
6	L	H	H	L	L	H	H	L	H	H	H	H	H	H
7	L	H	H	H	L	H	H	L	H	H	H	L	H	H
8	H	L	L	L	L	H	H	L	H	H	H	L	H	H
9	H	L	L	H	L	H	H	L	H	H	H	H	L	H
INVALID	H	L	H	L	L	H	H	L	H	H	H	H	H	H
	H	L	H	H	L	H	H	L	H	H	H	H	H	H
	H	H	L	L	L	H	H	L	H	H	H	H	H	H
	H	H	L	H	L	H	H	L	H	H	H	H	H	H
	H	H	H	L	L	H	H	L	H	H	H	H	H	H

H = high level (off), L = low level (on)

description

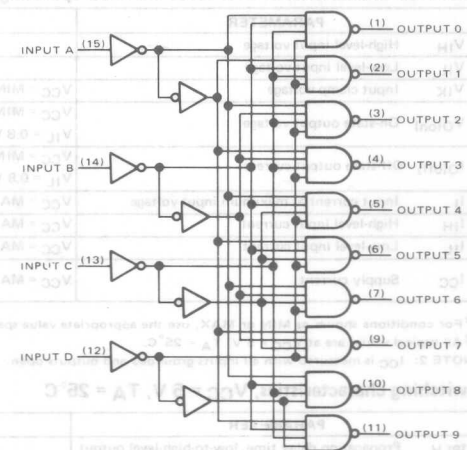
These monolithic BCD-to-decimal decoders/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

SN5445 ... J OR W PACKAGE
SN7445 ... J OR N PACKAGE

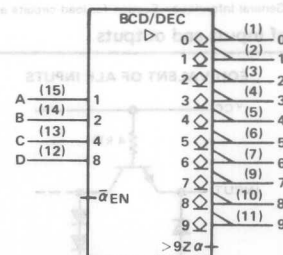
(TOP VIEW)



logic diagram



logic symbol



Pin numbers shown in logic notation are for J or N packages.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN5445, SN7445 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Maximum current into any output (off-state)	1 mA
Operating free-air temperature range: SN5445 Circuits	-55°C to 125°C
SN7445 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5445			SN7445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			30			30	V
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$		$I_{O(on)} = 80 \text{ mA}$ $I_{O(on)} = 20 \text{ mA}$	0.5 0.9	V
$I_{O(off)}$ Off-state output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{O(off)} = 30 \text{ V}$			250	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	SN5445 SN7445	43 43	62 70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

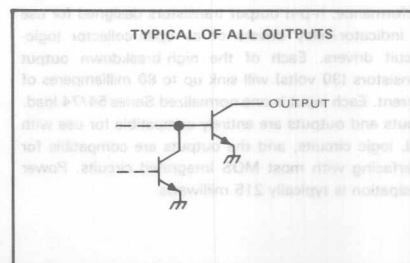
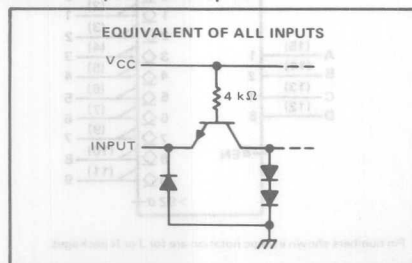
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 100 \Omega, \text{ See Note 3}$			50	ns
t_{PHL} Propagation delay time, high-to-low-level output				50	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



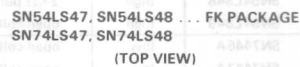
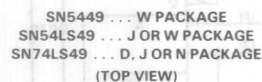
3

TTL DEVICES

MARCH 1974, REVISED DECEMBER 1983

**'49, 'LS49
feature**

- SN5446A, SN5447A, SN54LS47, SN5448,
SN54LS48 ... J OR W PACKAGE
SN7446A, SN7447A,
SN7448 ... J OR N PACKAGE
SN74LS47, SN74LS48 ... D, J OR N PACKAGE



TEXAS
INSTRUMENTS

**TYPES SN5446A, '47A, '48, '49, SN54LS47, 'LS48, 'LS49,
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

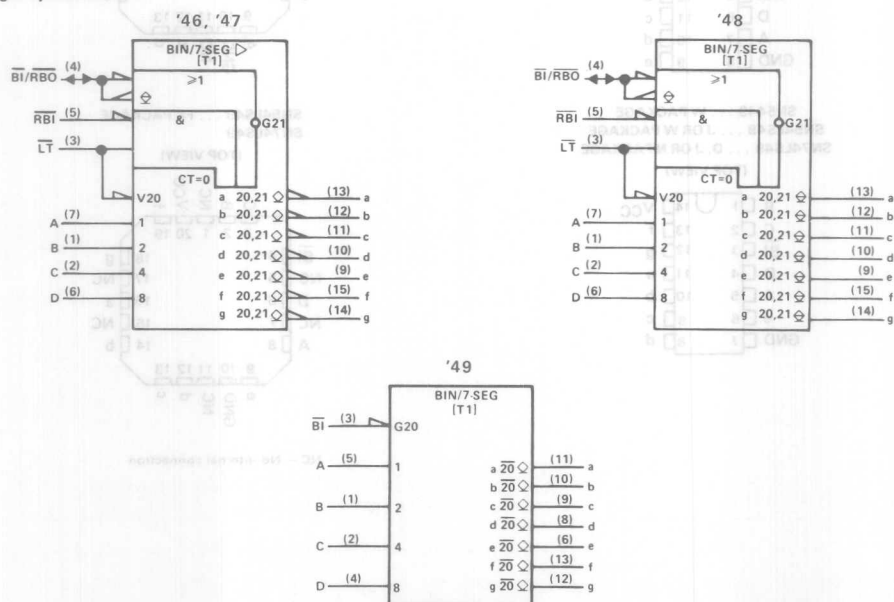
- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	ACTIVE LEVEL	DRIVER OUTPUTS			TYPICAL POWER DISSIPATION	PACKAGES
		OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, W
SN5449	high	open-collector	10 mA	5.5 V	165 mW	W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-k Ω pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-k Ω pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-k Ω pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols

3

TTL DEVICES



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN5446A, '47A, '48, '49, SN54LS47, 'LS48, 'LS49, SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

description

The '46A, '47A, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or common-cathode VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a lamp test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the $\overline{\text{BI}}/\text{RBO}$ node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ($\overline{\text{BI}}$) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the \square and the \square with tails and have been designed to offer the designer a choice between two indicator fonts. The SN54249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the '249 circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is not available in the '49 or 'LS49 circuit.



SEGMENT
IDENTIFICATION

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						$\overline{\text{BI}}/\text{RBO}^\dagger$	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are off regardless of the level of any other input.

3. When ripple blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output ($\overline{\text{BI}}/\text{RBO}$) is open or held high and a low is applied to the lamp test input, all segment outputs are on.

$^\dagger \overline{\text{BI}}/\text{RBO}$ is wire AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple blanking output (RBO).

**TYPES SN5446A, '47A, '48, '49, SN54LS47, 'LS48, 'LS49,
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

**'48, 'LS48
FUNCTION TABLE**

DECIMAL OR FUNCTION	INPUTS					$\overline{\text{BI}}/\text{RBO}^\dagger$	OUTPUTS							NOTE
	LT	RBI	D	C	B	A	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	L	H	L	L	H	
3	H	X	L	L	H	H	H	H	L	L	L	L	H	
4	H	X	L	H	L	L	H	L	H	L	L	H	H	
5	H	X	L	H	L	H	H	L	H	L	H	L	H	
6	H	X	L	H	H	L	H	L	L	H	H	L	H	
7	H	X	L	H	H	H	H	L	L	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	L	L	L	H	L	L	H	
11	H	X	H	L	H	H	L	L	H	L	L	L	L	
12	H	X	H	H	L	L	L	H	L	L	L	L	H	
13	H	X	H	H	L	H	H	L	L	L	L	H	H	
14	H	X	H	H	H	L	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high, if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are low regardless of the level of any other input.

3. When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a low level (response condition).

4. When the blanking input/ripple-blanking output ($\overline{\text{BI}}/\text{RBO}$) is open or held high and a low is applied to the lamp test input, all segment outputs are high.

$\dagger \overline{\text{BI}}/\text{RBO}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$).

**'49, 'LS49
FUNCTION TABLE**

DECIMAL OR FUNCTION	INPUTS					$\overline{\text{BI}}$	OUTPUTS							NOTE
	D	C	B	A			a	b	c	d	e	f	g	
0	L	L	L	L		H	H	H	H	H	H	H	L	1
1	L	L	L	H		H	L	H	H	L	L	L	L	
2	L	L	L	H		H	H	L	H	L	L	L	H	
3	L	L	L	H		H	H	H	L	L	L	L	H	
4	L	L	L	L		H	L	H	H	L	L	H	H	
5	L	L	L	H		H	H	L	H	L	L	H	H	
6	L	L	L	H		H	L	L	H	L	L	H	H	
7	L	L	L	H		H	H	H	L	L	L	L	L	
8	L	L	L	L		H	H	H	H	L	L	H	H	
9	L	L	L	H		H	H	H	L	L	L	H	H	
10	L	L	L	L		H	L	L	L	H	L	L	H	
11	L	L	L	H		H	L	L	H	L	L	L	H	
12	L	L	L	L		H	L	L	L	L	L	L	H	
13	L	L	L	H		H	L	L	L	L	L	L	H	
14	L	L	L	L		H	L	L	L	L	L	L	L	
15	L	L	L	H		H	L	L	L	L	L	L	L	
BI	X	X	X	X		L	L	L	L	L	L	L	L	2

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired.

2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are low regardless of the level of any other input.

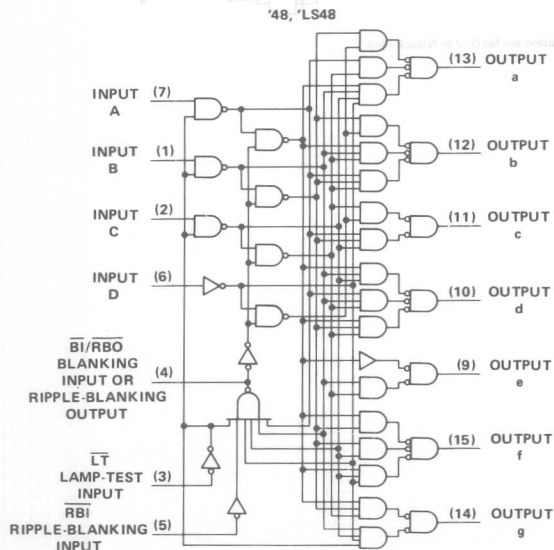
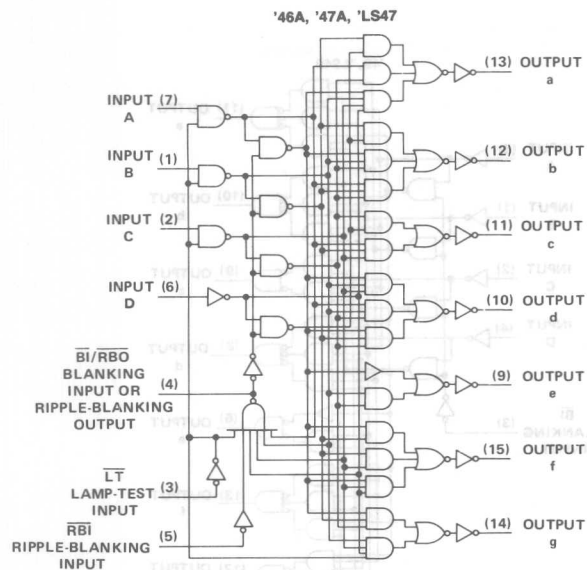
3

TTL DEVICES

TYPES SN5446A, '47A, '48, SN54LS47, 'LS48,
SN7446A, '47A, '48, SN74LS47, 'LS48
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

logic diagrams

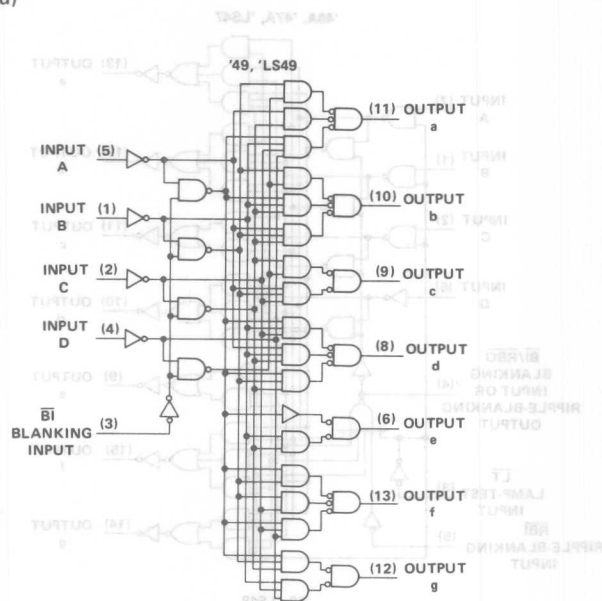
(continued) logic diagrams



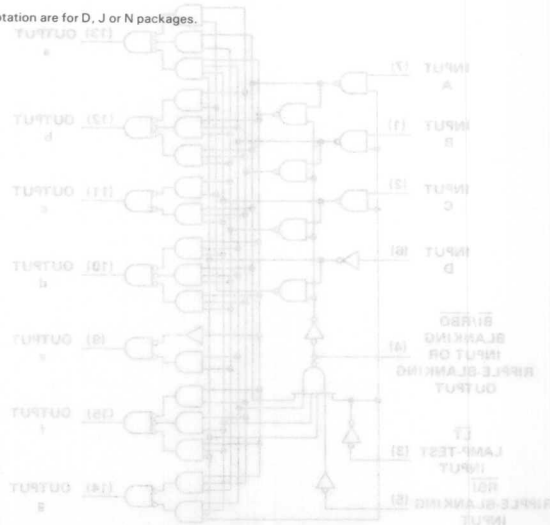
Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN5449, SN54LS49, SN74LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

logic diagrams (continued)



Pin numbers shown on logic notation are for D, J or N packages.



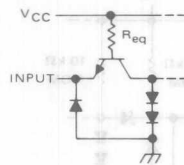
3 TTL DEVICES

TYPES SN5446A, '47A, '48, '49
SN7446A, '47A, '48
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

'46A, '47A, '48, '49

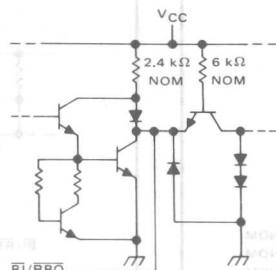
EQUIVALENT OF EACH INPUT
EXCEPT BI/RBO



SN54/SN74: $R_{eq} = 6 \text{ k}\Omega \text{ NOM}$
SN54L/SN74L: $R_{eq} = 8 \text{ k}\Omega \text{ NOM}$

'46A, '47A, '48

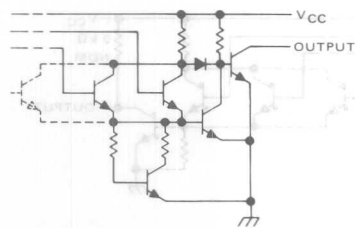
EQUIVALENT OF BI/RBO



BI/RBO

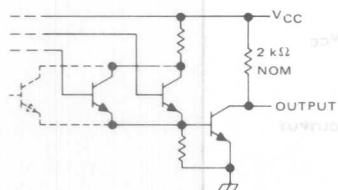
'46A, '47A

TYPICAL OF OUTPUTS
a THRU g



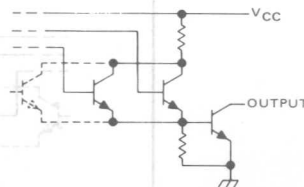
'48

TYPICAL OF OUTPUTS
a THRU g



'49

TYPICAL OF ALL OUTPUTS



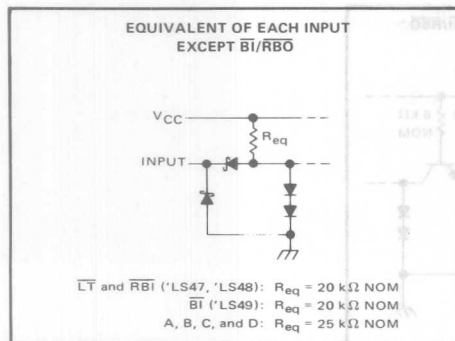
3

TTL DEVICES

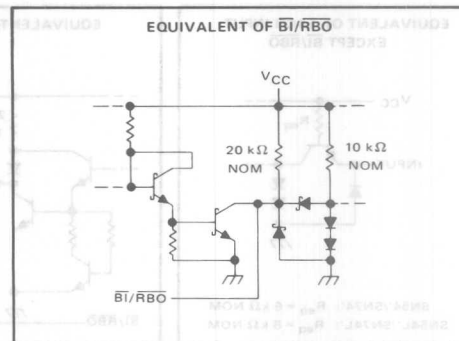
TYPES SN54LS47, 'LS48, 'LS49, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

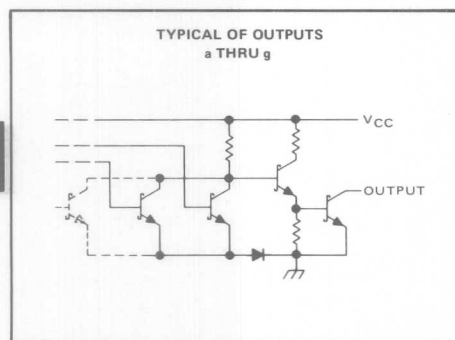
'LS47, 'LS48, 'LS49



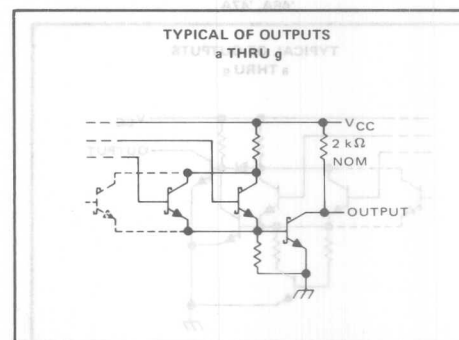
'LS47, 'LS48, 'LS49



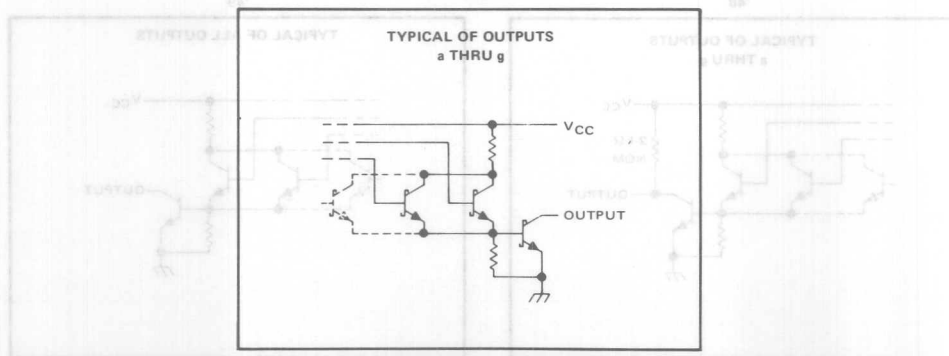
'LS47



'LS48



'LS49



3
TTL DEVICES

TYPES SN5446A, SN5447A, SN7446A, SN7447A BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN5446A, SN5447A	-55°C to 125°C
SN7446A, SN7447A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	$\bar{B}/\bar{R}\bar{B}\bar{O}$			-200			-200			-200			-200	μ A
Low-level output current, I_{OL}	$\bar{B}/\bar{R}\bar{B}\bar{O}$			8			8			8			8	mA
Operating free-air temperature, T_A		-55		125	-55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -200 \mu\text{A}$	$\bar{B}/\bar{R}\bar{B}\bar{O}$	2.4	3.7		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$	$\bar{B}/\bar{R}\bar{B}\bar{O}$		0.27	0.4	V
$I_{O(off)}$	Off-state output current	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{O(off)} = \text{MAX}$	a thru g			250	μ A
$V_{O(on)}$	On-state output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{O(on)} = 40 \text{ mA}$	a thru g		0.3	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	Any input except $\bar{B}/\bar{R}\bar{B}\bar{O}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	Any input except $\bar{B}/\bar{R}\bar{B}\bar{O}$			40	μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	Any input except $\bar{B}/\bar{R}\bar{B}\bar{O}$			-1.6	mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	$\bar{B}/\bar{R}\bar{B}\bar{O}$			-4	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2					
						64	85
						64	103

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input					100	ns
t_{on}	Turn-on time from A input	$C_L = 15 \text{ pF}, R_L = 120 \Omega,$				100	ns
t_{off}	Turn-off time from $\bar{R}\bar{B}\bar{I}$ input	See Note 3				100	ns
t_{on}	Turn-on time from $\bar{R}\bar{B}\bar{I}$ input					100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms. t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL} .

TYPES SN54LS47, SN74LS47 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS47	-55°C to 125°C
SN74LS47	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS47			SN74LS47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(\text{off})}$	a thru g			15			15	V
On-state output current, $I_{O(\text{on})}$	a thru g			12			24	mA
High-level output current, I_{OH}	$\overline{BI}/\overline{RBO}$			-50			-50	μA
Low-level output current, I_{OL}	$\overline{BI}/\overline{RBO}$			1.6			3.2	mA
Operating free-air temperature, T_A		-55		125	0		70	$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		SN54LS47			SN74LS47			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18$ mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MIN}, V_{IH} = 2$ V, $V_{IL} = V_{IL \text{ max}}, I_{OH} = -50$ μA		2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MIN}, I_{OH} = 2$ V, $V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6$ mA			0.25	0.4		0.25	0.4	V
		$I_{OL} = 3.2$ mA						0.35	0.5	
$I_{O(\text{off})}$	Off-state output current	a thru g $V_{CC} = \text{MAX}, V_{IH} = 2$ V, $V_{IL} = V_{IL \text{ max}}, V_{O(\text{off})} = 15$ V				250			250	μA
$V_{O(\text{on})}$	On-state output voltage	a thru g $V_{CC} = \text{MIN}, I_{O(\text{on})} = 12$ mA $V_{IH} = 2$ V, $V_{IL} = V_{IL \text{ max}}, I_{O(\text{on})} = 24$ mA			0.25	0.4		0.25	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7$ V				0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7$ V				20			20	μA
I_{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 0.4$ V				-0.4			-0.4	mA
		$\overline{BI}/\overline{RBO}$				-1.2			-1.2	
I_{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}$		-0.3		-2	-0.3		-2	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2		7	13		7	13		mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS [†]	MIN	TYP	MAX	UNIT
t_{off} Turn-off time from A input				100	ns
t_{on} Turn-on time from A input	$C_L = 15$ pF, $R_L = 665$ Ω			100	ns
t_{off} Turn-off time from \overline{RBI} input	See Note 3			100	ns
t_{on} Turn-on time from \overline{RBI} input				100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5448, SN7448 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5448	-55°C to 125°C
SN7448	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5448			SN7448			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			-400			-400	μ A
	$\overline{BI}/\overline{RBO}$			-200			-200	μ A
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	$\overline{BI}/\overline{RBO}$			8			8	mA
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	a thru g $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	4.2		V
		$\overline{BI}/\overline{RBO}$	2.4	3.7		V
I_O	Output current	a thru g $V_{CC} = \text{MIN}, V_O = 0.85 \text{ V},$ Input conditions as for V_{OH}	-1.3	-2		mA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$		0.27	0.4	V
I_I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μ A
I_{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
		$\overline{BI}/\overline{RBO}$			-4	mA
I_{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}$			-4	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2				mA
		SN5448		53	76	
		SN7448		53	90	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}; R_L = 1 \text{ k}\Omega,$ See Note 3			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	ns
t_{PHL}	Propagation delay time, high-to-low-level output from \overline{RBI} input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from \overline{RBI} input				100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS48, SN74LS48 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS48	-55°C to 125°C
SN74LS48	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS48			SN74LS48			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			-100			-100	μ A
	$\overline{BI}/\overline{RBO}$			-50			-50	
Low-level output current, I_{OL}	a thru g			2			6	mA
	$\overline{BI}/\overline{RBO}$			1.6			3.2	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS48			SN74LS48			UNIT		
				MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IH}	High-level input voltage			2			2			V		
V _{IL}	Low-level input voltage						0.7			V		
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = −18 mA	−1.5			−1.5			V		
V _{OH}	High-level output voltage	a thru g and $\overline{BI}/\overline{RBO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	4.2		2.4	4.2		V		
I _O	Output current	a thru g	V _{CC} = MIN, V _O = 0.85 V, Input conditions as for V _{OH}	−1.3	−2		−1.3	−2		mA		
V _{OL}	Low-level output voltage	a thru g	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max			0.25	0.4			0.25	0.4	V
				I _{OL} = 2 mA								
		$\overline{BI}/\overline{RBO}$		I _{OL} = 6 mA							0.35	0.5
			V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max			0.25	0.4			0.25	0.4	V
I _I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA		
I _{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 2.7 V			20			20	μA		
I _{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$	V _{CC} = MAX, V _I = 0.4 V			−0.4			−0.4	mA		
		$\overline{BI}/\overline{RBO}$				−1.2			−1.2			
I _{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$	V _{CC} = MAX	−0.3	−2	−0.3	−2			mA		
I _{CC}	Supply current		V _{CC} = MAX, See Note 2	25	38	25	38			mA		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 4 \text{ k}\Omega,$			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input	See Note 3			100	
t_{PHL}	Propagation delay time, high-to-low-level output from \overline{RBI} input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega,$			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from \overline{RBI} input	See Note 3			100	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN5449 BCD-TO-SEVEN-SEGMENT DECODER/DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5449			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			10	mA
Operating free-air temperature, T_A	-55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5449			UNIT
		MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.6	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -10 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 10 \text{ mA}$	0.27	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		33	47	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 667 \Omega,$ See Note 3			100	ns
t_{PLH} Propagation delay time, low-to-high-level output from A input				100	ns
t_{PHL} Propagation delay time, high-to-low-level output from RB1 input				100	ns
t_{PLH} Propagation delay time, low-to-high-level output from RB1 input				100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS49, SN74LS49 BCD-TO-SEVEN-SEGMENT-DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS49	-55°C to 125°C
SN74LS49	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS49			SN74LS49			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS49			SN74LS49			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			250			250	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$			0.25			0.35	V
	$I_{OL} = 4 \text{ mA}$		0.4			0.4		
	$I_{OL} = 8 \text{ mA}$						0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	8		15	8		15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$			100	ns
t_{PLH} Propagation delay time, low-to-high-level output from A input	See Note 3			100	ns
t_{PHL} Propagation delay time, high-to-low-level output from $R\bar{B}1$ input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega$			100	ns
t_{PLH} Propagation delay time, low-to-high-level output from $R\bar{B}1$ input	See Note 3			100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5450, SN7450

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

REVISED DECEMBER 1983

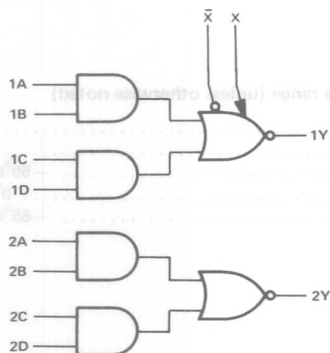
- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

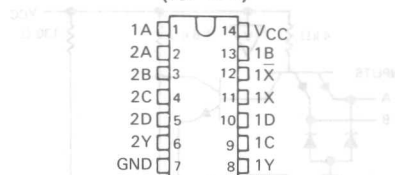
These devices contain two independent 2-wide 2-input AND-OR-INVERT gates with one gate expandable. They perform the Boolean function $Y = \overline{AB + CD + X}$ with X = output of SN5460/SN7460 for the SN5450/SN7450.

The SN5450 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7450 is characterized for operation from 0°C to 70°C .

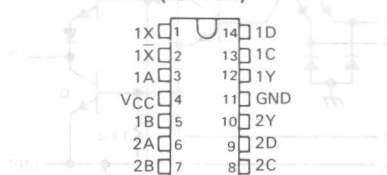
logic diagram



SN5450 ... J PACKAGE
SN7450 ... J OR N PACKAGE
(TOP VIEW)



SN5450 ... W PACKAGE
(TOP VIEW)



3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

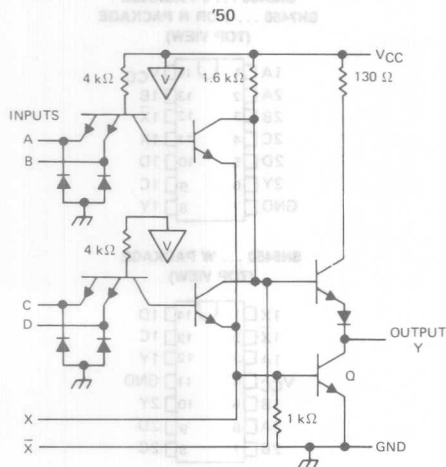
TEXAS
INSTRUMENTS

3-179

TYPES SN5450, SN7450

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

schematic



Resistor values shown are nominal.
If expander is not used, leave X and \bar{X} open.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3 TTL DEVICES

TYPES SN5450, SN7450 DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

recommended operating conditions

		SN5450			SN7450			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5450			SN7450			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4	8		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{See Note 2}$		7.4	14		7.4	14	mA
$I_{\bar{X}}^{\Delta}$	$V_{\bar{X}X} = 0.4 \text{ V}, I_{OL} = 16 \text{ mA}$			-2.9			-3.1	mA
$V_{BE(O)}^{\Delta}$	$I_X + I_{\bar{X}} = 0.41 \text{ mA}, R_{\bar{X}X} = 0, I_{OL} = 16 \text{ mA}$			1.1				V
	$I_X + I_{\bar{X}} = 0.62 \text{ mA}, R_{\bar{X}X} = 0, I_{OL} = 16 \text{ mA}$						1	
V_{OH}^{Δ}	$I_X = 0.15 \text{ mA}, I_{\bar{X}} = -0.15 \text{ mA}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4					V
	$I_X = 0.27 \text{ mA}, I_{\bar{X}} = -0.27 \text{ mA}, I_{OH} = -0.4 \text{ mA}$				2.4	3.4		
V_{OL}^{Δ}	$I_X + I_{\bar{X}} = 0.3 \text{ mA}, R_{\bar{X}X} = 138 \Omega, I_{OL} = 16 \text{ mA}$	0.2	0.4					V
	$I_X + I_{\bar{X}} = 0.43 \text{ mA}, R_{\bar{X}X} = 130 \Omega, I_{OL} = 16 \text{ mA}$				0.2	0.4		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

Δ Using expander inputs, $V_{CC} = \text{MIN}, T_A = \text{MIN}$, except typical values.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$ Expander pins open		13	22	ns
t_{PHL}					8	15	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN5450		SN7450	
		MIN	MAX	MIN	MAX
V_{CC} supply voltage		4.5	5	4.5	5
V_{IH} high-level input voltage		3		3	
V_{IL} low-level input voltage			0.8		0.8
I_{IH} high-level input current			-0.4		-0.4
I_{OH} high-level output current			16		16
I_{OL} low-level output current			1.5		0
T_A operating free-air temperature		-55		-55	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5450		SN7450	
		MIN	MAX	MIN	MAX
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -1.5 \text{ mA}$		1.5		1.5
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	2.4	2.4	2.4	2.4
V_{OL}	$V_{CC} = \text{MIN}$, $V_I = 3 \text{ V}$, $I_{OL} = 16 \text{ mA}$	0.3	0.4	0.3	0.4
I_I	$V_{CC} = \text{MAX}$, $V_I = 3 \text{ V}$		1		1
I_{IH}	$V_{CC} = \text{MAX}$, $V_{IH} = 3 \text{ V}$		40		40
I_{IL}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.8 \text{ V}$		-1.5		-1.5
I_{OZ}	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		5		5
I_{OCH}	$V_{CC} = \text{MAX}$, See Note 2		1.4		1.4
I_{OCL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$		1.5		1.5
I_X	$V_{CC} = 0.4 \text{ V}$, $I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^a	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^b	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^c	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^d	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^e	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^f	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^g	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^h	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^i	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^j	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^k	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^l	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^m	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^n	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^o	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^p	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^q	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^r	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^s	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^t	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^u	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^v	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^w	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^x	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^y	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1
I_{ZSD}^z	$I_X + I_Z = 0.4 \text{ mA}$, $I_{OL} = 16 \text{ mA}$		1.1		1.1

1. Test conditions shown as MIN or MAX, not in a square value specified under recommended operating conditions.
2. All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
3. Low-level input voltage should be limited to 0.8 V .
4. Low-level output current should be limited to 16 mA .
5. Input current I_I is MIN. Input current I_{IH} is MAX.
6. Input current I_{IL} is MIN. Input current I_{OL} is MAX.
7. All inputs of one AND gate of 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	1	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$		13	22	ns
t_{FALL}	Any	0	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$		8	10	ns

NOTE 3: See device information section for load circuit and voltage waveform.

3 TTL DEVICES

TYPES SN5451, SN54LS51, SN54S51, SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

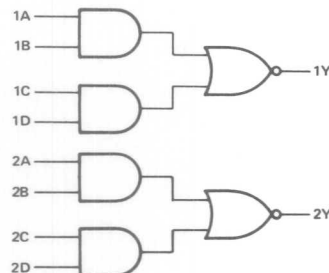
The '51, and 'S51 contain two independent 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean function $Y = AB + CD$.

The 'LS51 contains one 2-wide 3-input and one 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean functions $1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$ and $2Y = (2A \cdot 2B) + (2C \cdot 2D)$.

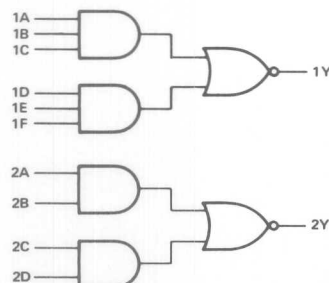
The SN5451, SN54LS51 and SN54S51 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7451, SN74LS51 and SN74S51 are characterized for operation from 0°C to 70°C .

logic diagrams

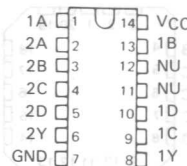
'51, 'S51



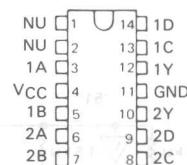
'LS51, 'LS51



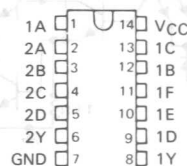
SN5451 ... J PACKAGE
SN54LS51 ... J OR W PACKAGE
SN7451 ... J OR N PACKAGE
SN74S51 ... D, J OR N PACKAGE
(TOP VIEW)



SN5451 ... W PACKAGE
(TOP VIEW)



SN54LS51 ... J OR W PACKAGE
SN74LS51 ... D, J OR N PACKAGE
(TOP VIEW)



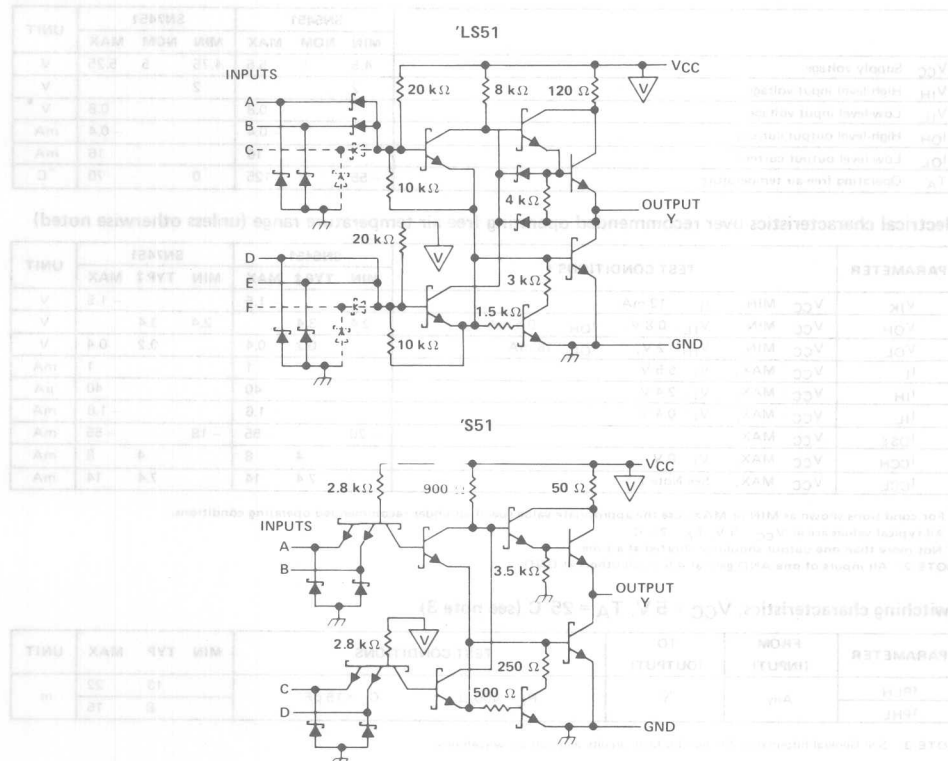
NC - No internal connection
NU - Make no external connection

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

**TYPES SN5451, SN54LS51, SN54S51,
SN7451, SN74LS51, SN74S51
AND-OR-INVERT GATES**

schematics



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '51, 'LS51, 'S51	7 V
Input voltage: '51, 'S51	5.5 V
'LS51	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5451, SN7451 AND-OR-INVERT GATES

recommended operating conditions

	SN5451			SN7451			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5451			SN7451			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} MIN, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} MAX, V _I = 2.4 V			40			40	μA
I _{IL}	V _{CC} MAX, V _I = 0.4 V			-1.6			-1.6	mA
I _{OS} §	V _{CC} MAX	-20		-55	-18		-55	mA
I _{CCH}	V _{CC} MAX, V _I = 0 V		4	8		4	8	mA
I _{CCL}	V _{CC} MAX, See Note 2		7.4	14		7.4	14	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 400 Ω, C _L = 15 pF	13	22		ns
t _{PHL}				8	15		

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS51, SN74LS51 AND-OR-INVERT GATES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS51			SN74LS51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage		0.7			0.8		V
I_{OH}	High-level output current		-0.4			-0.4		mA
I_{OL}	Low-level output current		4			8		mA
T_A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †		SN54LS51			SN74LS51			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5		V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = -0.4 \text{ mA}$		2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 8 \text{ mA}$					0.35	0.5		V
I_I	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1		mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20		µA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4		mA
$I_{OS} §$	$V_{CC} = \text{MAX}$		-20	-100		-20	-100		mA
I_{CCH}	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		0.8	1.6		0.8	1.6		mA
I_{CCL}	$V_{CC} = \text{MAX}$, See Note 2		1.4	2.8		1.4	2.8		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega$, $C_L = 15 \text{ pF}$		12	20	ns
t_{PHL}					12.5	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S51, SN74S51 AND-OR-INVERT GATES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54S51			SN74S51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S51			SN74S51			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		8.2	17.8		8.2	17.8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		13.6	22		13.6	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		3.5	5.5	ns
t_{PHL}					3.5	5.5	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		5		ns
t_{PHL}					5.5		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN5453, SN7453 EXPANDABLE 4-WIDE AND-OR-INVERT GATES

REVISED DECEMBER 1983

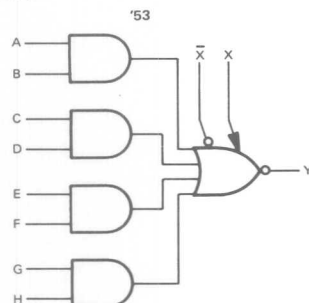
- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

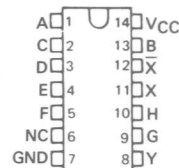
These devices contain expandable 4-wide AND-OR-INVERT gates. The '53 perform the Boolean function $Y = \overline{AB + CD + EF + GH + X}$ = output of SN5460/SN7460.

The SN5453 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7453 is characterized for operation from 0°C to 70°C .

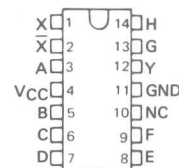
logic diagram



SN5453 ... J PACKAGE
SN7453 ... J OR N PACKAGE
(TOP VIEW)



SN5453 ... W PACKAGE
(TOP VIEW)



3

TTL DEVICES

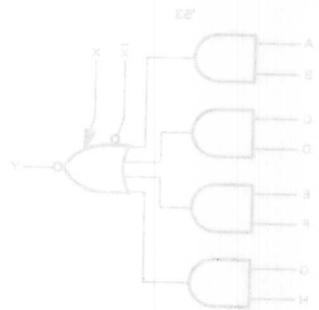
- Dependable Texas Instruments Quality and Reliability
- Package Options include Plastic and Ceramic Dips

Description

These devices contain expandable 4-wide AND-OR-INVERT gates. The 83 performs the Boolean function $Y = A\bar{B} + CD + EF + GH + X$ = output of SN74801 SN74802.

The SN74823 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74823 is characterized for operation from 0°C to 70°C.

Logic diagram



EXPANDABLE 4-WIDE AND-OR-INVERT GATES

TYPES SN74823, SN74823

REVISED DECEMBER 1983

SN74823 ... 1 PACKAGE
SN74823 ... 3 OR 9 PACKAGE



SN74823 ... W PACKAGE

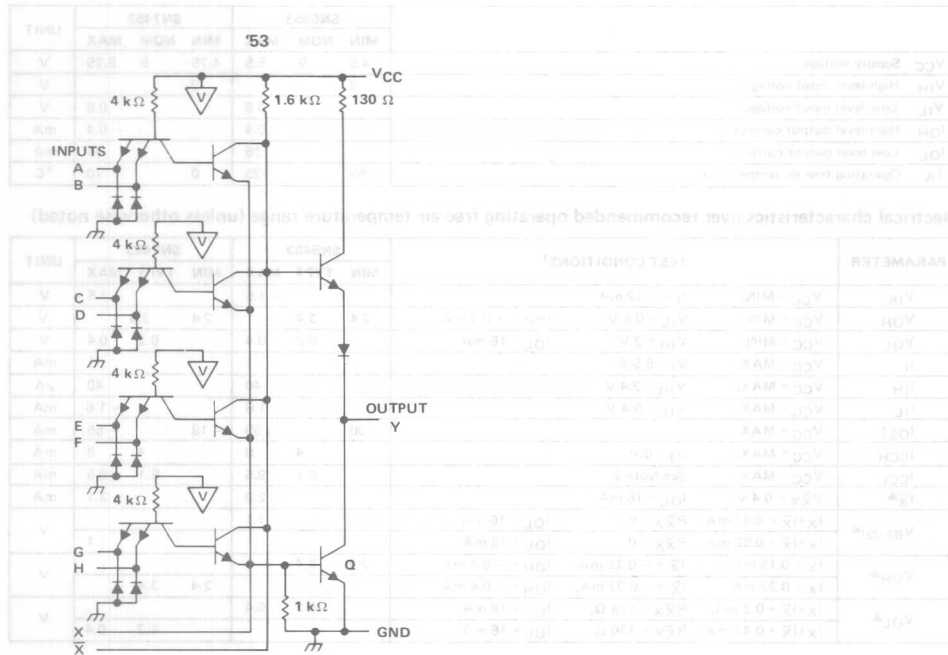


3

TTL DEVICES

TYPES SN5453, SN7453 EXPANDABLE 4-WIDE AND-OR-INVERT GATES

schematic



Resistor values shown are nominal.
If expander is not used, leave X and \bar{X} open.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX
V_{CC}	$V_{CC} = 5V$	0	7
V_{OH}	$V_{OH} = 5V$	0	5.5
V_{OL}	$V_{OL} = 5V$	0	0.5
I_{CC}	$V_{CC} = 5V$	0	10
I_{OH}	$V_{OH} = 5V$	0	10
I_{OL}	$V_{OL} = 0.5V$	0	10
t_{PD}	$V_{CC} = 5V$	0	10
t_{RST}	$V_{CC} = 5V$	0	10
t_{FALL}	$V_{CC} = 5V$	0	10
t_{RISE}	$V_{CC} = 5V$	0	10
t_{SETUP}	$V_{CC} = 5V$	0	10
t_{HOLD}	$V_{CC} = 5V$	0	10
t_{RETR}	$V_{CC} = 5V$	0	10
t_{PULSE}	$V_{CC} = 5V$	0	10
$t_{DURATION}$	$V_{CC} = 5V$	0	10
$t_{RECOVERY}$	$V_{CC} = 5V$	0	10
$t_{STORAGE}$	$V_{CC} = 5V$	0	10

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5453, SN7453

EXPANDABLE 4-WIDE AND-OR-INVERT GATES

recommended operating conditions

	SN5453			SN7453			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5453			SN7453			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4	8		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{See Note 2}$		5.1	9.5		5.1	9.5	mA
$I_{\bar{X}}^{\Delta}$	$V_{\bar{X}X} = 0.4 \text{ V}, I_{OL} = 16 \text{ mA}$			-2.9			-3.1	mA
$V_{BE(IQ)}^{\Delta}$	$I_X + I_{\bar{X}} = 0.41 \text{ mA}, R_{\bar{X}X} = 0, I_{OL} = 16 \text{ mA}$			1.1				
	$I_X + I_{\bar{X}} = 0.62 \text{ mA}, R_{\bar{X}X} = 0, I_{OL} = 16 \text{ mA}$						1	V
V_{OH}^{Δ}	$I_X = 0.15 \text{ mA}, I_{\bar{X}} = -0.15 \text{ mA}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4					
	$I_X = 0.27 \text{ mA}, I_{\bar{X}} = -0.27 \text{ mA}, I_{OH} = -0.4 \text{ mA}$				2.4	3.4		V
V_{OL}^{Δ}	$I_X + I_{\bar{X}} = 0.3 \text{ mA}, R_{\bar{X}X} = 138 \Omega, I_{OL} = 16 \text{ mA}$		0.2	0.4				
	$I_X + I_{\bar{X}} = 0.43 \text{ mA}, R_{\bar{X}X} = 130 \Omega, I_{OL} = 16 \text{ mA}$					0.2	0.4	V

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

Δ Using expander inputs, $V_{CC} = \text{MIN}, T_A = \text{MIN}$, except typical values

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}^{\S}$		13	22	ns
t_{PHL}					8	15	ns

¶ Expander pins open.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

**TYPES SN5454, SN54LS54,
SN7454, SN74LS54**
4-WIDE AND-OR-INVERT GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

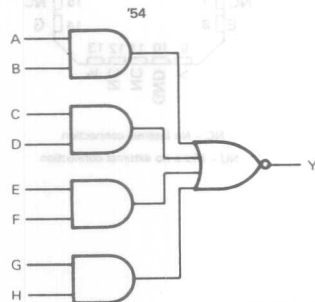
These devices contain 4-wide AND-OR-INVERT gates. They perform the following Boolean functions:

$$\text{'54 } Y = AB + CD + EF + GH$$

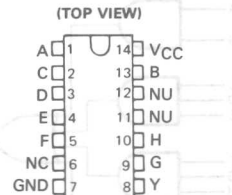
$$\text{LS54 } Y = \overline{AB + CDE + FGH + IJ}$$

The SN5454 and the SN54LS54 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7454 and the SN74LS54 are characterized for operation from 0°C to 70°C.

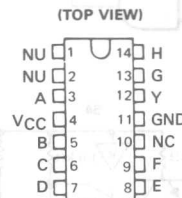
logic diagrams



SN5454 . . . J PACKAGE
SN7454 . . . J OR N PACKAGE



SN5454 . . . W PACKAGE



3

TTL DEVICES

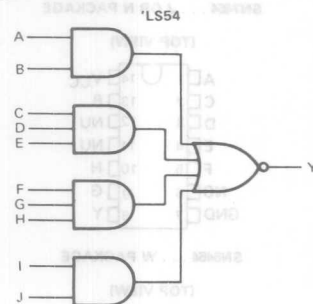
PRODUCTION DATA

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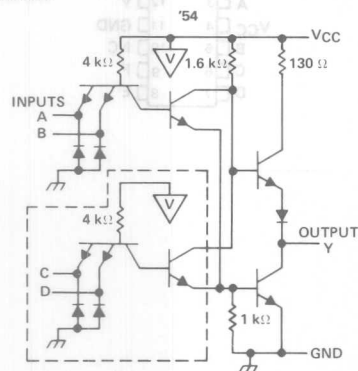
**TEXAS
INSTRUMENTS**

**TYPES SN5454, SN54LS54,
SN7454, SN74LS54
4-WIDE AND-OR-INVERT GATES**

logic diagrams (continued)



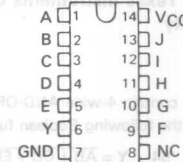
schematics



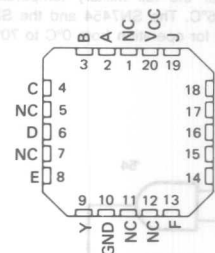
Resistor values shown are nominal.

The portion of the circuits within the dashed lines is repeated for each additional AND section.

**SN54LS54 ... J OR W PACKAGE
SN74LS54 ... D, J OR N PACKAGE
(TOP VIEW)**



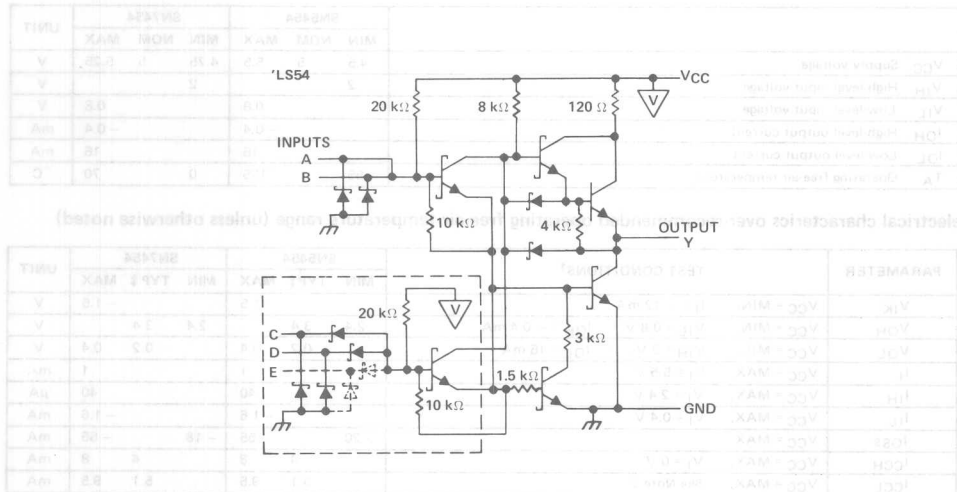
**SN54LS54 ... FK PACKAGE
SN74LS54
(TOP VIEW)**



NC - No internal connection

NU - Make no external connection

SN7454, SN74LS54
4-WIDE AND-OR-INVERT GATES



In 'LS54 circuits, 3-input gate represented by additional dashed line.

The portion of the circuits within the dashed lines is repeated for each additional AND section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '54, 'LS54	7 V
Input voltage: '54	5.5 V
'LS54	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5454, SN7454

4-WIDE AND-OR-INVERT GATES

recommended operating conditions

	SN5454			SN7454			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5454			SN7454			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4	8		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		5.1	9.5		5.1	9.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega,$	$C_L = 15 \text{ pF}$		13	22	ns
t_{PHL}						8	15	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS54, SN74LS54

4-WIDE AND-OR-INVERT GATES

recommended operating conditions

	SN54LS54			SN74LS54			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS54			SN74LS54			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS§}	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		0.8	1.6		0.8	1.6	mA
I _{CCL}	V _{CC} = MAX, See Note 2		1	2		1	2	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 2 kΩ, C _L = 15 pF		12	20	ns
t _{PHL}					12.5	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

4-WIDE AND/OR-INVERT GATES TYPES SN74LS24, SN74LS24A

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN74LS24		SN74LS24A		UNIT
		MIN	TYP	MAX	MIN	
V _{CC} Supply voltage	V _{CC} = MAX, I _{CC} = 0	4.5	5	5.5	4.5	V
V _{OH} High-level output voltage	V _{CC} = MAX, I _{OH} = 0	3			3	V
V _{OL} Low-level output voltage	V _{CC} = MAX, I _{OL} = 0	0.1			0.1	V
I _{OH} High-level output current	V _{CC} = MAX, V _{OH} = 3 V	-0.4			-0.4	mA
I _{OL} Low-level output current	V _{CC} = MAX, V _{OL} = 0.1 V	0			0	mA
T _A Operating free-air temperature		-55		125	0	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74LS24		SN74LS24A		UNIT
		MIN	TYP	MAX	MIN	
V _{IK}	V _{CC} = MAX, I _{IK} = 0	-1.5			-1.5	V
V _{OH}	V _{CC} = MAX, I _{OH} = 0	3.5	3.4		3.5	V
V _{OL}	V _{CC} = MAX, I _{OL} = 0	0.1	0.1		0.1	V
I _{OH}	V _{CC} = MAX, V _{OH} = 3 V	-0.4			-0.4	mA
I _{OL}	V _{CC} = MAX, V _{OL} = 0.1 V	0			0	mA
t _{PLH}	V _{CC} = MAX, V _{OH} = 3 V	-			-	ns
t _{PLH}	V _{CC} = MAX, V _{OL} = 0.1 V	-			-	ns
t _{PHL}	V _{CC} = MAX, V _{OH} = 3 V	-			-	ns
t _{PHL}	V _{CC} = MAX, V _{OL} = 0.1 V	-			-	ns

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5 V, T_A = 25°C.
3. For more than one output, the duration of the short-circuit should not exceed one second.
NOTE 2: All inputs to any AND gate or OR gate must be at 0 V or 5 V to ensure correct operation.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	UNIT
t _{PLH}	Any	Y	C _L = 50 pF	ns
t _{PHL}	Any	Y	C _L = 50 pF	ns

NOTE 3: See General Information Section for load circuit and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS55, SN74LS55 2-WIDE 4-INPUT AND-OR-INVERT GATES

REVISED DECEMBER 1983

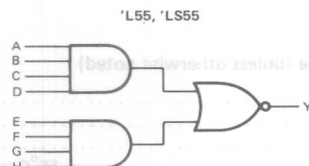
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

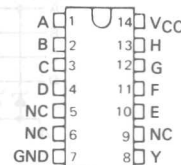
These devices contain 2-wide 4-input AND-OR-INVERT gates. 'LS55 perform the Boolean function $Y = ABCD + EFGH$.

The SN54LS55 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS55 is characterized for operation from 0°C to 70°C .

logic diagram

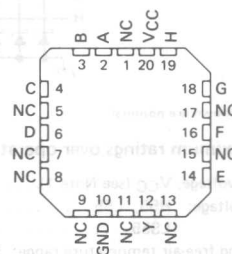


SN54LS55 ... J OR W PACKAGE
SN74LS55 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS55 ... FK PACKAGE
SN74LS55

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

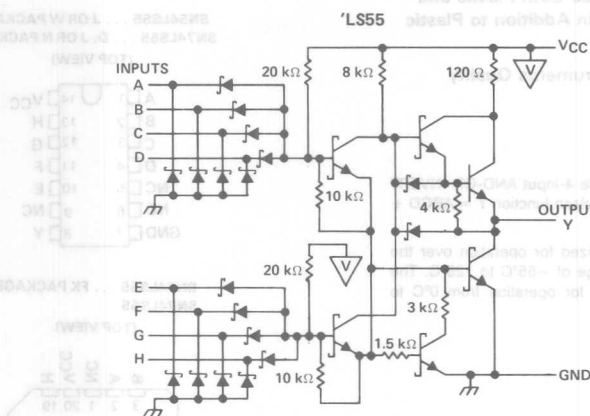
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TEXAS
INSTRUMENTS

TYPES SN54LS55, SN74LS55, 2-WIDE 4-INPUT OR-OR-INVERT GATES

schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'H55, 'L55	5.5 V
'LS55	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54LS55, SN74LS55 2-WIDE 4-INPUT AND-OR-INVERT GATES

recommended operating conditions

		SN54LS55			SN74LS55			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS55			SN74LS55			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.4	0.8		0.4	0.8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		0.7	1.3		0.7	1.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All outputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		12	20	ns
t_{PHL}					12.5	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



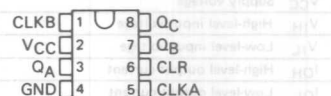
TYPES SN54LS56, SN54LS57, SN74LS56, SN74LS57 FREQUENCY DIVIDERS

REVISED DECEMBER 1983

- 'LS56 Performs 50 to 1 Frequency Division (5 to 1, 5 to 1, and 10 to 1)
- 'LS57 Performs 60 to 1 Frequency Division (6 to 1, 5 to 1, and 10 to 1)
- Available in P or JG package (two P or JG Packages Fit in a Single 16-pin Socket)
- Maximum Clock Frequency 25 MHz Typical

SN54LS56, SN54LS57 . . . JG PACKAGE
SN74LS56, SN74LS57 . . . JG OR P PACKAGE

(TOP VIEW)



FOR CHIP CARRIER INFORMATION, CONTACT THE FACTORY.

description

These frequency dividers are particularly useful in generating one second or one hour timing pulses from 50 Hz (European standard frequency) or 60 Hz (United States standard frequency). 50 to 1 frequency division is accomplished in the 'LS56 by connecting output QA to input CLKB. 60 to 1 frequency division in the 'LS57 is accomplished in the same way. More universal capabilities are evidenced by the 25 MHz typical f_{max} and the almost limitless frequency division possibilities when used in cascade. Two 'LS56 packages may be interconnected to give frequency division of 2500 to 1, 625 to 1, 100 to 1, etc. Two 'LS57 packages can be connected to generate frequency divisions of 3600 to 1, 1800 to 1, 900 to 1 etc.

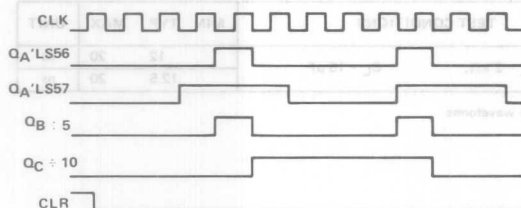
The 'LS56 and 'LS57 frequency dividers consist of three separate counters, A, B, and C on a single monolithic substrate. The A counter divides by 5 to 1 in the 'LS56 and by 6 to 1 in the 'LS57. The B counter divides by 5 to 1 in both devices and is internally tied to the C counter which divides by 2 to 1. The resulting C counter output is 10 to 1. Both the 'LS56 and 'LS57 feature a clear pin which is common to all three counters, A, B, and C. When the clear pin is low, the counters are enabled. When the clear is high, the counters are disabled and their outputs are set to a low-level.

All three counters, A, B, and C trigger on the high-to-low transition of the clock input. All output waveforms are symmetrical except for the 5 to 1 outputs (A and B of the 'LS56 and B of the 'LS57). See the output waveform drawings below.

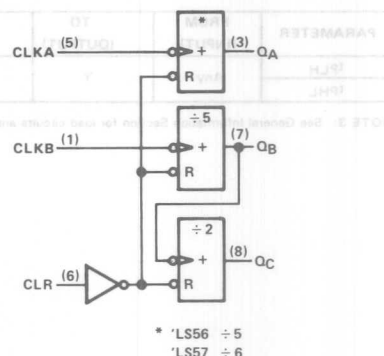
3

TTL DEVICES

input and output waveforms



logic diagram

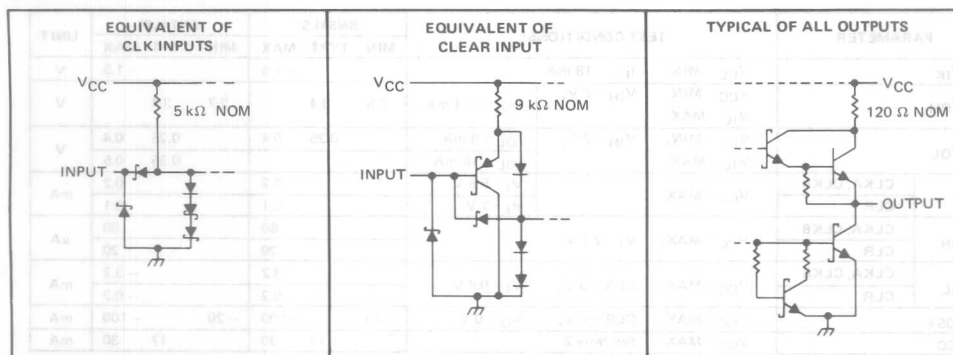


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TYPES SN54LS56, SN54LS57, SN74LS56, SN74LS57 FREQUENCY DIVIDERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: CLR	7 V
CLKA, CLKB	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	-0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			8			16	mA
f_{clock}	Clock frequency	0		15	0		15	MHz
t_r, t_f	Rise and fall time of clock			50			50	ns
t_w	Pulse width of clock or clear	30			30			ns
t_{su}	Clear inactive state set-up time	25			25			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

3

TTL DEVICES

TYPES SN54LS56, SN54LS57, SN74LS56, SN74LS57 FREQUENCY DIVIDERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS*			SN74LS*			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = −18 mA		−1.5			−1.5			V	
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OH} = −1 mA		2.5	3.4	2.7	3.4	V	
V _{OL}		V _{CC} = MIN, V _{IL} = MAX		V _{IH} = 2 V, I _{OL} = 8 mA		0.25 0.4		0.25 0.4		V	
				I _{OL} = 16 mA				0.35 0.5			
I _I	CLKA, CLKB	V _{CC} = MAX		V _I = 5.5 V		0.2		0.2		mA	
	CLR			0.1		0.1					
	V _I = 7 V										
I _{IH}	CLKA, CLKB	V _{CC} = MAX, V _I = 2.7 V				80		80		μA	
	CLR			20		20					
I _{IL}	CLKA, CLKB	V _{CC} = MAX, CLR = 0 V, V _I = 0.4 V				−3.2		−3.2		mA	
	CLR			−0.2		−0.2					
I _{OS} §		V _{CC} = MAX, CLR = 0 V, V _O = 0 V		−20		−100		−20 −100		mA	
I _{CC}		V _{CC} = MAX, See Note 2				17 30		17 30		mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured by applying 4.5 V to the CLR pin with all other inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS56			'LS57			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CLKA	Q_A	$R_L = 1 \text{ k}\Omega, C_L = 30 \text{ pF}$	15	25		15	25		MHz
f_{max}	CLKB	Q_B, Q_C		15	25		15	25		MHz
t_{PLH}	CLKB	Q_B			8	15		8	15	ns
t_{PHL}		Q_B			14	25		14	25	ns
t_{PLH}^*	CLKB	Q_C			18	30		18	30	ns
t_{PHL}^*		Q_C			24	35		24	35	ns
t_{PLH}	CLKA	Q_A			12	20		14	25	ns
t_{PHL}		Q_A			14	25		18	30	ns
t_{PHL}	CLR	Q_A			17	30		17	30	ns
t_{PHL}	CLR	Q_B			17	30		17	30	ns
t_{PHL}	CLR	Q_C			17	30		17	30	ns

* Times measured from CLKB to output Q_C are taken with output Q_B unloaded.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS63, SN74LS63 **HEX CURRENT-SENSING INTERFACE GATES** **WITH TOTEM-POLE OUTPUTS** REVISED DECEMBER 1983

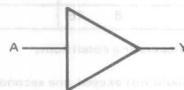
- Translates Low-Level Input Current to Low-Level Output Voltage
- Translates High-Level Input Current to High-Level Output Voltage
- Interfaces to PLA's or Other Logic Elements that Source Current but Do Not Sink Current
- Operates from a Single 5 V Supply
- TTL Compatible
- Low Power Dissipation . . . 40 mW Typical.

description

Each of these Schottky-clamped interface gates is able to discriminate between low-level ($\leq 50\mu\text{A}$) and high-level ($\geq 200\mu\text{A}$) input currents.

The outputs are fabricated with standard Low-Power Schottky design rules and are compatible with all TTL families.

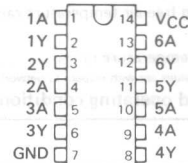
logic diagram (each gate)



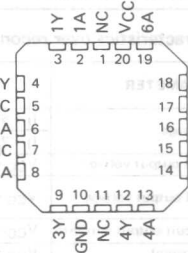
positive logic

$$Y = A$$

SN54LS63 . . . J OR W PACKAGE
 SN74LS63 . . . D, J OR N PACKAGE
 (TOP VIEW)

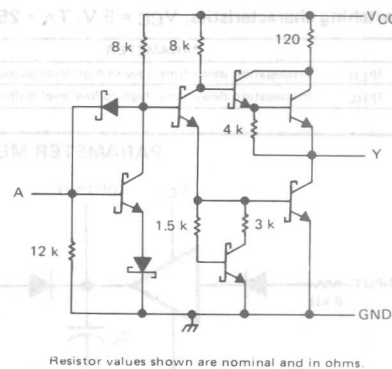


SN54LS63 . . . FK PACKAGE
 SN74LS63
 (TOP VIEW)



NC - No internal connection

schematic (each gate)



Resistor values shown are nominal and in ohms.

3

TTL DEVICES

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TEXAS
 INSTRUMENTS

8053-205

TYPES SN54LS63, SN74LS63 HEX CURRENT-SENSING INTERFACE GATES WITH TOTEM-POLE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS63	–55°C to 125°C
SN74LS63	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS63			SN74LS63			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			–400			–400	μ A
I_{OL} Low-level output current			4			8	mA
I_I Input current			1			1	mA
T_A Operating free-air temperature	–55	125	0	70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS63			SN74LS63			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I Input voltage	$I_I = 50 \mu$ A, $V_{CC} = \text{MIN}$ $I_I = 200 \mu$ A, $V_{CC} = \text{MAX}$	0.35	1.05	1.75	0.6	1.05	1.6	V
V_{OH} High-level output voltage	$V_{CC} = \text{MAX}$, $I_I = 200 \mu$ A, $I_{OH} = -400 \mu$ A	3.5	3.4		3.2	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_I = 50 \mu$ A $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$, $I_I = 600 \mu$ A	–20	–100		–20	–100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	8	16		8	16		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

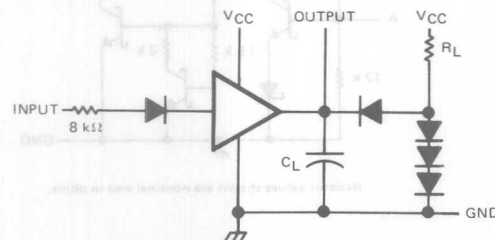
§ Not more than one output should be shorted at a time, and duration of output short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

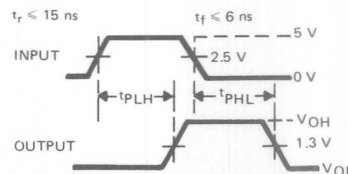
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 2 \text{ k}\Omega$, $C_L = 15 \text{ pF}$		27	45	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	25	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: a. C_L includes probe and jig capacitance
b. All diodes are 1N3064 or equivalent.

TEST CIRCUIT



VOLTAGE WAVEFORMS

TYPES SN54S64, SN54S65, SN74S64, SN74S65 4-2-3-2 INPUT AND-OR-INVERT GATES

REVISED DECEMBER 1983

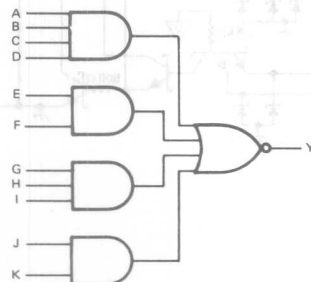
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

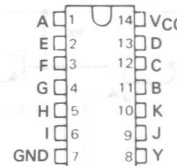
These devices contain 4-2-3-2 input AND-OR-INVERT gates. They perform the Boolean function $Y = ABCD + EF + GHI + JK$. The 'S64 has totem-pole outputs and the 'S65 has open-collector outputs.

The SN54S64 and the SN54S65 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74S64 and the SN74S65 are characterized for operation from 0°C to 70°C .

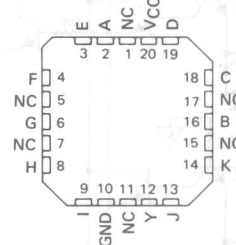
logic diagram (each device)



SN54S64, SN54S65 ... J OR W PACKAGE
SN74S64, SN74S65 ... D, J OR N PACKAGE
(TOP VIEW)



SN54S64, SN54S65 ... FK PACKAGE
SN74S64, SN74S65
(TOP VIEW)



NC - No internal connection

3

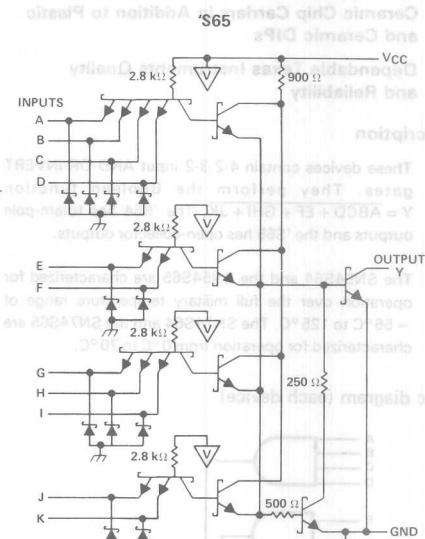
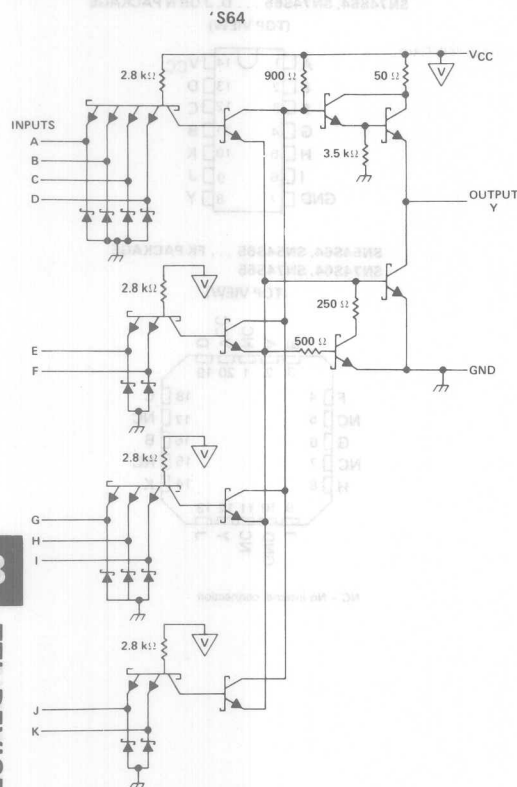
TTL DEVICES

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schematics (each gate)



3

TTL DEVICES

Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage, 'S65	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54S64, SN74S64 4-2-3-2 INPUT AND-OR-INVERT GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54S64			SN74S64			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S64			SN74S64			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		7	12.5		7	12.5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		8.5	16		8.5	16	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega,$	$C_L = 15 \text{ pF}$	3.5	5.5	ns	
t_{PHL}					3.5	5.5	ns	
t_{PLH}			$R_L = 280 \Omega,$	$C_L = 50 \text{ pF}$	5		ns	
t_{PHL}					5.5		ns	

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S65, SN74S65 4-2-3-2 INPUT AND-OR-INVERT GATES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54S65			SN74S65			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55	125		0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN.}$, $I_I = -18 \text{ mA}$			-1.2	V
I_{OH}	$V_{CC} = \text{MIN.}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 5.5 \text{ V}$			0.25	mA
V_{OL}	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5	V
I_I	$V_{CC} = \text{MAX.}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	$V_{CC} = \text{MAX.}$, $V_I = 2.7 \text{ V}$			50	μA
I_{IL}	$V_{CC} = \text{MAX.}$, $V_I = 0.5 \text{ V}$			-2	mA
I_{CCH}	$V_{CC} = \text{MAX.}$, $V_I = 0 \text{ V}$		6	11	mA
I_{CCL}	$V_{CC} = \text{MAX.}$, $V_I = 4.5 \text{ V}$		8.5	16	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega$, $C_L = 15 \text{ pF}$	2	5	7.5	ns
t_{PHL}				2	5.5	8.5	ns
t_{PLH}			$R_L = 280 \Omega$, $C_L = 50 \text{ pF}$		8		ns
t_{PHL}					6.5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS68, SN54LS69, SN74LS68, SN74LS69 DUAL 4-BIT DECADE OR BINARY COUNTERS

REVISED DECEMBER 1983

- Heavy Duty Outputs I_{OL} Rated at 8mA/16 mA
- Counter One of Either 'LS68 or 'LS69 Has Individual Clicks for the A Flip-Flop
- Direct Clear for Each 4-Bit Counter
- Guaranteed Maximum Count Frequency is 50 MHz for 'LS69 and 40 MHz for 'LS68

description

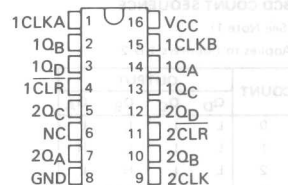
Each of the 'LS68 and 'LS69 circuits contain two four-bit counters. The 'LS68 is a dual decade counter, while the 'LS69 is a dual binary counter. Counter number one of both the 'LS68 and 'LS69 has two clock pins. Clock 1 is for the A flip-flop, while clock 2 is for the B, C, D flip-flops. Counter one of the 'LS68 can perform bi-quinary counting. All $1Q_A$ outputs are rated with sufficient I_{OL} to drive clock 2 while maintaining a full fan-out.

All clocks trigger on the high-to-low transition of the clock pulse. All counters have direct overriding clear pins which, when low, reset Q_A , Q_B , Q_C , and Q_D low regardless of the state of the clock.

The SN54LS68 and SN54LS69 circuits are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS68 and SN74LS69 circuits are characterized for operation from 0°C to 70°C .

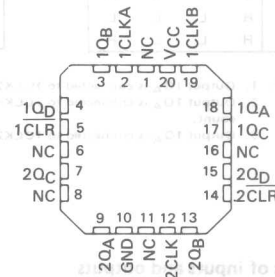
SN54LS68, SN54LS69 ... J PACKAGE
SN74LS68, SN74LS69 ... D, J OR N PACKAGE

(TOP VIEW)

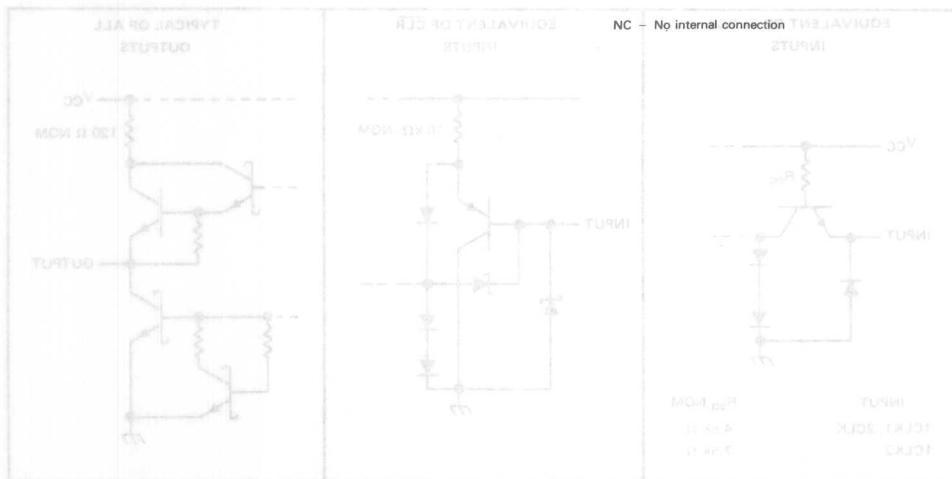


SN54LS68, SN54LS69 ... FK PACKAGE
SN74LS68, SN74LS69

(TOP VIEW)



NC - No internal connection



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TEXAS
INSTRUMENTS

TYPES SN54LS68, SN54LS69, SN74LS68, SN74LS69 DUAL 4-BIT DECADE OR BINARY COUNTERS

count sequence tables

'LS68 DECADE COUNTER

BCD COUNT SEQUENCE

(See Note 1)

Applies to Counters 1 & 2

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'LS68 DECADE COUNTER

BI-QUINARY SEQUENCE

(See Note 2)

Applies to Counter 1 only

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'LS69 BINARY COUNTER

BCD COUNT SEQUENCE

(See Note 3)

Applies to Counters 1 & 2

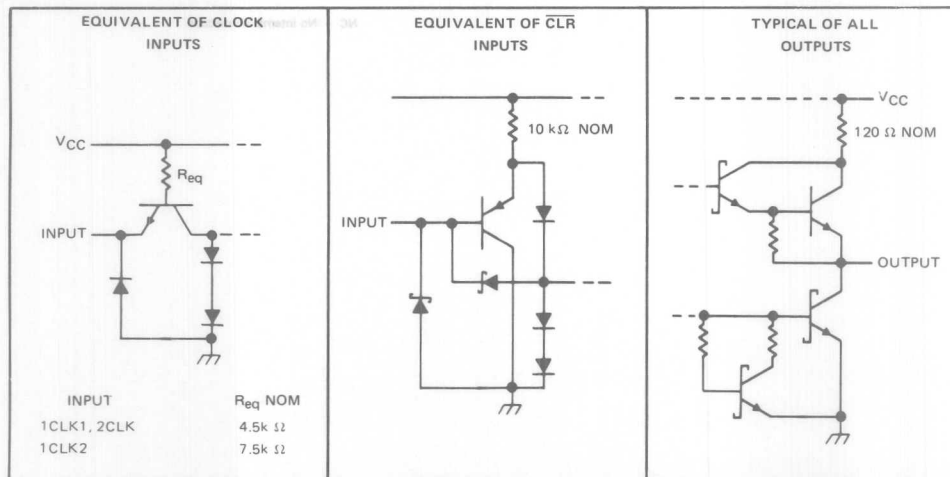
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

- NOTES: 1. Output 1Q_A is connected to 1CLK2 for BCD count.
2. Output 1Q_A is connected to 1CLK1 for bi-quinary count.
3. Output 1Q_A is connected to 1CLK2 for binary count.

3

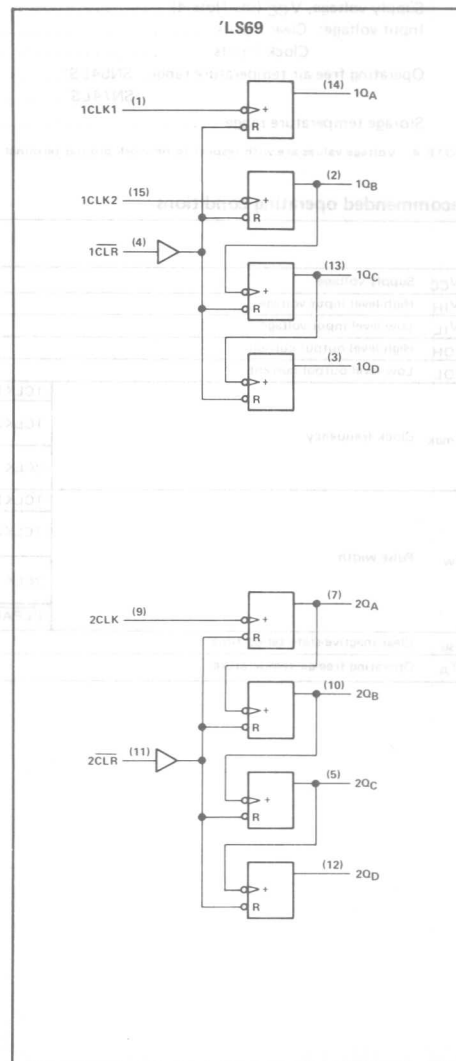
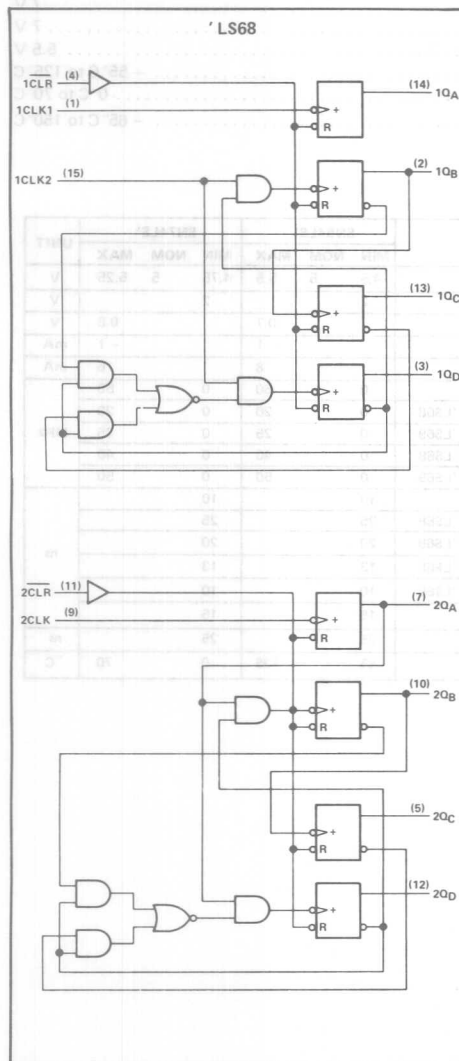
schematics of inputs and outputs

TTL DEVICES



TYPES SN54LS68, SN54LS69, SN74LS68, SN74LS69
DUAL 4-BIT DECADE OR BINARY COUNTERS

logic diagrams



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54LS68, SN54LS69, SN74LS68, SN74LS69 DUAL 4-BIT DECADE OR BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4)	7 V
Input voltage: Clear inputs	7 V
Clock inputs	5.5 V
Operating free-air temperature range: SN54LS'	-55° C to 125° C
SN74LS'	0° C to 70° C
Storage temperature range	-65° C to 150° C

NOTE 4: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-1			-1	mA
I _{OL}	Low-level output current			8			16	mA
f _{max}	Clock frequency	1CLK1		0	50	0	50	MHz
		1CLK2	'LS68	0	20	0	20	
			'LS69	0	25	0	25	
		2CLK	'LS68	0	40	0	40	
			'LS69	0	50	0	50	
t _w	Pulse width	1CLK1		10		10	ns	
		1CLK2	'LS68	25		25		
			'LS69	20		20		
		2CLK	'LS68	13		13		
			'LS69	10		10		
		CLEAR		15		15		
t _{su}	Clear inactive-state set-up time			25		25	ns	
T _A	Operating free-air temperature	-55		125	0		70	°C

3

TTL DEVICES

TYPES SN54LS68, SN54LS69, SN74LS68, SN74LS69 DUAL 4-BIT DECADE OR BINARY COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}, I_{OL} = 16 \text{ mA}$				0.35	0.5		
I_I	CLK $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1			0.1	mA
	CLR $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	
I_{IH}	CLK $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			40			40	μA
	CLR $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	
I_{IL}	1CLK1, 2CLK			-2			-2	mA
	1CLK2			-1.2			-1.2	
	CLR			-0.2			-0.2	
				-0.2			-0.2	
I_{OS}^{\S}	$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$	-20	-100		-20	-100		mA
I_{CC}	$V_{CC} = \text{MAX}, \text{see Note 5}$	36	54		36	54		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 5: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS68			'LS69			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	1CLK1	1Q _A	$R_L = 1 \text{ k}\Omega, C_L = 30 \text{ pF}$	50	70		50	70		MHz
f_{max}		1Q _B , 1Q _C , 1Q _D		20	30		25	35		MHz
f_{max}		2Q _A , 2Q _B , 2Q _C , 2Q _D		40	60		50	70		MHz
t_{PLH}	1CLK1	1Q _A		7	11		7	11		ns
t_{PHL}		1Q _A		14	21		14	21		ns
t_{PLH}	1CLK2	1Q _B		8	12		7	11		
t_{PHL}		1Q _B		12	18		14	21		
t_{PLH}		1Q _C		15	23		16	24		
t_{PHL}		1Q _C		21	32		21	32		
t_{PLH}	2CLK	1Q _D		8	12		25	38		ns
t_{PHL}		1Q _D		13	20		30	45		
t_{PLH}		2Q _A		7	11		7	11		
t_{PHL}		2Q _A		14	21		14	21		
t_{PLH}	2CLK	2Q _B		16	24		14	21		ns
t_{PHL}		2Q _B		19	29		19	29		
t_{PLH}		2Q _C		23	35		23	35		
t_{PHL}		2Q _C		27	40		27	40		
t_{PLH}	2CLK	2Q _D		16	24		32	48		ns
t_{PHL}		2Q _D		19	29		36	54		
t_{PLH}		Any Q		20	30		20	30		
t_{PHL}		Any Q		20	30		20	30		

NOTE 6: See General Information Section for load circuits and voltage waveforms.

TYPES SN5470, SN7470 AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and \bar{Q} outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium-to-high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

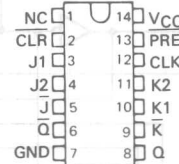
The SN5470 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7470 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

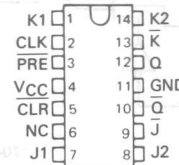
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L	L
H	H	↑	L	L	Q_0	Q_0
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q_0	Q_0

If inputs J and K are not used, they must be grounded. Preset or clear function can occur only when the clock input is low.
This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SN5470 ... J PACKAGE
SN7470 ... J OR N PACKAGE
(TOP VIEW)

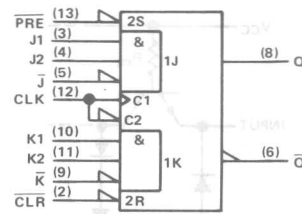


SN5470 ... W PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown are for J and N packages only.

positive logic

$$J = J1 \cdot J2 \cdot \bar{J}$$

$$K = K1 \cdot K2 \cdot \bar{K}$$

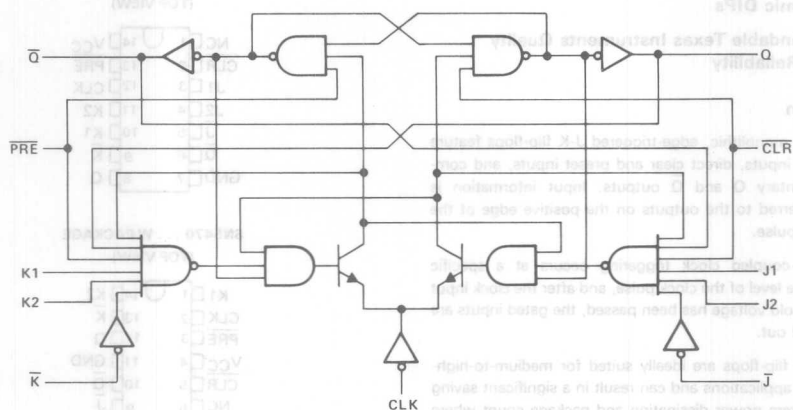
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



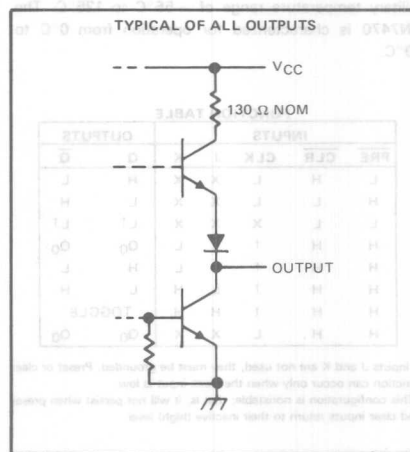
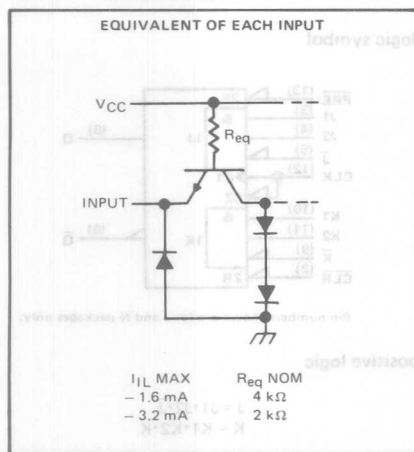
TYPES SN5470, SN7470 AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

logic diagram



'70-GATED J-K WITH CLEAR AND PRESET

schematics of input and outputs



3 TTL DEVICES

TYPES SN5470, SN7470 AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature: SN5470	–55°C to 125°C
SN7470	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5470			SN7470			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			−0.4			−0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _W	Pulse duration	CLK high		20	20			ns
		CLK low		30	30			
		PRE or CLR low		25	25			
t _{SU}	Setup time before CLK †	20			20			ns
t _H	Hold time-Data after CLK †	5			5			ns
T _A	Operating free-air temperature	−55		125	0		70	°C

† The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5470			SN7470			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = – 12 mA		– 1.5			– 1.5			V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = – 0.4 mA		2.4	3.4		2.4	3.4		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I _I		V _{CC} = MAX, V _I = 5.5 V		1			1			mA
I _{IH}	PRE or CLR	V _{CC} = MAX, V _I = 2.4 V		80			80			µA
	All other			40			40			
I _{IL}	PRE or CLR★	V _{CC} = MAX, V _I = 0.4 V		– 3.2			– 3.2			mA
	All other			– 1.6			– 1.6			
I _{OS} §		V _{CC} = MAX		– 20	– 57		– 18	– 57		mA
I _{CC}		V _{CC} = MAX, See Note 2		13	26		13	26		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

*Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

TYPES SN5470, SN7470 **AND-GATED J-K POSITIVE-EDGE-TRIGGERED** **FLIP-FLOPS WITH PRESET AND CLEAR**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				20	35		MHz
t_{PLH}	PRE or CLR	Q or \bar{Q}	$R_L = 400\ \Omega$, $C_L = 15\text{ pF}$			50	ns
t_{PHL}						50	ns
t_{PLH}	CLK	Q or \bar{Q}				27	ns
t_{PHL}						18	ns

¹ f_{max} maximum clock frequency; t_{PLH} = propagation delay time, low-to-high level output;
 t_{PHL} propagation delay time, high-to-low level output.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

PARAMETER	UNIT	MIN	TYP	MAX
V_{CC} Supply voltage	V	4.5	5.0	5.5
V_{IH} High-level input voltage	V	2		
V_{IL} Low-level input voltage	V	0.8		
I_{OH} High-level output current	mA	-0.4		
I_{OL} Low-level output current	mA	18		
t_w Pulse duration	ns		20	
	ns		30	
	ns		28	
t_{SET} Setup time before CLK ¹	ns		30	
t_{HOLD} Hold time after CLK ¹	ns		5	
T_A Operating free-air temperature	$^\circ\text{C}$	-55	125	0

¹ The arrow indicates the edge of the clock pulse used for reference. For the setup delay, t_{SET} , the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	MIN	TYP	MAX	UNIT
V_{IK}	$V_{CC} - \text{MIN}$, $I_K = -15\text{ mA}$	-1.5			V
V_{OH}	$V_{CC} - \text{MIN}$, $V_{IH} = 2\text{ V}$	2.4	2.4	2.4	V
	$V_{CC} - \text{MIN}$, $I_{OH} = -0.4\text{ mA}$	2.4	2.4	2.4	V
V_{OL}	$V_{CC} - \text{MIN}$, $V_{IL} = 0.8\text{ V}$	0.2	0.2	0.2	V
	$V_{CC} - \text{MIN}$, $I_{OL} = 18\text{ mA}$	0.2	0.2	0.2	V
I_I	$V_{CC} - \text{MAX}$, $V_I = 0\text{ V}$	1			mA
I_H	PRE or CLR, $V_{CC} - \text{MAX}$, $V_I = 2.4\text{ V}$	30			mA
	data input, $V_{CC} - \text{MAX}$, $V_I = 2.4\text{ V}$	40			mA
I_L	PRE or CLR, $V_{CC} - \text{MAX}$, $V_I = 0.4\text{ V}$	2.2			mA
	data input, $V_{CC} - \text{MAX}$, $V_I = 0.4\text{ V}$	1.5			mA
I_{DC}	$V_{CC} - \text{MAX}$	50			mA
I_{CC}	$V_{CC} - \text{MAX}$, see Note 3	12	12	12	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified when recommended operating free-air temperature is 25°C .

² All typical values were measured at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

³ For input and output signals, the delay time is the time from the input signal to the output signal.

⁴ Clear is tested with output high and 50-ohm load. Output high is tested with 50-ohm load.

NOTE 3: With all outputs open, I_{CC} is measured with the Q output high and \bar{Q} output low. All other inputs are held high or low as indicated. The clock input is held high.

3-220

3

TTL DEVICES

TYPES SN5472, SN7472

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

The SN5472 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7472 is characterized for operation from 0°C to 70°C .

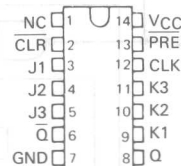
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^{\dagger}	H^{\dagger}
H	H	\downarrow	L	L	Q_0	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	

\dagger This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

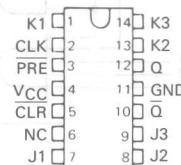
SN5472 ... J PACKAGE SN7472 ... J OR N PACKAGE

(TOP VIEW)



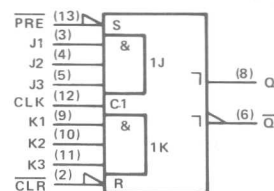
SN5472 ... W PACKAGE

(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown are for J and N packages.

positive logic

$$J = J1 \cdot J2 \cdot J3$$

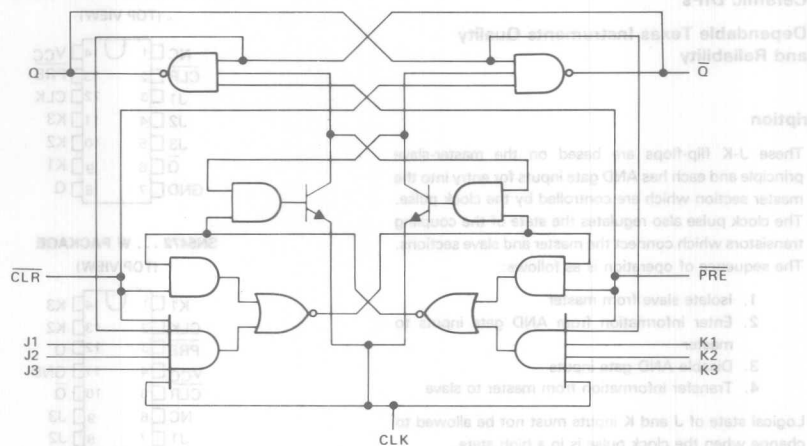
$$K = K1 \cdot K2 \cdot K3$$

PRODUCTION DATA

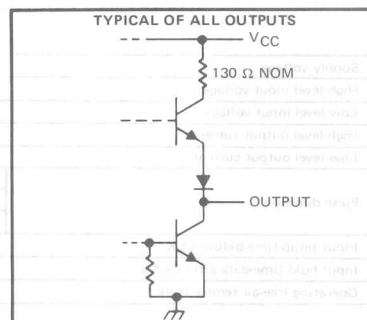
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TEXAS
INSTRUMENTS

logic diagram:
'72



TTL DEVICES



..... 7 V

55 V

55°C : 105°C

- 55 °C to 125 °C

TYPES SN5472, SN7472

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN5472			SN7472			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
t_w	Pulse duration	CLK high	20		20			ns
		CLK low	47		47			
		PRE or CLR	25		25			
t_{su}	Input setup time before CLK \uparrow	0			0			ns
t_h	Input hold time-data after CLK \downarrow	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS \dagger	SN5472			SN7472			UNIT
			MIN	TYP \ddagger	MAX	MIN	TYP \ddagger	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	J or K	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40			40		μA
	All other			80			80		
I_{IL}	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6			-1.6		mA
	All other			-3.2			-3.2		
$I_{OS}\S$		$V_{CC} = \text{MAX}$	-20	-57		-18	-57		mA
I_{CC}		$V_{CC} = \text{MAX},$ See Note 2	10	20		10	20		mA

\dagger For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

\ddagger All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

\S Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			$R_L = 400 \Omega, C_L = 15 \text{ pF}$		15	20		MHz
t_{PLH}	$\bar{\text{PRE}}$ or $\bar{\text{CLR}}$	Q or \bar{Q}			16	25		ns
t_{PHL}					25	40		ns
t_{PLH}	CLK	Q or \bar{Q}			16	25		ns
t_{PHL}					25	40		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

**TYPES SN5473, SN54LS73A
SN7473, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR**
REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

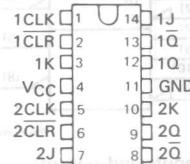
The '73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73 are positive pulsetriggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

The SN5473 and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7473 and the SN74LS73A are characterized for operation from 0°C to 70°C .

SN5473, SN54LS73A ... J OR W PACKAGE
SN7473 ... J OR N PACKAGE
SN74LS73A ... D, J OR N PACKAGE

(TOP VIEW)



'73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	H	X	X	Q_0	Q_0

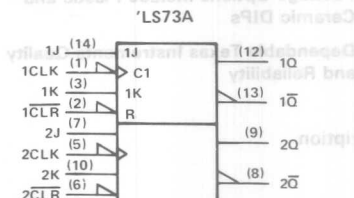
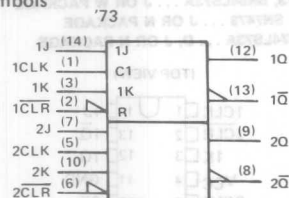
FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

3

TTL DEVICES

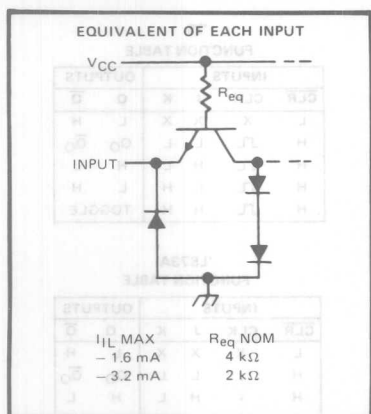
**TYPES SN5473, SN54LS73A
SN7473, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR**

logic symbols

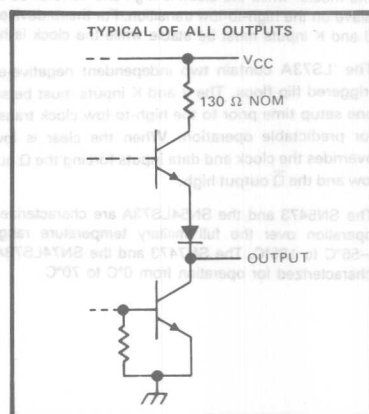


Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



'73



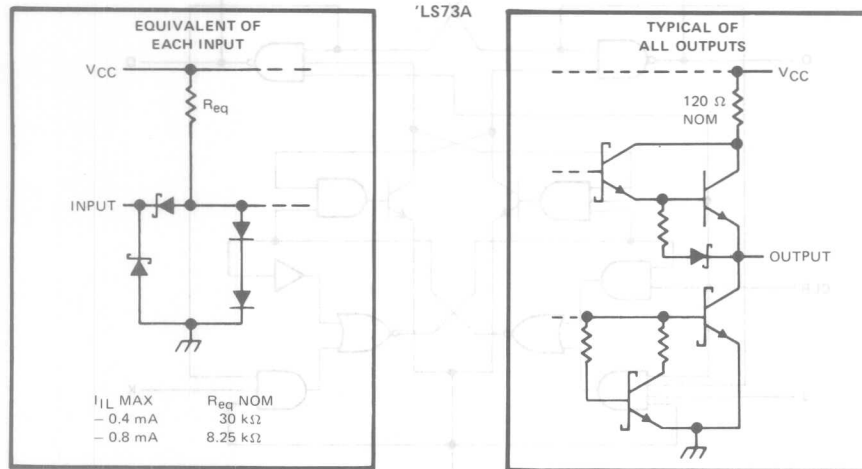
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TTL DEVICES

TYPES SN54LS73A, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

schematics of inputs and outputs (continued)

logic diagram

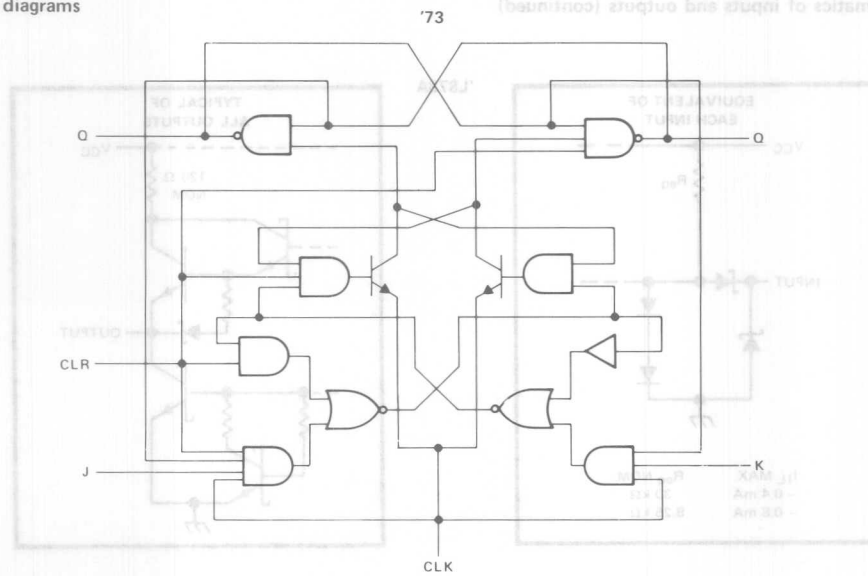


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TTL DEVICES

TYPES SN5473, SN7473
DUAL J-K FLIP-FLOPS WITH CLEAR

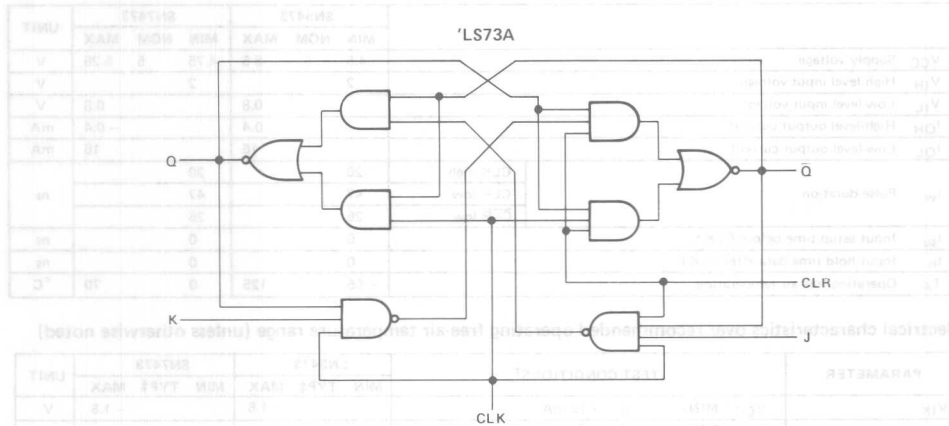
logic diagrams



3 TTL DEVICES

TYPES SN5473, SN54LS73A
SN7473, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

logic diagrams (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '73	5.5 V
'LS73A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3
TTL DEVICES

PARAMETER ¹	FROM	TO	TEST CONDITIONS	UNIT
t_{PLH}	Q	Q	$V_{CC} = 5V, T_A = 25°C$	ns
t_{PLZ}	Q	Q	$V_{CC} = 5V, T_A = 25°C$	ns
t_{PHL}	Q	Q	$V_{CC} = 5V, T_A = 25°C$	ns
t_{PZL}	Q	Q	$V_{CC} = 5V, T_A = 25°C$	ns

TYPES SN5473, SN7473

DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

		SN5473			SN7473			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration	CLK high	20		20			ns
		CLK low	47		47			
		CLR low	25		25			
t _{su}	Input setup time before CLK ↑	0			0			ns
t _h	Input hold time data after CLK ↓	0			0			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5473			SN7473			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	J or K			40			40	μA
	CLR or CLK			80			80	
I _{IL}	J or K			-1.6			-1.6	mA
	CLR			-3.2			-3.2	
	CLK			-3.2			-3.2	
I _{OS} §	V _{CC} = MAX	-20		-57	-18		-57	mA
I _{CC}	V _{CC} = MAX, See Note 2		10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 400 Ω, C _L = 15 pF	15	20		MHz
t _{PLH}	CLR	Q			16	25	ns
t _{PHL}		Q			25	40	ns
t _{PLH}	CLK	Q or Q			16	25	ns
t _{PHL}		Q or Q			25	40	ns

¶ f_{max} - maximum clock frequency; t_{PLH} - propagation delay time, low-to-high-level output; t_{PHL} - propagation delay time, high-to-low-level output.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS73A, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

			SN54LS73A			SN74LS73A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current		−0.4			−0.4			mA
I _{OL}	Low-level output current		4			8			mA
f _{clock}	Clock frequency		0	30		0	30		MHz
t _w	Pulse duration		CLK high		20				ns
			CLR low		20				
t _{su}	Set up time-before CLK ↓		data high or low		20				ns
			CLR inactive		20				
t _h	Hold time-data after CLK ↓		0		0				ns
T _A	Operating free-air temperature		− 55		125		0 70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS73A		SN74LS73A		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN, I _I = − 18 mA	− 1.5		− 1.5			V
V _{OH}		V _{CC} = MIN, I _{OH} = − 0.4 mA	2.5	3.4		2.7	3.4	V
V _{OL}		V _{CC} = MIN, I _{OL} = 4 mA	0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, I _{OL} = 8 mA				0.35	0.5	
I _I	J or K	V _{CC} = MAX, V _I = 7 V	0.1		0.1		mA	
	CLR		0.3		0.3			
	CLK		0.4		0.4			
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V	20		20		μA	
	CLR		60		60			
	CLK		80		80			
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V	− 0.4		− 0.4		mA	
	CLR or CLK		− 0.8		− 0.8			
I _{OS} §		V _{CC} = MAX, See Note 4	− 20	− 100	− 20	− 100	mA	
I _{CC}		V _{CC} = MAX, See Note 2	4	6	4	6	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		30	45		MHz
t_{PLH}	CLR or CLK	Q or \bar{Q}			15	20		ns
t_{PHL}					15	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN5474, SN54LS74A, SN54S74 SN7474, SN74LS74A, SN74S74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

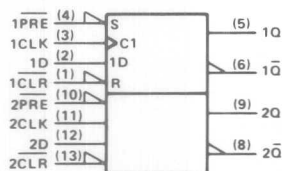
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H^{\dagger}	H^{\dagger}
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

\dagger The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

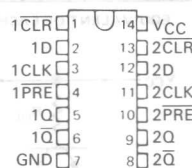
SN5474 ... J PACKAGE

SN54LS74A, SN54S74 ... J OR W PACKAGE

SN7474 ... J OR N PACKAGE

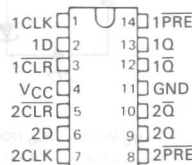
SN74LS74A, SN74S74 ... D, J OR N PACKAGE

(TOP VIEW)



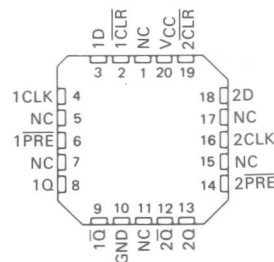
SN5474 ... W PACKAGE

(TOP VIEW)



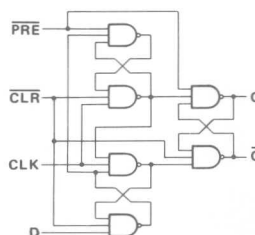
SN54LS74A, SN54S74 ... FK PACKAGE
SN74LS74A, SN74S74

(TOP VIEW)



NC - No internal connection

logic diagram



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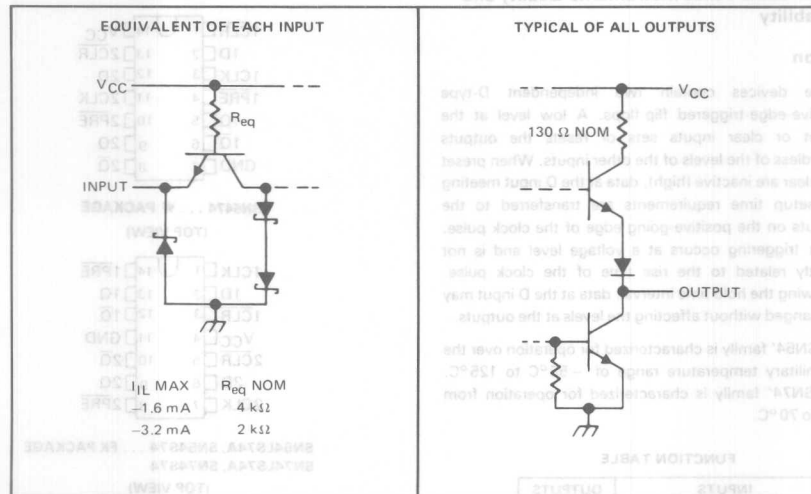
TEXAS
INSTRUMENTS

TYPES SN5474, SN7474

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs

74

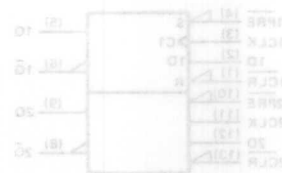


FUNCTION TABLE

PRE	CLR	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	L
H	H	X	X	L	H
H	H	L	L	L	H
H	H	L	X	X	L

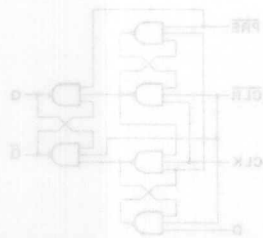
1 The output levels (the configuration are not guaranteed) to meet the minimum level in V_{CC} if the level is greater and data the level V_{CC} maximum. Furthermore, this can be a positive level, it will not be zero when the power is applied to the inactive (high) level.

logic symbol



Pin numbers shown in logic notation are for D, 16-pin package.

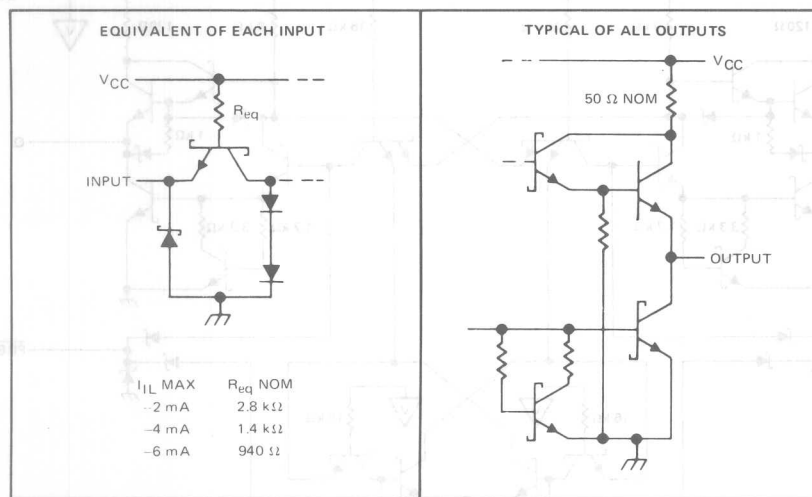
logic diagram



3

TTL DEVICES

'S74



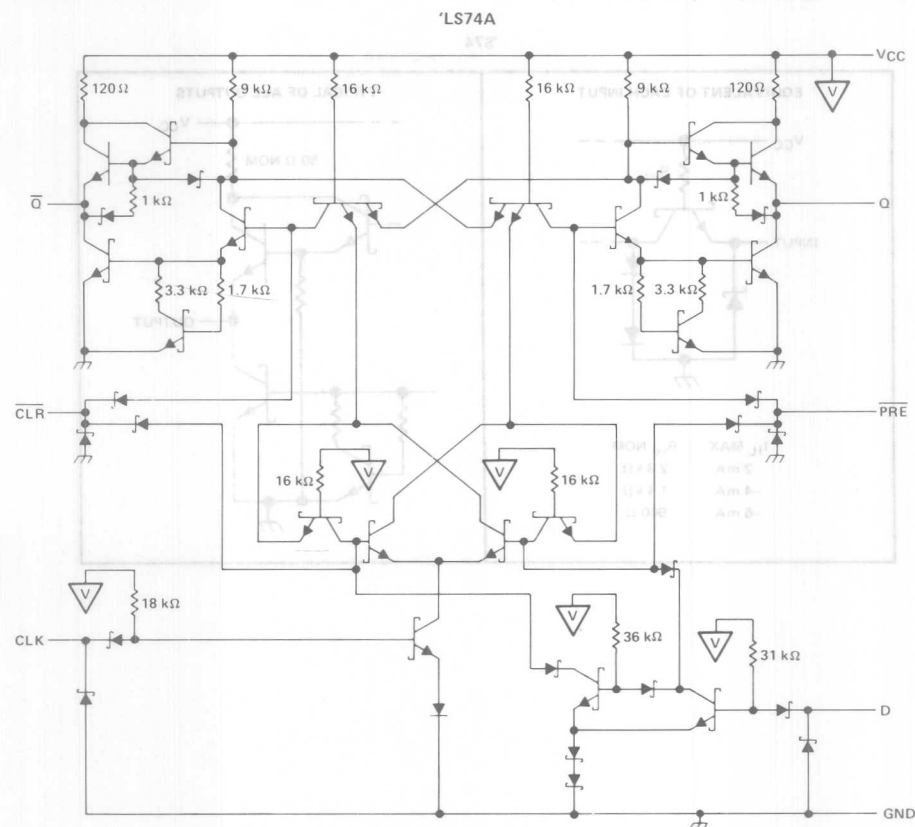
3

TTL DEVICES

Storage temperature range: -55°C to 180°C
 Operating free-air temperature range: 0°C to 70°C
 Input voltage: 0V to 5.5V
 Output voltage: 0V to 5.5V
 Supply voltage: 5V to 5.5V
 Absolute maximum ratings over operating free-air temperature range (unless otherwise noted):

**TYPES SN5474, SN54LS74A, SN54S74
SN7474, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '74, 'S74	5.5 V
'LS74A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

ALST. JAT TYPES SN5474, SN7474 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

PARAM	DESCRIPTION	SN5474			SN7474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration			CLK high	30			ns
				CLK low	37			ns
				PRE or CLR low	30			ns
t _{su}	Input setup time before CLK †	20			20			ns
t _h	Input hold time-data after CLK †	5			5			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5474			SN7474			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	D			40			40	mA
	CLR			120			120	mA
	All Other			80			80	mA
I _{IL}	D			-1.6			-1.6	mA
	PRE*			-1.6			-1.6	mA
	CLR*			-3.2			-3.2	mA
	CLK			-3.2			-3.2	mA
I _{OS} §	V _{CC} = MAX	-20		-57	-18		-57	mA
I _{CC} Supply Current (average per Flip-Flop)	V _{CC} = MAX, See Note 2		8.5	15		8.5	15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

* Clear is tested with preset high and preset is tested with clear high.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				15	25		MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	R _L = 400 Ω, C _L = 15 pF			25	ns
t _{PHL}		Q or \bar{Q}				40	ns
t _{PLH}	CLK	Q or \bar{Q}			14	25	ns
t _{PHL}		Q or \bar{Q}			20	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS74A, SN74LS74A DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS74A			SN74LS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			− 0.4			− 0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		25	0		25	MHz
t _w	Pulse duration	CLK high			25			ns
		PRE or CLR low			25			
t _{su}	Setup time-before CLK ↑	High-level data			20			ns
		Low-level data			20			
t _h	Hold time-data after CLK ↑	5			5			ns
T _A	Operating free-air temperature	− 55			0			70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS74A			SN74LS74A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35	0.5		V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$							V
I_I	D or CLK			0.1			0.1	mA
	CLR or PRE			0.2			0.2	mA
I_{IH}	D or CLK			20			20	μA
	CLR or PRE			40			40	μA
I_{IL}	D or CLK			-0.4			-0.4	mA
	CLR or PRE			-0.8			-0.8	mA
I_{OS}^{\S}	$V_{CC} = \text{MAX}, \text{ See Note 4}$	-20		-100	-20		-100	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ See Note 2}$	4		8	4		8	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{\max}			$R_L = 2\text{ k}\Omega,$	$C_L = 15\text{ pF}$	25	33		MHz
t_{PLH}	$\overline{CLR}, \overline{PRE}$ or CLK	Q or \overline{Q}			13	25		ns
t_{PHL}					25	40		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S74, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			SN54S74			SN74S74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				-1			-1	mA
I_{OL}	Low-level output current				20			20	mA
t_W	Pulse duration	CLK high	6			6			ns
		CLK low	7.3			7.3			
		CLR or PRE low	7			7			
t_{su}	Setup time, before CLK \uparrow	High-level data	3			3			ns
		Low-level data	3			3			
t_h	Input hold time, data after CLK \uparrow		2			2			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S74			SN74S74			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	D	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	mA
	CLR				150			150	
	PRE or CLK				100			100	
I_{IL}	D	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
	CLR*				-6			-6	
	PRE*				-4			-4	
	CLK				-4			-4	
$I_{OS}§$		$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CC} Supply Current (average per Flip-Flop)		$V_{CC} = \text{MAX},$ See Note 2	15	25		15	25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: All outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				75	110		MHz
t_{PLH}	PRE or CLR	Q or \bar{Q}	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	4	6		ns
t_{PHL}	PRE or CLR (CLK high)	\bar{Q} or Q		9	13.5		ns
	PRE or CLR (CLK low)			5	8		ns
t_{PLH}	CLK	Q or \bar{Q}		6	9		ns
t_{PHL}				6	9		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

FUNCTION TABLE

(each latch)

INPUTS		OUTPUTS	
D	C	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = high level, L = low level, X = irrelevant

 Q_0 = the level of Q before the high-to-low transition of G

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75, and 'LS75 feature complementary Q and \bar{Q} outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77, and 'LS77 4-bit latches are available in 14-pin flat packages.

These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54, and 54LS devices are characterized for operation over the fully military temperature range of -55°C to 125°C ; Series 74, and 74LS devices are characterized for operation from 0°C to 70°C .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '75, '77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

PRODUCTION DATA

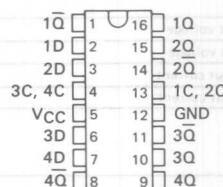
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SN5475, SN54LS75 ... J OR W PACKAGE

SN7475 ... J OR N PACKAGE

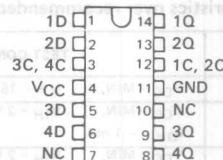
SN74LS75 ... D, J OR N PACKAGE

(TOP VIEW)



SN5477, SN54LS77 ... W PACKAGE

(TOP VIEW)

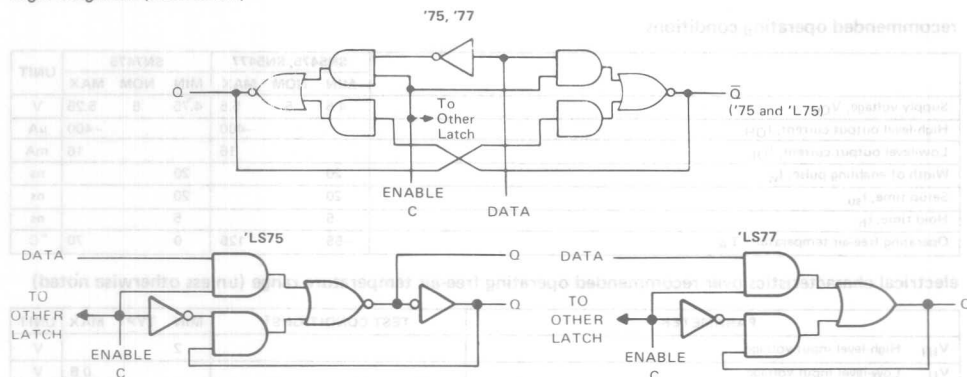


NC - No internal connection.

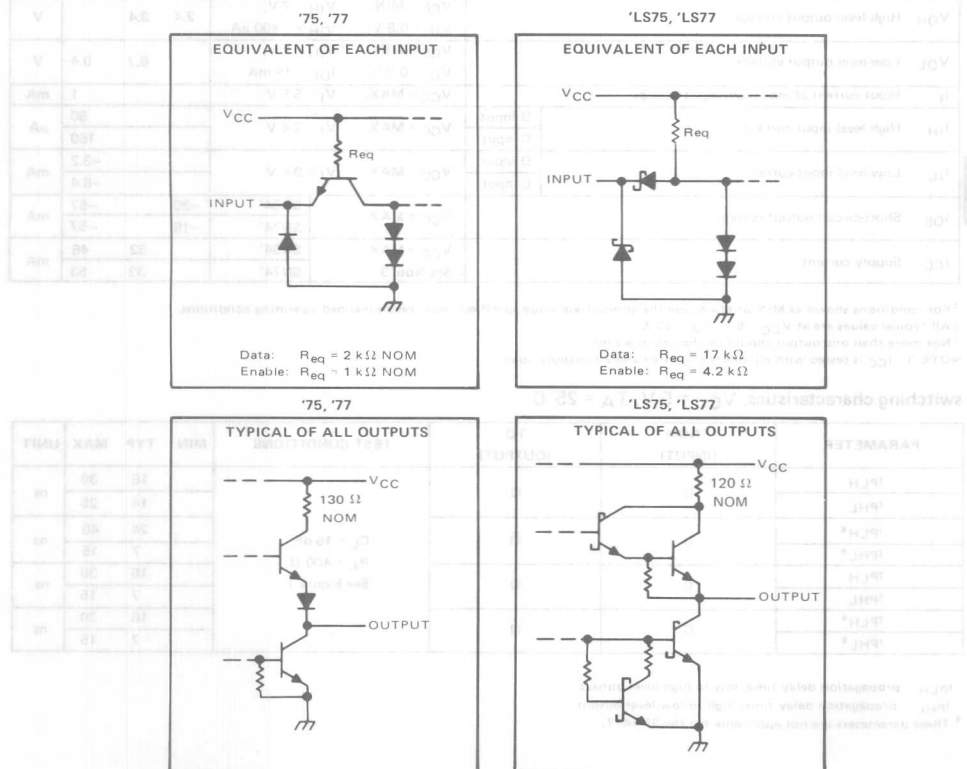
FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

TYPES SN5475, SN5477, SN54LS75, SN54LS77, SN7475, SN74LS75 4-BIT BISTABLE LATCHES

logic diagrams (each latch)



schematics of inputs and outputs



TYPES SN5475, SN5477, SN7475 4-BIT BISTABLE LATCHES

recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	D input			80	μ A
		C input			160	
I_{IL}	Low-level input current	D input			-3.2	mA
		C input			-6.4	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$				mA
I_{CC}	Supply current	SN54'	-20		-57	
		SN74'	-18		-57	
		$V_{CC} = \text{MAX}$, SN54'		32	46	mA
		See Note 3, SN74'		32	53	





[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}		Q	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1	16	30	ns	
t_{PHL}		Q		14	25		
t_{PLH}^*		\bar{Q}		24	40	ns	
t_{PHL}^*		\bar{Q}		7	15		
t_{PLH}		Q		16	30	ns	
t_{PHL}		Q		7	15		
t_{PLH}^*		\bar{Q}		16	30	ns	
t_{PHL}^*		\bar{Q}		7	15		

t_{PLH} propagation delay time, low to high-level output

t_{PHL} propagation delay time, high to low-level output

* These parameters are not applicable for the SN5477.

TYPES SN54LS75, SN54LS77, SN74LS75 4-BIT BISTABLE LATCHES

recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS75 SN54LS77			SN74LS75			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$							V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	mA
		$I_{OL} = 8 \text{ mA}$				0.35	0.5	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	D input		0.1			0.1	μ A
		C input		0.4			0.4	
		D input		20			20	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	C input		80			80	mA
		D input		-0.4			-0.4	
I_{OS} Short-circuit output current [‡]	$V_{CC} = \text{MAX}$	D input		-1.6			-1.6	mA
		C input		-20	-100	-20	-100	
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	'LS75		6.3	12	6.3	12	mA
		'LS77		6.9	13			

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡]Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [‡]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			'LS77			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figure 1	15	27		11	19		ns
t_{PHL}				9	17		9	17		
t_{PLH}				12	20					
t_{PHL}	C	\bar{Q}		7	15					ns
t_{PLH}				15	27		10	18		
t_{PHL}				14	25		10	18		
t_{PLH}	C	\bar{Q}		16	30					ns
t_{PHL}				7	15					

[‡] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

**TYPES SN5475, SN5477, SN54LS75, SN54LS77,
SN7475, SN74LS75
4-BIT BISTABLE LATCHES**

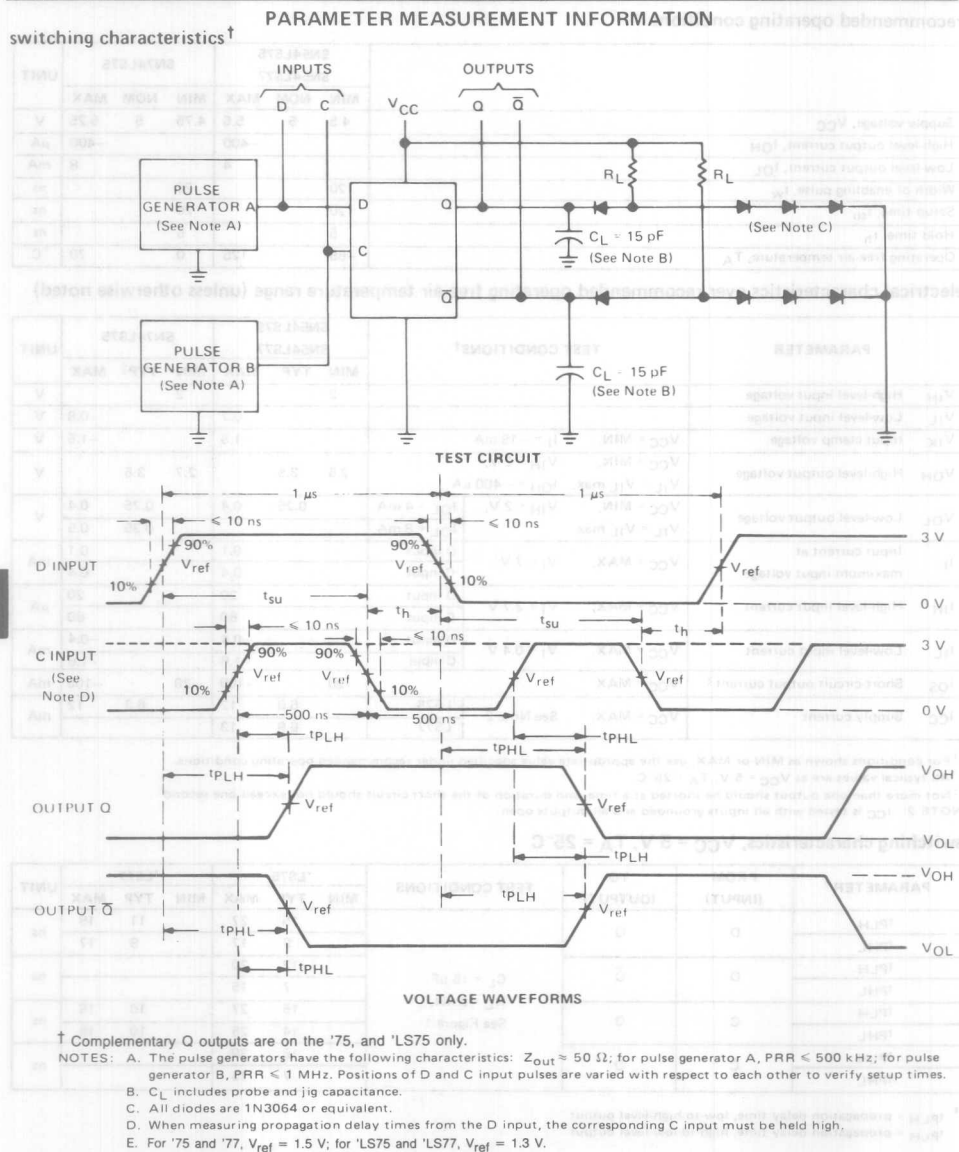


FIGURE 1

**TYPES SN5476, SN54LS76A,
SN7476, SN74LS76A
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR**

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

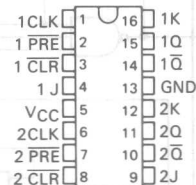
description

The '76 contain two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 are positive-edge-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476, and the SN54LS76A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7476 and the SN74LS76A are characterized for operation from 0°C to 70°C .

SN5476, SN54LS76A ... J OR W PACKAGE
SN7476 ... J OR N PACKAGE
SN74LS76A ... D, J OR N PACKAGE
(TOP VIEW)



**'76
FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE

**'LS76A
FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	Q̄ ₀

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

3

TTL DEVICES

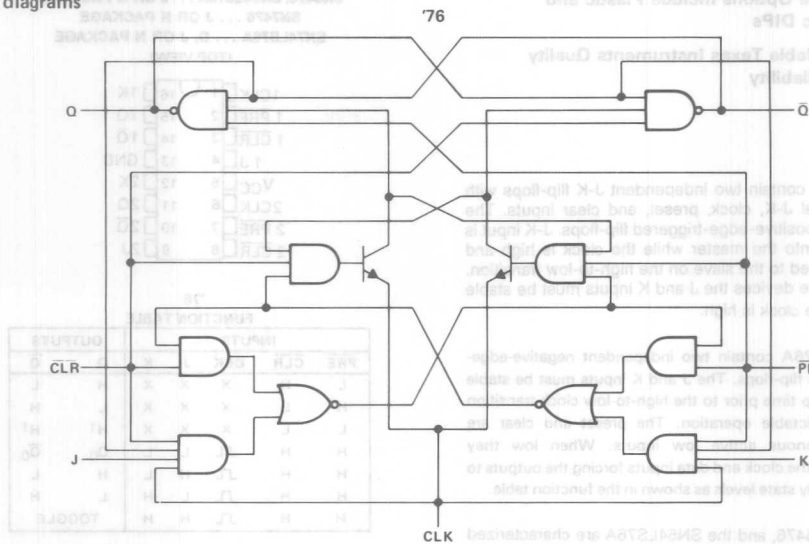
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TYPES SN5476, SN7476
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

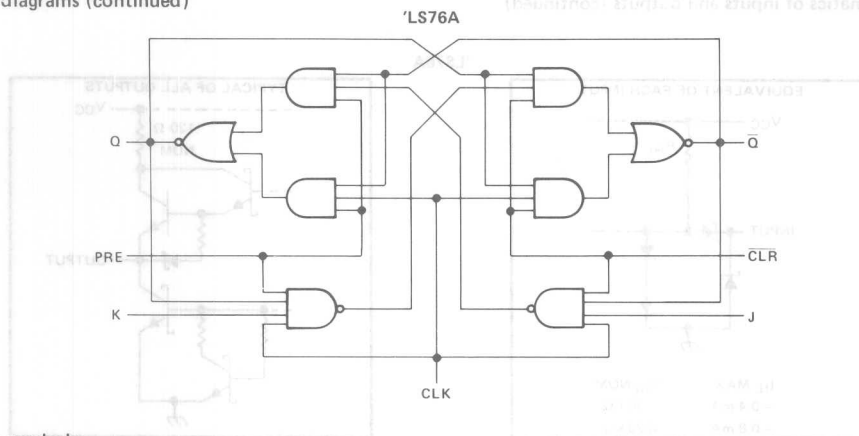
logic diagrams



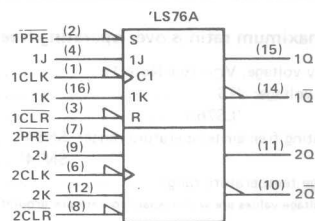
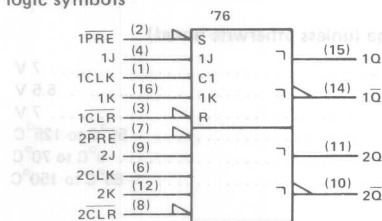
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**TYPES SN5476, SN54LS76A,
SN7476, SN74LS76A**
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

logic diagrams (continued)

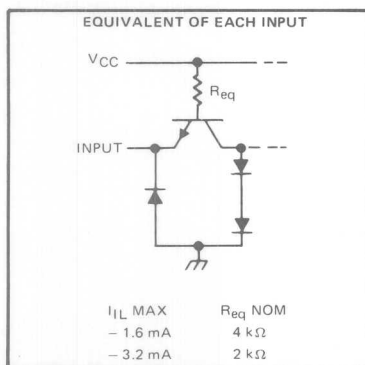


logic symbols

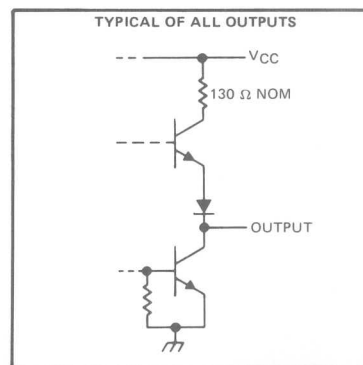


Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs

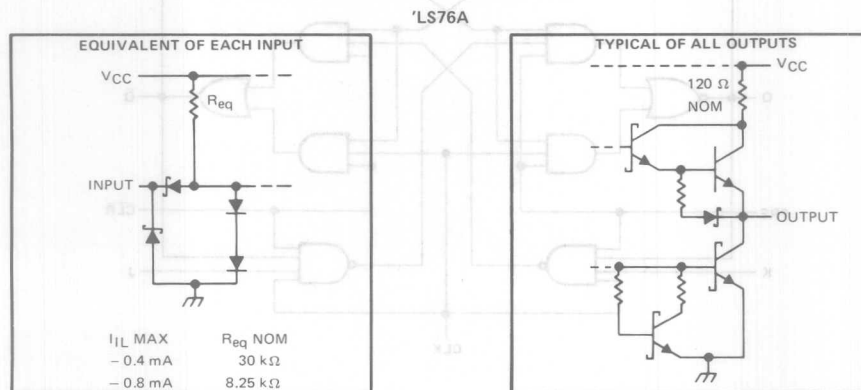


'76



3

TTL DEVICES



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '76	5.5 V
'LS76A	7 V
Operating free-air temperature range: SN54'	- 55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES



TYPES SN5476, SN7476 DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN5476			SN7476			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
t_W	Pulse duration	CLK high	20		20			ns
		CLK low	47		47			ns
		PRE or CLR low	25		25			ns
t_{SU}	Input setup time before CLK \uparrow	0			0			ns
t_H	Input hold time-data after CLK \downarrow	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		SN5476			SN7476			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -0.4 \text{ mA}$	$V_{IL} = 0.8 \text{ V}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 16 \text{ mA}, V_{IH} = 2 \text{ V}$	$V_{IL} = 0.8 \text{ V}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
I_{IH}	J or K All other	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	J or K All other*	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS}	$V_{CC} = \text{MAX}$		-20	-57		-18	-57		mA
I_{CC} Supply Current (average per Flip-Flop)	$V_{CC} = \text{MAX},$ See Note 2			10	20		10	20	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

*Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}					15	20		MHz
t_{PLH}	\bar{PRE} or \bar{CLR}	Q or \bar{Q}	$R_L = 400 \Omega, C_L = 15 \text{ pF}$			16	25	ns
t_{PHL}						25	40	ns
t_{PLH}	CLK	Q or \bar{Q}				16	25	ns
t_{PHL}						25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS76A, SN74LS76A
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS76A			SN74LS76A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.75	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		30	0		30	MHz
t _w	Pulse duration							ns
t _{su}	Setup time before CLK ↓	CLK high	20		20			ns
		PRE or CLR low	25		25			
		data high or low	20		20			
		CLR inactive	20		20			
t _h	Hold time-data after CLK ↓	PRE inactive	25		25			ns
			0		0			
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS76A			SN74LS76A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	J or K			0.1			0.1	mA
	CLR or PRE			0.3			0.3	
	CLK			0.4			0.4	
I _{IH}	J or K			20			20	μA
	CLR or PRE			60			60	
	CLK			80			80	
I _{IL}	J or K			-0.4			-0.4	mA
	All other			-0.8			-0.8	
I _{OS} §	V _{CC} = MAX, See Note 4	-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, See Note 2		4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{max}			R _L = 2 kΩ, C _L = 15 pF		30	45		MHz
t _{PLH}	PRE, CLR or CLK	Q or \bar{Q}			15	20		ns
t _{PHL}					15	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

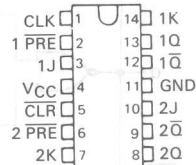
The 'LS78A contain two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and K inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN54LS78A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS78A is characterized for operation from 0°C to 70°C .

FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

SN54LS78A ... J OR W PACKAGE
SN74LS78A ... D, J OR N PACKAGE

(TOP VIEW)



'LS78A

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	\bar{Q}_0

[†] This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

3

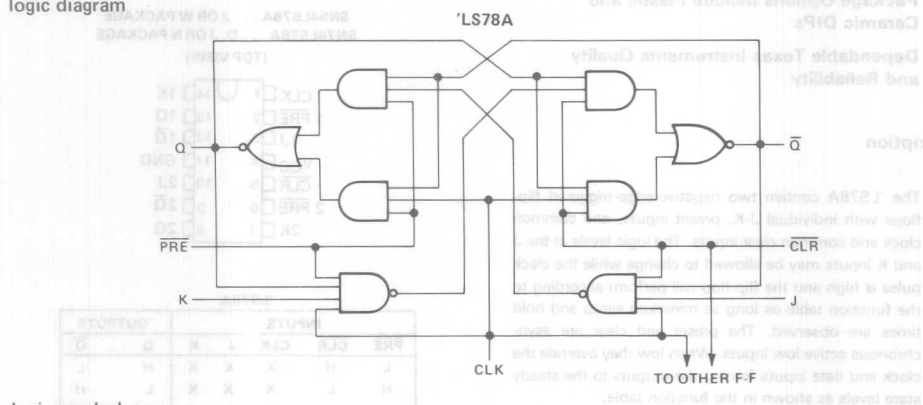
TTL DEVICES

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TEXAS
INSTRUMENTS

3-251

DUAL J-K FL



logic symbol

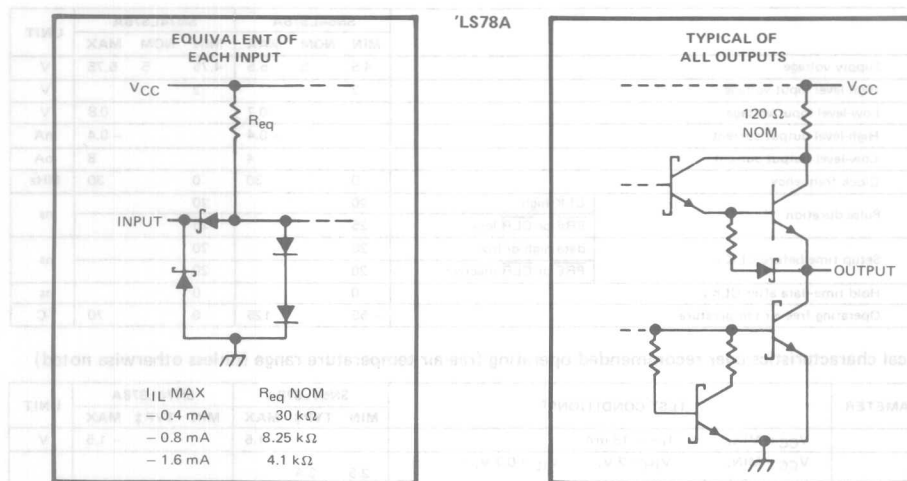
OUTPUT		INPUT					
D	C	K	L	M	N	PRES CLK	
H	H	X	X	X	X	L	
L	L	X	X	X	X	H	
H	H	X	X	X	X	L	
L	L	X	X	X	X	H	
H	L	L	L	L	L		CLK (1)
L	H	L	L	L	L		CLR (5)
H	L	L	L	L	L		1PRE (2)
L	H	L	L	L	L		J (3)

Pin numbers shown on logic notation are for D, J or N packages.

TTL DEVICES

TYPES SN54LS78A, SN74LS78A **DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR**

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS78A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

TYPES SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

recommended operating conditions

			SN54LS78A			SN74LS78A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				-0.4			-0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		PRE or CLR low	25			25			
t_{su}	Setup time before CLK \downarrow	data high or low	20			20			ns
		PRE or CLR inactive	20			20			
t_h	Hold time-data after CLK \downarrow		0			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS78A			SN74LS78A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4					V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$				2.7	3.4		
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	J or K		0.1	0.1		0.1		mA
	CLR		0.6	0.6		0.6		
	PRE		0.3	0.3		0.3		
	CLK		0.8	0.8		0.8		
I_{IH}	J or K		20	20		20		μA
	CLR		120	120		120		
	PRE		60	60		60		
	CLK		160	160		160		
I_{IL}	J or K		-0.4	-0.4		-0.4		mA
	CLR		-1.6	-1.6		-1.6		
	PRE		-0.8	-0.8		-0.8		
	CLK		-1.6	-1.6		-1.6		
$I_{OS}§$	$V_{CC} = \text{MAX},$ See Note 4	-20	-100	-100	-20	-100	-100	mA
I_{CC}	$V_{CC} = \text{MAX},$ See Note 2	4	6		4	6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3

TTL DEVICES

TYPES SN54LS78A, SN74LS78A
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max}			$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	30	45		MHz
t_{PLH}	$\overline{\text{PRE}}$, $\overline{\text{CLR}}$ or CLK	Q or \overline{Q}		15	20		ns
t_{PHL}				15	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

TYPES SNAL578A, SNAL578B

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROP. DEL. t_{PLH} PRE. CLR. @ CLK	Q = 0	Q = 1	$R_L = 1\text{ k}\Omega$ $C_L = 15\text{ pF}$	20	45		nS
				15	30		nS
				15	30		nS

NOTE 3: See General Information Section for test conditions and voltage waveforms.

3

TTL DEVICES

TYPES SN5482, SN7482

2-BIT BINARY FULL ADDERS

DECEMBER 1972—REVISED DECEMBER 1983

For applications in:

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

FUNCTION TABLE

INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
A1	B1	A2	B2	$\Sigma 1$	$\Sigma 2$	C2	$\Sigma 1$	$\Sigma 2$	C2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	H	L	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

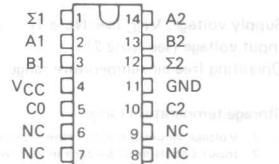
H = high level, L = low level

description

These full adders perform the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, these circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) and are compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

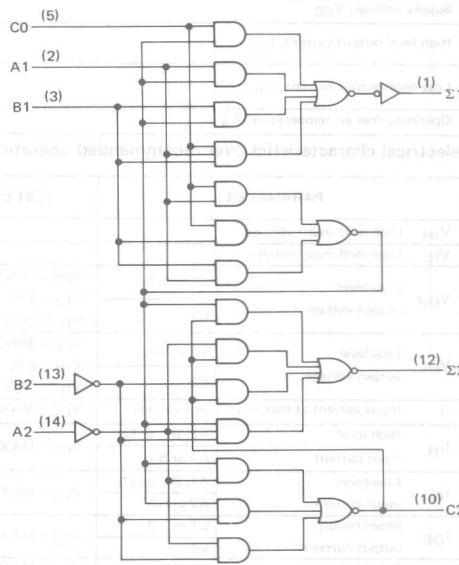
SN5482 . . . J OR W PACKAGE
SN7482 . . . J OR N PACKAGE

(TOP VIEW)



NC—No internal connection

logic diagram



Pin numbers shown on logic notation are for J or N packages.

3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN5482, SN7482 2-BIT BINARY FULL ADDERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5482 Circuits	-55°C to 125°C
SN7482 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN5482			SN7482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	$\Sigma 1$ or $\Sigma 2$			-400			-400	μA
	C2			-200			-200	
Low-level output current, I_{OL}	$\Sigma 1$ or $\Sigma 2$			16			16	mA
	C2			8			8	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5482			SN7482			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage	$\Sigma 1$ or $\Sigma 2$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.4 \text{ V}, I_{OH} = -400 \mu A$	2.4	3.4		2.4	3.4		V
		C2	$I_{OH} = -200 \mu A$							
V_{OL}	Low-level output voltage	$\Sigma 1$ or $\Sigma 2$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.4 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
		C2	$I_{OL} = 8 \text{ mA}$							
I_I	Input current at maximum input voltage		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	A1, B1, or C0	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			160			160	μA
		A2 or B2				40			40	
I_{IL}	Low-level input current	A1, B1, or C0	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-6.4			-6.4	mA
		A2 or B2				-1.6			-1.6	
I_{OS}	Short-circuit output current§	$\Sigma 1$ or $\Sigma 2$	$V_{CC} = \text{MAX}$			-20			-55	mA
		C2				-70			-70	
I_{CC}	Supply current		$V_{CC} = \text{MAX}, \text{ See Note 3}$			35			58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with outputs open, B1 and B2 grounded, and 4.5 V applied to A1, A2, and C0.

TYPES SN5482, SN7482 2-BIT BINARY FULL ADDERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 4)

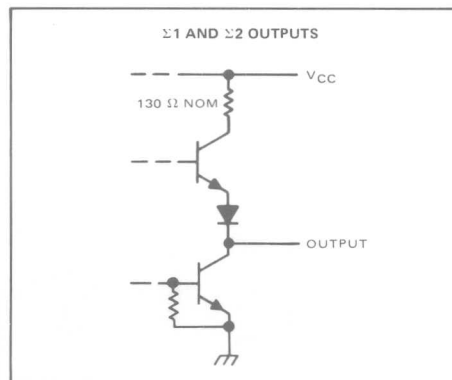
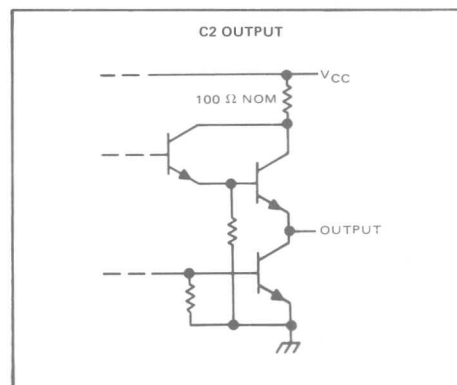
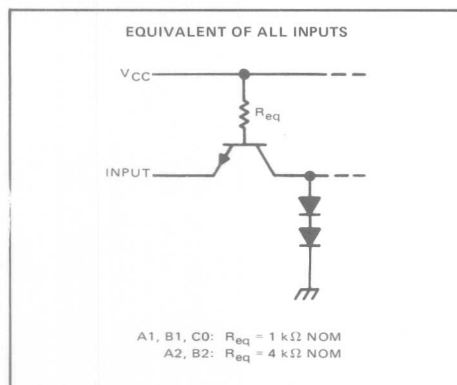
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	C0	Σ1	C _L = 15 pF, R _L = 400 Ω			34	ns
t _{PHL}						40	
t _{PLH}	B2	Σ2				40	ns
t _{PHL}						35	
t _{PLH}	C0	Σ2				38	ns
t _{PHL}						42	
t _{PLH}	C0	C2	C _L = 15 pF, R _L = 780 Ω		12	19	ns
t _{PHL}						17	

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



3
TTL DEVICES

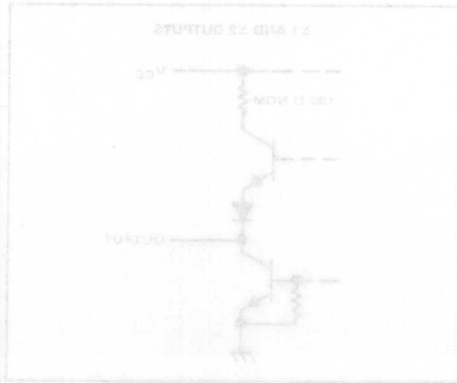
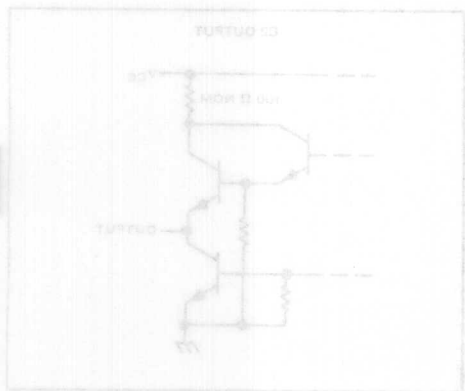
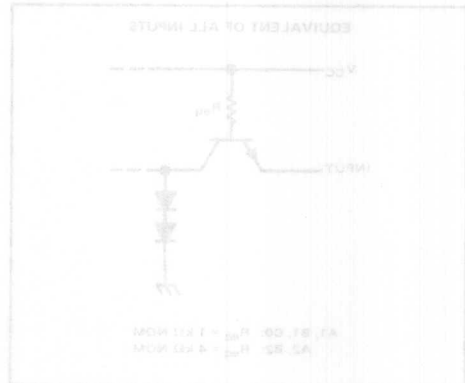
3-BIT BINARY FULL ADDERS TYPES SN6485, SN7485

Switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 4)

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	C0	Z1	$C_L = 15\text{ pF}$, $R_L = 100\ \Omega$	34		48	ns	
				43		58	ns	
t_{PHL}				43		58	ns	
t_{PLH}	B3	Z3		39		50	ns	
t_{PHL}				39		50	ns	
t_{PLH}	D0	Z3		43		58	ns	
t_{PHL}				43		58	ns	
t_{PLH}	C0	C3	$C_L = 15\text{ pF}$, $R_L = 100\ \Omega$	43		58	ns	
t_{PHL}				43		58	ns	

¹ t_{PLH} : propagation delay time low-to-high-level output
 t_{PHL} : propagation delay time high-to-low-level output
 NOTE 4: See general information section for load circuit and related information.

schematics of inputs and outputs



3 TTL DEVICES

TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A 4-BIT BINARY FULL ADDERS WITH FAST CARRY

MARCH 1974—REVISED DECEMBER 1983

- Full-Carry Look-Ahead across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- SN54283/SN74283 and SN54LS283/SN74LS283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout

TYPE	TYPICAL ADD TIMES		TYPICAL POWER DISSIPATION PER 4-BIT ADDER
	TWO 8-BIT WORDS	TWO 16-BIT WORDS	
'83A	23 ns	43 ns	310 mW
'LS83A	25 ns	45 ns	95 mW

description

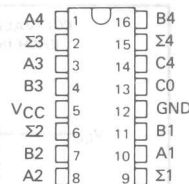
These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

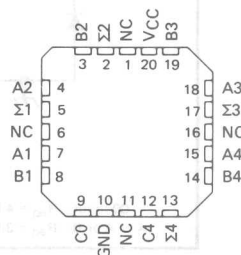
Designed for medium-speed applications, the circuits utilize transistor-transistor logic that is compatible with most other TTL families and other saturated low-level logic families.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C , and Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C .

SN5483A, SN54LS83A ... J OR W PACKAGE
SN7483A ... J OR N PACKAGE
SN74LS83A ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS83A ... FK PACKAGE
SN74LS83A
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUT										OUTPUT			
										WHEN C0 = L	WHEN C0 = H	WHEN C2 = L	WHEN C2 = H
A1	B1	A2	B2	A3	B3	A4	B4	Σ1	Σ2	C2	Σ1	Σ2	C2
L	L	L	L	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	H	L	L	L	L	L	L	H	L
L	H	L	L	L	L	H	L	L	L	L	L	H	L
H	H	L	L	L	L	H	H	L	L	L	L	H	L
L	L	H	L	L	L	H	L	L	H	L	H	H	L
H	L	H	L	L	H	H	L	L	L	L	L	L	H
L	H	H	L	L	L	H	H	L	L	L	H	L	H
H	H	H	L	L	L	L	H	L	H	H	L	H	L
L	L	L	H	L	L	H	L	L	H	L	H	H	L
H	L	L	H	L	H	H	L	L	L	L	L	L	H
L	H	L	H	L	H	H	H	L	L	L	L	L	H
H	H	L	H	L	L	L	H	L	H	H	L	L	H
L	L	H	H	L	L	L	L	L	L	H	H	L	H
H	L	H	H	L	H	H	L	L	L	H	L	H	H
L	H	H	H	L	L	L	L	L	L	L	L	H	H
H	H	H	H	L	L	L	L	L	L	L	L	H	H

H = high level, L = low level

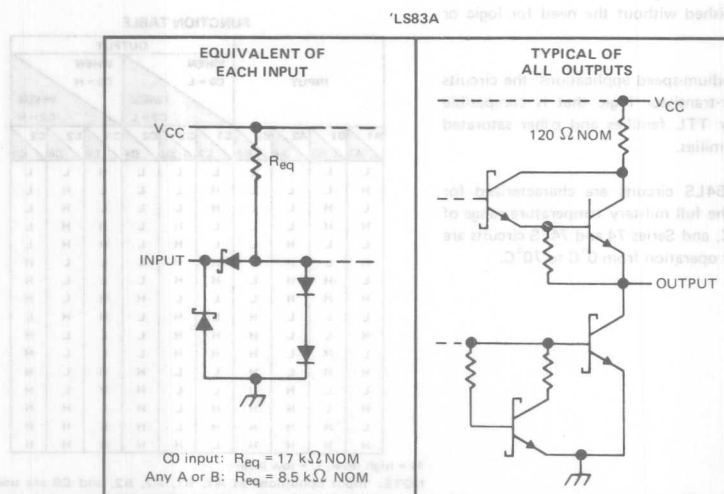
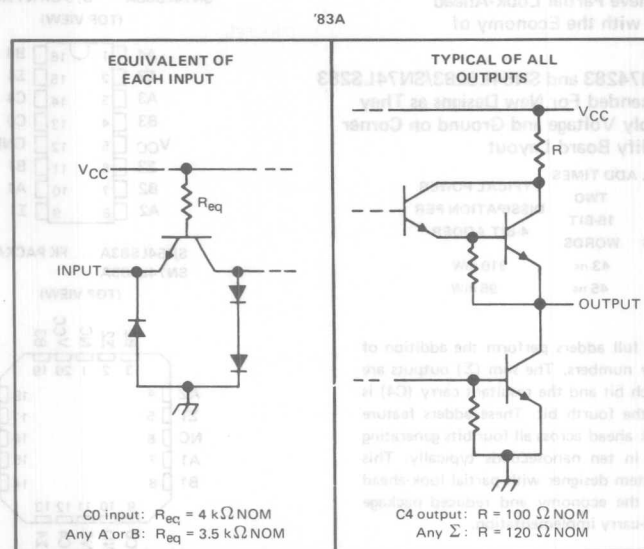
NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

PRODUCTION DATA
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TEXAS
INSTRUMENTS

TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A 4-BIT BINARY FULL ADDERS WITH FAST CARRY

schematics of inputs and outputs

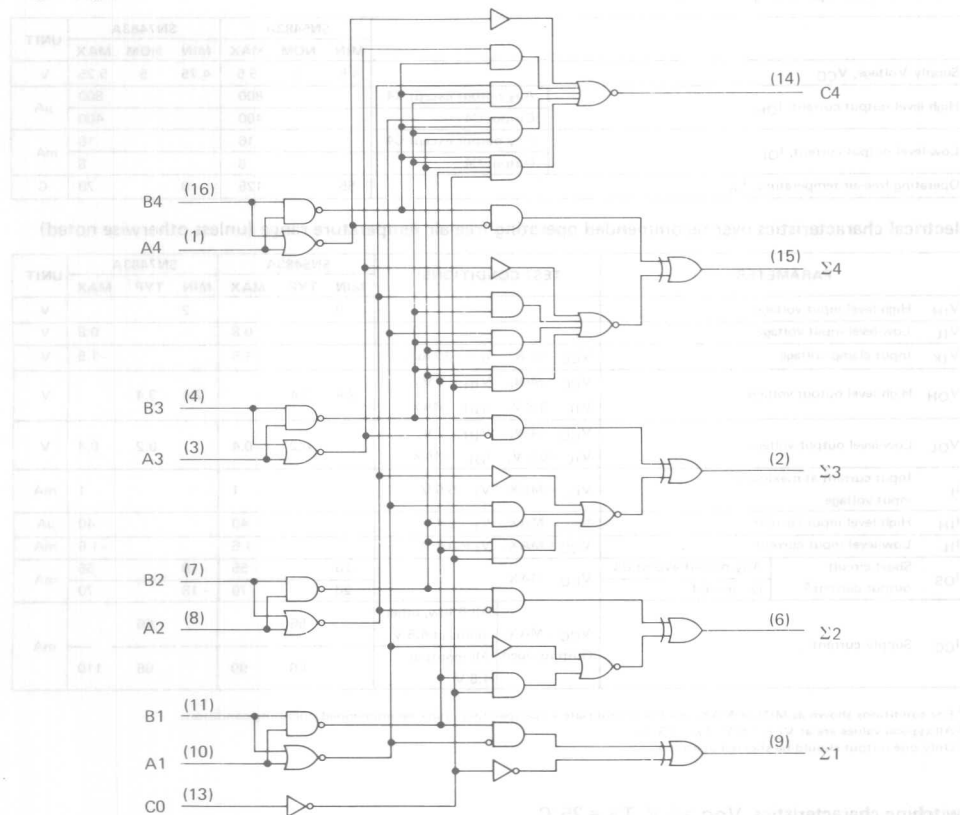


3

TTL DEVICES

TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A 4-BIT BINARY FULL ADDERS WITH FAST CARRY

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '83A	5.5 V
'LS83A	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5483A, SN54LS83A	-55°C to 125°C
SN7483A, SN74LS83A	0°C to 70°C
Storage temperature range	65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '83A only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

TYPES SN5483A, SN7483A 4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

		SN5483A			SN7483A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	Any output except C4	800			800			μA
	Output C4	400			400			
Low-level output current, I _{OL}	Any output except C4	16			16			mA
	Output C4	8			8			
Operating free-air temperature, T _A		-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5483A			SN7483A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.8			0.8			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.5			-1.5			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$	0.2	0.4		0.2	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	40			40			μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-1.6			-1.6			mA
I_{OS}	Short-circuit output current‡	Any output except C4	$V_{CC} = \text{MAX}$			$V_{CC} = \text{MAX}$			mA
		Output C4	-20	-55	-18	-20	-55	-18	
I_{CC}	Supply current	All B low, other inputs at 4.5 V	56			56			mA
		All inputs at 4.5 V	66	99		66	110		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	C0	Any Σ	C _L = 15 pF, R _L = 400 Ω, See Note 3	14	21	ns	
t _{PHL}				12	21		
t _{PLH}	A _i or B _i	Σ _i		16	24	ns	
t _{PHL}				16	24		
t _{PLH}	C0	C4	C _L = 15 pF, R _L = 780 Ω, See Note 3	9	14	ns	
t _{PHL}				11	16		
t _{PLH}	A _i or B _i	C4		9	14	ns	
t _{PHL}				11	16		

¶ t_{PLH} Propagation delay time, low to high level output

t_{PHL} Propagation delay time, high to low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms

3
TTL DEVICES

TYPES SN54LS83A, SN74LS83A 4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

	SN54LS83A			SN74LS83A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS83A			SN74LS83A			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage			2			2		V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I	Input current at maximum input voltage	Any A or B			0.2			0.2	mA
		C0			0.1			0.1	
I_{IH}	High-level input current	Any A or B			40			40	μ A
		C0			20			20	
I_{IL}	Low-level input current	Any A or B			-0.8			-0.8	mA
		C0			-0.4			-0.4	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC}	Supply current	All inputs grounded	22		39	22		39	mA
		All B low, other inputs at 4.5 V	19		34	19		34	
		All inputs at 4.5 V	19		34	19		34	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

[§] Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
[†] PLH	C0	Any Σ	CL = 15 pF, See Note 4	RL = 2 k Ω , See Note 4		16	24	ns
[†] PHL						15	24	
[†] PLH	Ai or Bi	Σ_i				15	24	ns
[†] PHL						15	24	
[†] PLH	C0	C4				11	17	ns
[†] PHL						15	22	
[†] PLH	Ai or Bi	C4				11	17	ns
[†] PHL						12	17	

[¶] t_{PLH} Propagation delay time, low to high level output

t_{PHL} Propagation delay time, high to low level output

Note 4: See General Information Section for load circuits and voltage waveforms

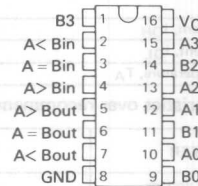
3

TTL DEVICES

TYPES SN5485, SN54LS85, SN54S85, SN7485, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS MARCH 1974 REVISED DECEMBER 1983

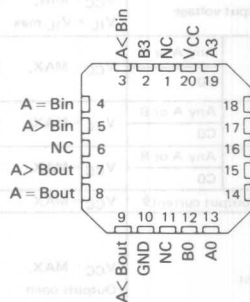
TYPE	POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'LS85	52 mW	24 ns
'S85	365 mW	11 ns

SN5485, SN54LS85, SN54S85 ... J OR W PACKAGE
SN7485 ... J OR N PACKAGE
SN74LS85, SN74S85 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS85, SN54S85 ... FK PACKAGE
SN74LS85, SN74S85

(TOP VIEW)



NC - No internal connection

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 < B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 < B3	A2 < B2	X	X	X	X	X	H	L	L
A3 < B3	A2 < B2	X	X	X	X	X	L	H	L
A3 < B2	A2 < B2	A1 < B1	X	X	X	X	H	L	L
A3 < B3	A2 < B2	A1 < B1	X	X	X	X	L	H	L
A3 < B3	A2 < B2	A1 < B1	A0 < B0	X	X	X	H	L	L
A3 < B3	A2 < B2	A1 < B1	A0 < B0	X	X	X	L	H	L
A3 < B3	A2 < B2	A1 < B1	A0 < B0	H	L	L	H	L	L
A3 < B3	A2 < B2	A1 < B1	A0 < B0	L	H	L	L	H	L
A3 < B3	A2 < B2	A1 < B1	A0 < B0	L	L	H	L	L	H

'85, 'LS85, 'S85

A3 < B3	A2 < B2	A1 < B1	A0 < B0	X	X	H	L	L	H
A3 < B3	A2 < B2	A1 < B1	A0 < B0	H	H	L	L	L	L
A3 < B3	A2 < B2	A1 < B1	A0 < B0	L	L	L	H	H	L

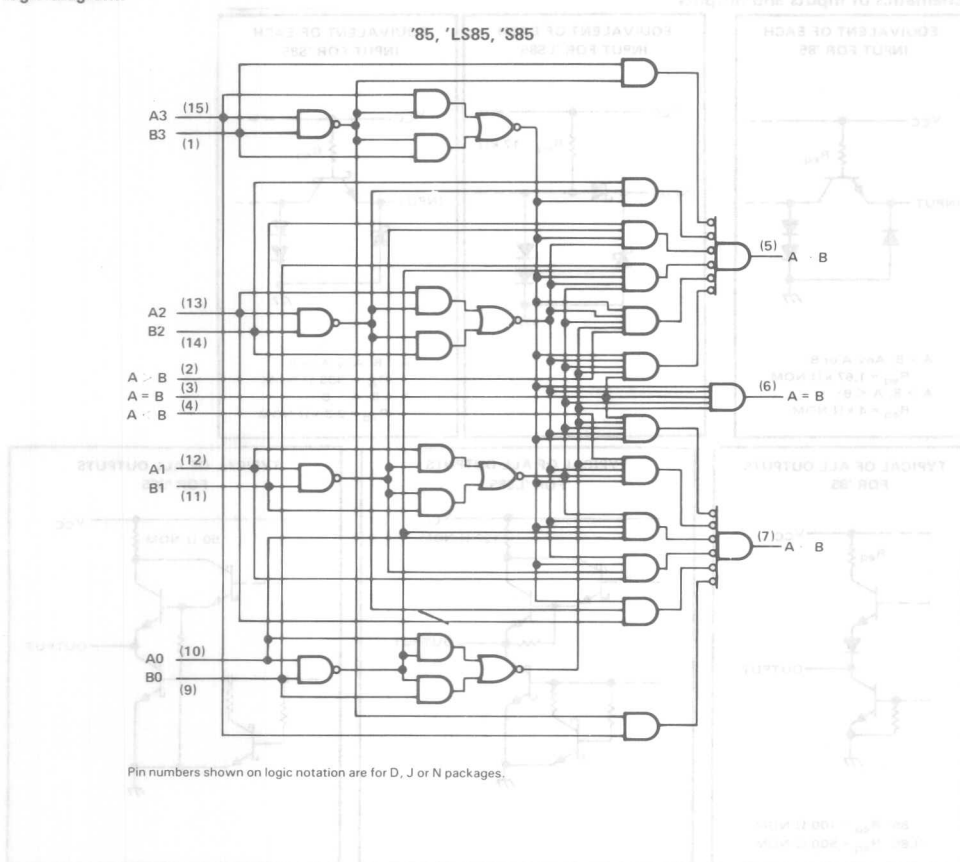
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

**TYPES SN5485, SN54LS85, SN54S85,
SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS**

logic diagram.

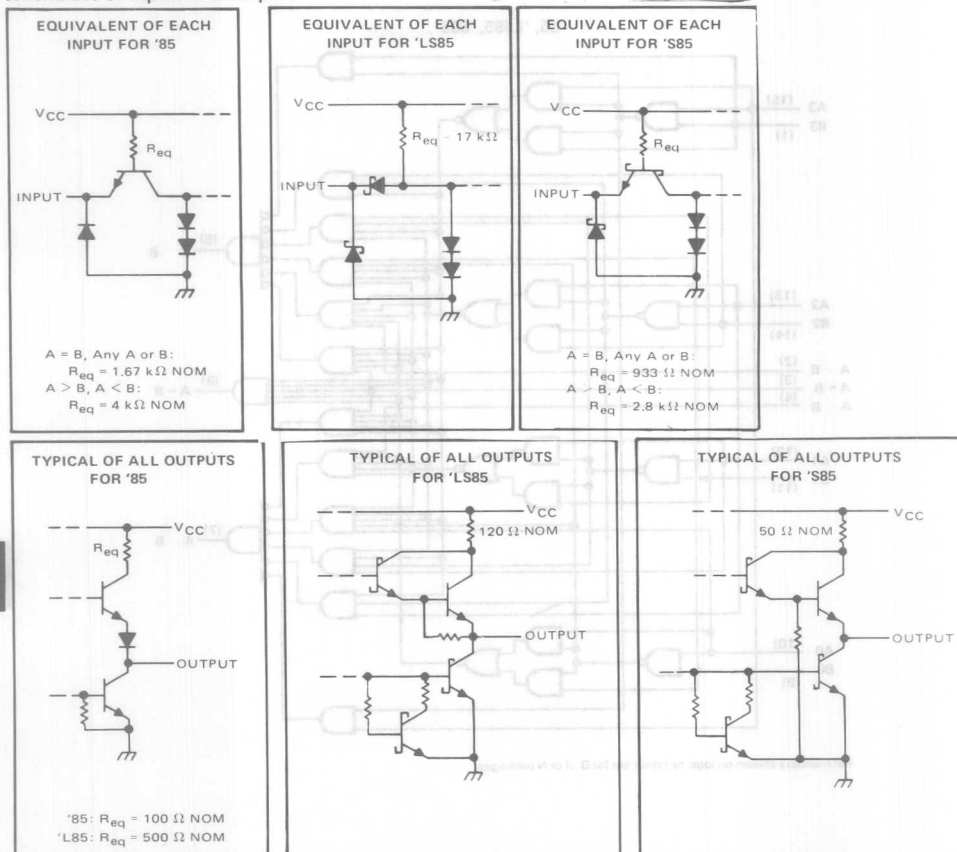


absolute maximum ratings over operating temperature range (unless otherwise noted)

PARAMETER	MINIMUM	MAXIMUM	UNIT
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C
Input voltage	-0.5	5.5	V
Output voltage	-0.5	5.5	V
Input current	-1	1	mA
Output current	-1	1	mA

**TYPES SN5485, SN54LS85, SN54S85,
SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS**

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'		SN54LS'	SN74'	SN74LS'	UNIT
	SN54S'			SN74S'		
Supply voltage, V_{CC} (see Note 1)	7		7	7	7	V
Input voltage	5.5		7	5.5	7	V
Interemitter voltage (see Note 2)	5.5			5.5		V
Operating free-air temperature range		-55 to 125		-0 to 70		$^{\circ}\text{C}$
Storage temperature range		-65 to 150		-65 to 150		$^{\circ}\text{C}$

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A_i input in conjunction with its respective B input of the '85 and 'S85.

3

TTL DEVICES

TYPES SN5485, SN7485 4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$A < B, A > B$ inputs all other inputs $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40	μ A
I_{IL}	Low-level input current	$A < B, A > B$ inputs all other inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-1.6	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}, V_O = 0$	SN5485	-20		-55	mA
			SN7485	-18		-55	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 4			.55	88	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with outputs open, $A = B$ grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	$A < B, A > B$	1	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 5		7		ns
			2			12		
			3			17	26	
		$A = B$	4			23	35	ns
t_{PHL}	Any A or B data input	$A < B, A > B$	1			11		
			2			15		
			3			20	30	
		$A = B$	4			20	30	
t_{PLH}	$A < B$ or $A = B$	$A > B$	1			7	11	ns
t_{PHL}	$A < B$ or $A = B$	$A > B$	1			11	17	ns
t_{PLH}	$A = B$	$A = B$	2			13	20	ns
t_{PHL}	$A = B$	$A = B$	2			11	17	ns
t_{PLH}	$A > B$ or $A = B$	$A < B$	1			7	11	ns
t_{PHL}	$A > B$ or $A = B$	$A < B$	1			11	17	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 5: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS85, SN74LS85 4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN54LS85			SN74LS85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS85			SN74LS85			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	Input current at maximum input voltage	$A < B, A > B \text{ inputs}$			0.1			0.1	mA
		all other inputs			0.3			0.3	
I_{IH}	High-level input current	$A < B, A > B \text{ inputs}$			20			20	μ A
I_{IL}	Low-level input current	all other inputs			60			60	mA
		$A < B, A > B \text{ inputs}$			-0.4			-0.4	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 4}$	10.4	20		10.4	20		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	$A < B, A > B$	1	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 5}$		14		ns
			2			19		
			3			24	36	
		$A = B$	4			27	45	ns
t_{PHL}	Any A or B data input	$A < B, A > B$	1			11		
			2			15		
			3			20	30	
		$A = B$	4			23	45	ns
t_{PLH}	$A < B \text{ or } A = B$	$A > B$	1			14	22	
t_{PHL}	$A < B \text{ or } A = B$	$A > B$	1			11	17	ns
t_{PLH}	$A = B$	$A = B$	2			13	20	ns
t_{PHL}	$A = B$	$A = B$	2			13	26	ns
t_{PLH}	$A > B \text{ or } A = B$	$A < B$	1			14	22	ns
t_{PHL}	$A > B \text{ or } A = B$	$A < B$	1			11	17	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 5: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S85, SN74S85 4-BIT MAGNITUDE COMPARATORS

recommended operating conditions

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -1 \text{ mA}$	SN54S85 2.5 SN74S85 2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	A < B, A > B inputs			50	μA
		all other inputs			150	
I_{IL}	Low-level input current	A < B, A > B inputs			-2	mA
		all other inputs			-6	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 4		73	115	mA
		$V_{CC} = \text{MAX}$, $T_A = 125^\circ\text{C}$, See Note 4	SN54S85W		110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, See Note 5		5		ns
			2			7.5		
			3			10.5	16	
		A = B	4			12	18	
t_{PHL}	Any A or B data input	A < B, A > B	1			5.5		ns
			2			7		
			3			11	16.5	
		A = B	4			11	16.5	
t_{PLH}	A < B or A = B	A > B	1			5	7.5	ns
t_{PHL}	A < B or A = B	A > B	1			5.5	8.5	ns
t_{PLH}	A = B	A = B	2			7	10.5	ns
t_{PHL}	A = B	A = B	2			5	7.5	ns
t_{PLH}	A > B or A = B	A < B	1			5	7.5	ns
t_{PHL}	A > B or A = B	A < B	1			5.5	8.5	ns

¶ t_{PLH} propagation delay time, low-to-high-level output

¶ t_{PHL} propagation delay time, high-to-low-level output

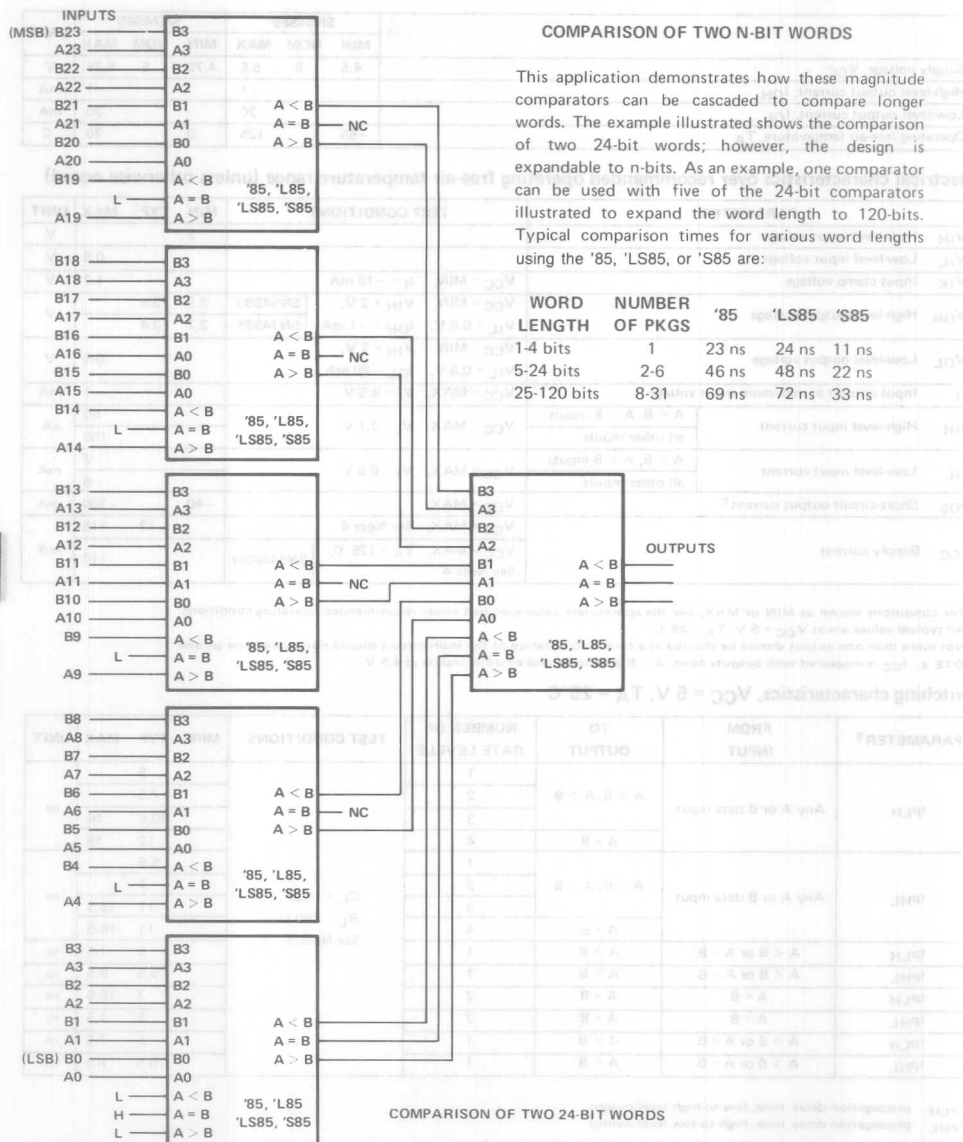
NOTE 5: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

**TYPES SN5485, SN54LS85, SN54S85,
SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS**

TYPICAL APPLICATION DATA



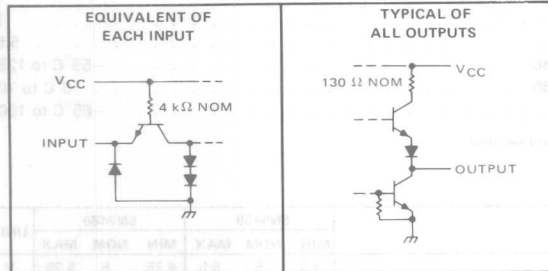
3 TTL DEVICES

**TYPES SN5486, SN54LS86A, SN54S86,
SN7486, SN74LS86A, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

DECEMBER 1972 - REVISED DECEMBER 1983

schematics of inputs and outputs

'86

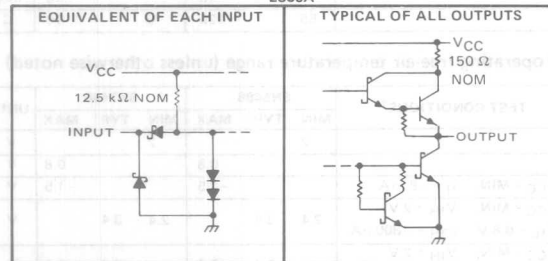


SN5486, SN54LS86A, SN54S86 ... J OR W PACKAGE
SN7486 ... J OR N PACKAGE
SN74LS86A, SN74S86 ... D, J OR N PACKAGE

(TOP VIEW)

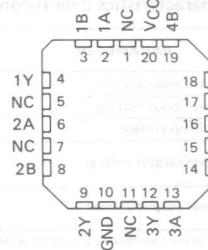


'LS86A



SN54LS86A, SN54S86 ... FK PACKAGE
SN74LS86A, SN74S86

(TOP VIEW)



NC - No internal connection

FUNCTION TABLES

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

TYPE

'86
'LS86A
'S86

H = high level, L = low level

TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
14 ns	150 mW
10 ns	30.5 mW
7 ns	250 mW

3

TTL DEVICES

PRODUCTION DATA

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TEXAS
INSTRUMENTS

TYPES SN5486, SN7486

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5486	-55°C to 125°C
SN7486	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5486			SN7486			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5486			SN7486			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	30	43		30	50		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Note 3}$	15	23		ns
t_{PHL}				11	17		
t_{PLH}	A or B	Other input high		18	30		ns
t_{PHL}				13	22		

¶ t_{PLH} = propagation delay time, low to high level output

t_{PHL} = propagation delay time, high to low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS86A, SN74LS86A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS86A	–55°C to 125°C
SN74LS86A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS86A			SN74LS86A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS86A			SN74LS86A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$		–1.5			–1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \text{ μA}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.2			0.2		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		40			40		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		–0.8			–0.8		mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–20	–100	100	–20	100	100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	6.1	10		6.1	10		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low $C_L = 15 \text{ pF}$		12	23	ns
t_{PHL}	A or B	Other input high $R_L = 2 \text{ k}\Omega$		10	17	ns
t_{PLH}	A or B	See Note 3		20	30	ns
t_{PHL}	A or B	See Note 3		13	22	ns

† t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

3 TTL DEVICES A392 TYPES SN54S86, SN74S86QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S86	-55°C to 125°C
SN74S86	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S86			SN74S86			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50			50		µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2			-2		mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40	-100		-40	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		50	75		50	75	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Other input low	C _L = 15 pF, R _L = 280 Ω, See Note 3		7	10.5	ns
t _{PHL}					6.5	10	
t _{PLH}	A or B	Other input high			7	10.5	ns
t _{PHL}					6.5	10	

¶ t_{PLH} propagation delay time, low to high level output

t_{PHL} propagation delay time, high to low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

MARCH 1974 — REVISED DECEMBER 1983

'90A, 'LS90 ... DECADE COUNTERS

'92A, 'LS92 ... DIVIDE-BY-TWELVE COUNTERS

'93A, 'LS93 ... 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, and 'LS93.

All of these counters have a gated zero reset and the '90A, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

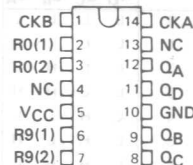
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A .

SN5490A, SN54LS90 ... J OR W PACKAGE

SN7490A ... J OR N PACKAGE

SN74LS90 ... D, J OR N PACKAGE

(TOP VIEW)



SN5492A, SN54LS92 ... J OR W PACKAGE

SN7492A ... J OR N PACKAGE

SN74LS92 ... D, J OR N PACKAGE

(TOP VIEW)



SN5493A, SN54LS93 ... J OR W PACKAGE

SN7493A ... J OR N PACKAGE

SN74LS93 ... D, J OR N PACKAGE

(TOP VIEW)



For new chip carrier design, use

'LS290, 'LS292, and 'LS293.

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TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-277

**TYPES SN5490A, '92A, '93A, SN54LS90, 'LS92, 'LS93,
SN7490A, '92A, '93A SN74LS90, 'LS92, 'LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

'90A, 'LS90

**BCD COUNT SEQUENCE
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'92A, 'LS92

**COUNT SEQUENCE
(See Note C)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

**'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE**

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

- NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKB for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

'90A, 'LS90

**BI-QUINARY (5-2)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'LS90

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	H
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	X	COUNT			
X	L	L	X	COUNT			

'93A, 'LS93

**COUNT SEQUENCE
(See Note C)**

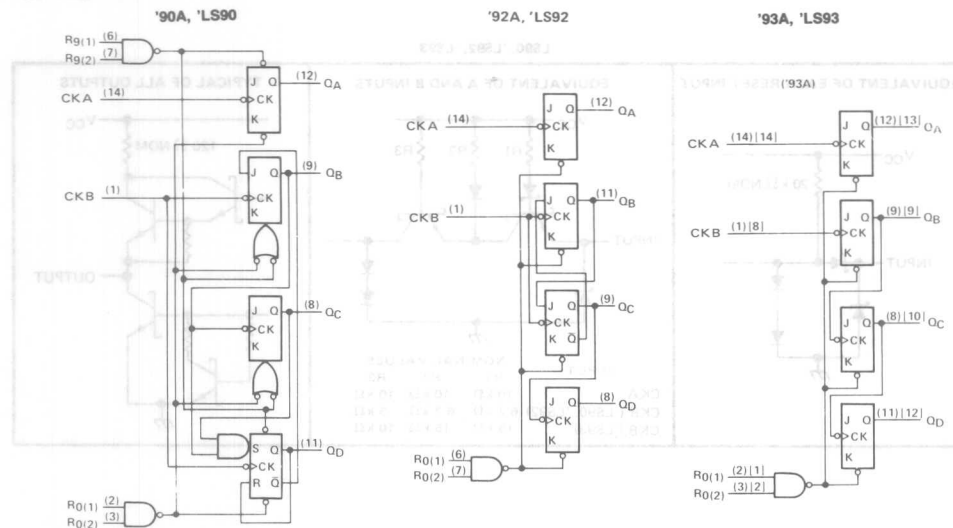
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

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TTL DEVICES

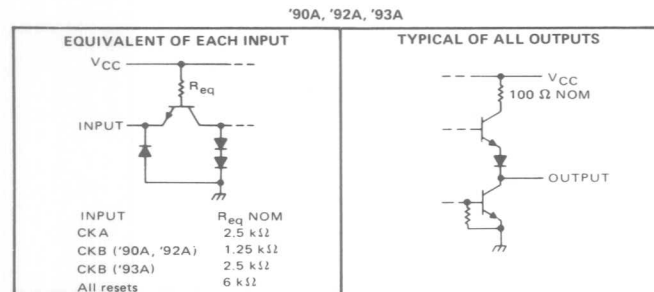
**TYPES SN5490A, '92A, '93A, SN54LS90, 'LS92, 'LS93,
SN7490A, '92A, '93A, SN74LS90, 'LS92, 'LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

logic diagrams



The J and K inputs shown without connection are for reference only and are functionally at a high level.

schematics of inputs and outputs

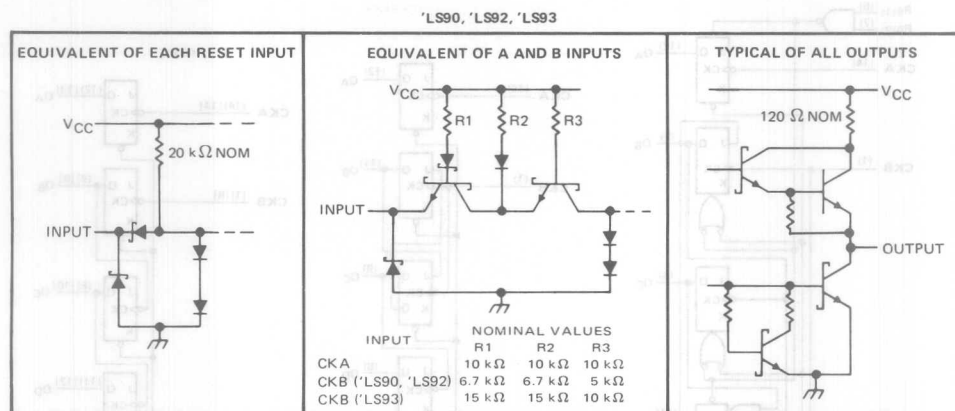


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TTL DEVICES

TYPES SN54LS90, 'LS92, 'LS93
SN74LS90, 'LS92, 'LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

schematics of inputs and outputs (continued)



3

TTL DEVICES



TYPES SN5490A, SN5492A, SN5493A, SN7490A, SN7492A, SN7493A DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A	-55°C to 125°C
SN7490A, SN7492A, SN7493A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_0 inputs.

recommended operating conditions

		SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER [†]		TEST CONDITIONS [‡]		'90A		'92A		'93A		UNIT
				MIN	TYP [§]	MAX	MIN	TYP [§]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4	2.4	3.4	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}^*$	0.2	0.4		0.2	0.4	0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1				1	mA
I_{IH}	High-level input current	Any reset			40				40	μ A
		CKA	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		80				80	
		CKB			120				120	
I_{IL}	Low-level input current	Any reset			-1.6				-1.6	mA
		CKA	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-3.2				-3.2	
		CKB			-4.8				-4.8	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54 [*]	-20	-57	-20	-57	-20	-57	mA
			SN74 [*]	-18	-57	-18	-57	-18	-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3		29	42		26	39		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time.

^{*} I_{OL} outputs are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

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TTL DEVICES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ^f	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{m,x}	CKA	O _A	C _L = 15 pF, R _L = 400 Ω, See Figure 1	32	42		32	42		32	42		MS	
	CKB	O _B		16			16			16				
t _{PLH}	CKA	O _A			10	16		10	16		10	16		ns
t _{PHL}					12	18		12	18		12	18		
t _{PLH}	CKA	O _D			32	48		32	48		46	70		ns
t _{PHL}					34	50		34	50		46	70		
t _{PLH}	CKB	O _B			10	16		10	16		10	16		ns
t _{PHL}					14	21		14	21		14	21		
t _{PLH}	CKB	O _C			21	32		10	16		21	32		ns
t _{PHL}					23	35		14	21		23	35		
t _{PLH}	CKB	O _D			21	32		21	32		34	51		ns
t _{PHL}					23	35		23	35		34	51		
t _{PHL}	Set-to-0	Any			26	40		26	40		26	40		ns
t _{PLH}	Set-to-9	O _A , O _D			20	30								ns
t _{PHL}				O _B , O _C		26	40							

f_{\max}	maximum count frequency
t_{PLH}	propagation delay time, low to high level output
t_{PHL}	propagation delay time, high to low level output

3

TTL DEVICES

**TYPES SN54LS90, SN54LS92, SN54LS93,
SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS [†] Circuits	−55°C to 125°C
SN74LS [†] Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

		SN54LS90			SN74LS90			UNIT
		SN54LS92			SN74LS92			
		SN54LS93			SN74LS93			
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μA
Low-level output current, I_{OL}		4			8			mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_W	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{SU}		25			25			ns
Operating free-air temperature, T_A		-55			125			$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS90 SN54LS92		SN74LS90 SN74LS92		UNIT			
				MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V _{IH}	High-level input voltage					2		V			
V _{IL}	Low-level input voltage					0.7		V			
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA			-1.5		V			
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4	V		
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 4 mA¶ I _{OL} = 8 mA¶		0.25	0.4		0.25	0.4	V	
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA		
		CKA			0.2		0.2				
		CKB	V _{CC} = MAX, V _I = 5.5 V		0.4		0.4				
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V			20		20	µA		
		CKA			40		40				
		CKB			80		80				
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA		
		CKA			-2.4		-2.4				
		CKB			-3.2		-3.2				
I _{OS}	Short-circuit output current§		V _{CC} = MAX	-20		-100	-20		-100	mA	
I _{CC}	Supply current		V _{CC} = MAX, See Note 3	'LS90		9	15		9	15	mA
				'LS92		9	15		9	15	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

†All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

⁴ Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

**TYPES SN54LS90, SN54LS92, SN54LS93,
SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS93			SN74LS93			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}^{\S}$	0.25	0.4		0.25	0.4		V
	$V_{IL} = V_{IL} \text{ max}, I_{OL} = 8 \text{ mA}^{\S}$				0.35	0.5		
I_I Input current at maximum input voltage	Any reset			0.1			0.1	mA
	CKA or CKB			0.2			0.2	
I_{IH} High-level input current	Any reset		20			20		μA
	CKA or CKB		40			80		
I_{IL} Low-level input current	Any reset		-0.4			-0.4		mA
	CKA		-2.4			-2.4		
	CKB		-1.6			-1.6		
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3	9	15		9	15		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_Q inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS92			'LS93			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CKA	Q_A	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$ See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A		10	16		10	16		10	16		ns
t_{PHL}				12	18		12	18		12	18		
t_{PLH}	CKA	Q_D		32	48		32	48		46	70		ns
t_{PHL}				34	50		34	50		46	70		
t_{PLH}	CKB	Q_B		10	16		10	16		10	16		ns
t_{PHL}				14	21		14	21		14	21		
t_{PLH}	CKB	Q_C		21	32		10	16		21	32		ns
t_{PHL}				23	35		14	21		23	35		
t_{PLH}	CKB	Q_D		21	32		21	32		34	51		ns
t_{PHL}				23	35		23	35		34	51		
t_{PHL}	Set to 0	Any		26	40		26	40		26	40		ns
t_{PLH}	Set to 9	Q_A, Q_D	20	30								ns	
t_{PHL}		Q_B, Q_C	26	40									

[¶] f_{max} maximum count frequency

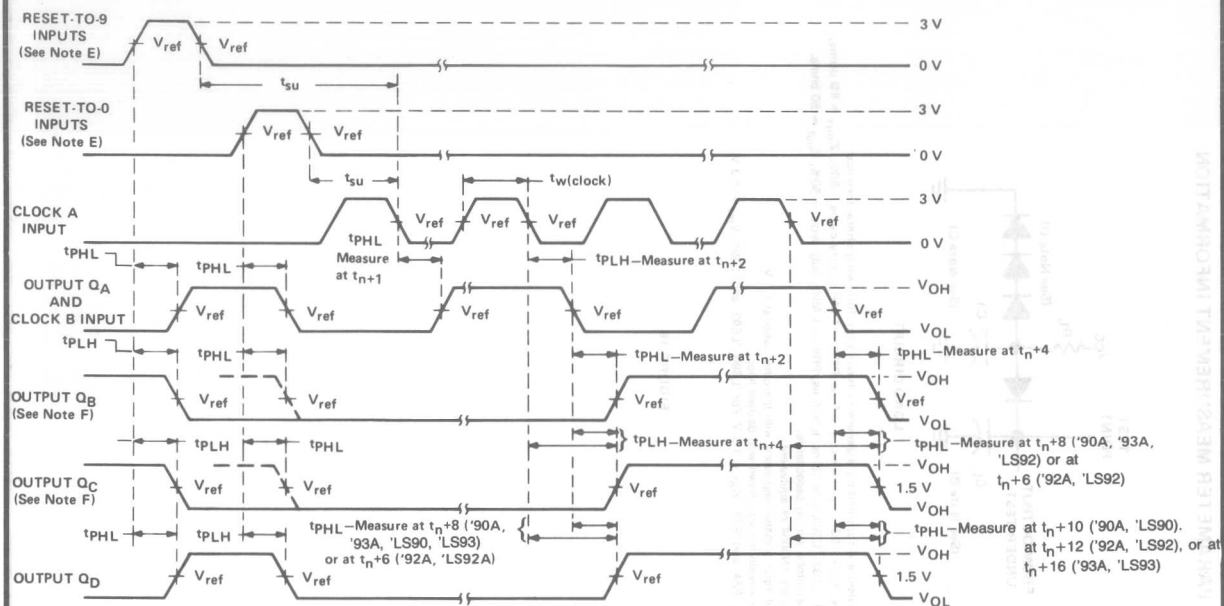
t_{PLH} propagation delay time, low to high level output

t_{PHL} propagation delay time, high to low level output

3

TTL DEVICES

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

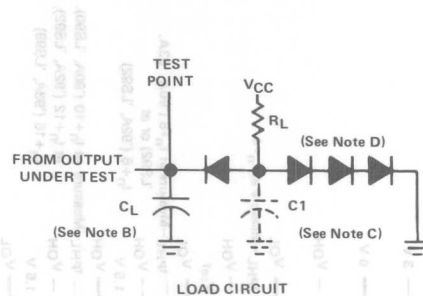
FIGURE 1A

TTL DEVICES



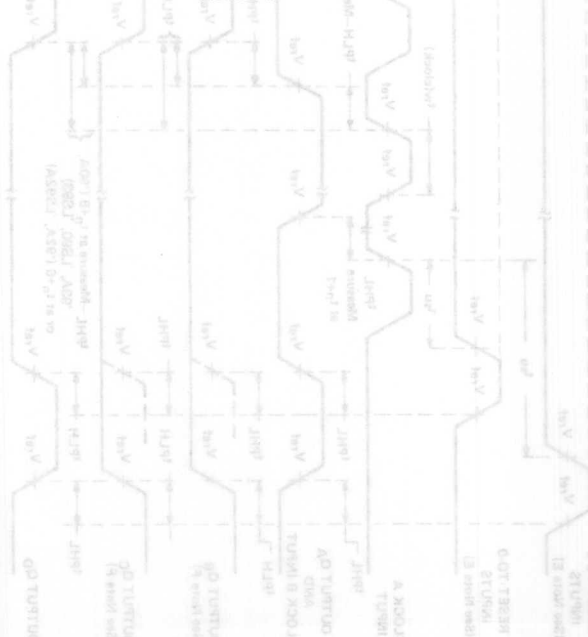
**TYPES SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92,
SN54LS93, SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. For '90A, '92A, and '93A: $V_{ref} = 1.5$ V. For 'LS90, 'LS92, and 'LS93: $V_{ref} = 1.3$ V.

FIGURE 1B



TYPES SN54LS91, SN74LS91 8-BIT SHIFT REGISTERS

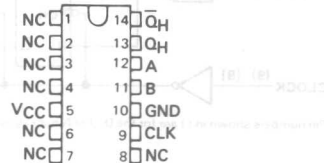
MARCH 1974 — REVISED DECEMBER 1983

- For applications in:
Digital Computer Systems
Data-Handling Systems
Control Systems

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'LS91	18 MHz	60 mW

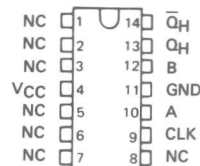
SN54LS91 ... J PACKAGE
SN74LS91 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS91 ... W PACKAGE

(TOP VIEW)



NC - No internal connection

description

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

FUNCTION TABLE

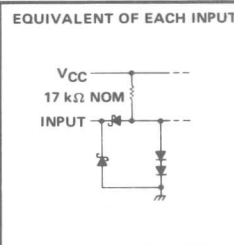
INPUTS AT t_n		OUTPUTS AT $t_n + 8$	
A	B	Q_H	\bar{Q}_H
H	H	H	L
L	X	L	H
X	L	L	H

t_n = Reference bit time,
clock low

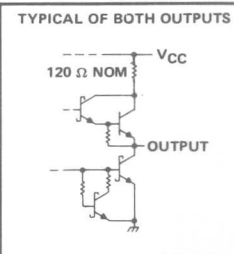
$t_n + 8$ = Bit time after 8
low-to-high
clock transitions.

schematics of inputs and outputs

'LS91



'LS91



3

TTL DEVICES

PRODUCTION DATA

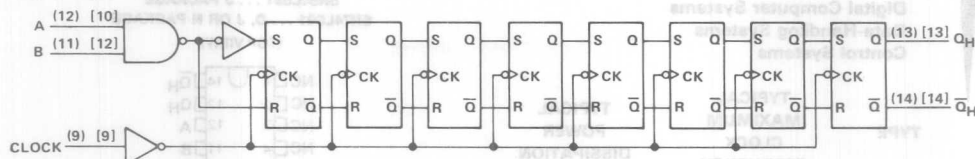
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-287

TYPES SN54LS91A, SN74LS91A 8-BIT SHIFT REGISTERS

logic diagram



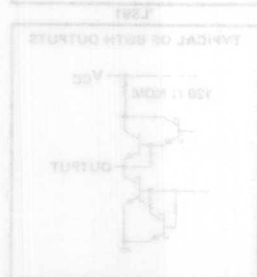
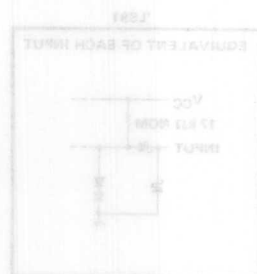
Pin numbers shown in () are for the D, J or N packages and pin numbers shown in | | are for the W package.

SN54LS91A W PACKAGE



NC - no internal connection

symbolic of inputs and outputs



These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuitry and are composed of eight D-type master-slave flip-flops. Input control is gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes three circuits to shift information one bit on the positive edge of an input clock pulse.

FUNCTION TABLE

INPUTS		OUTPUTS	
A	B	Q1	Q2
H	H	H	H
H	L	X	L
L	L	L	L

H = Reference pin time.
L = Logic low.
X = Bit time delay.
low-to-high
clock transitions

3

TTL DEVICES

TYPES SN54LS91, SN74LS91 **8-BIT SHIFT REGISTERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS91	-55°C to 125°C
SN74LS91	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS91			SN74LS91			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of clock input pulse, t_W	25			25			ns
Setup time, t_{su} (see Figure 1)	25			25			ns
Hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS91			SN74LS91			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$	12		20	12		20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

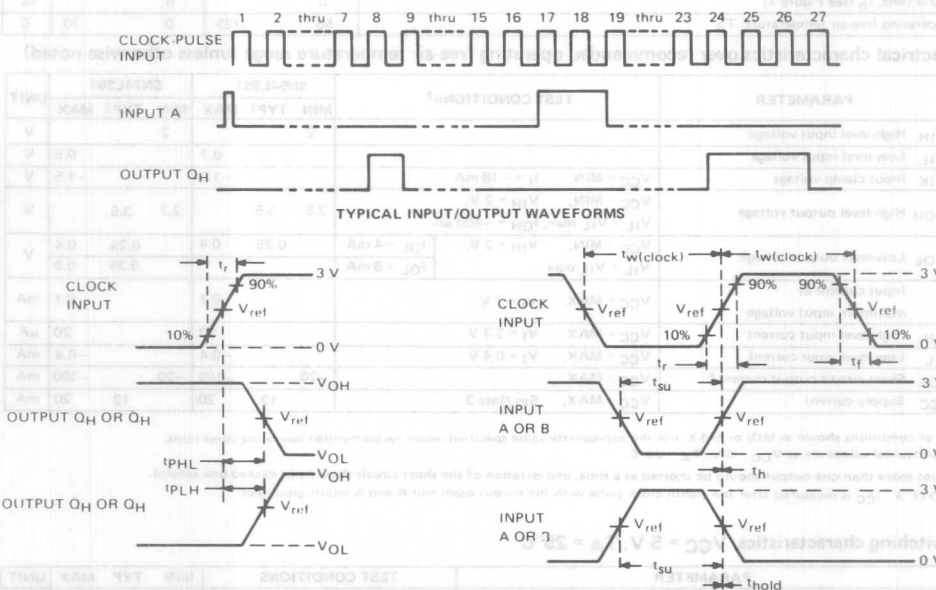
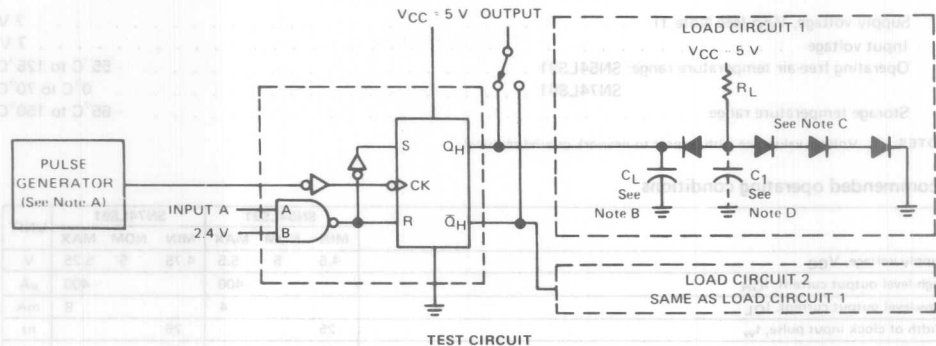
NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	10	18		MHz
t_{PLH} Propagation delay time, low-to-high-level output	See Figure 1		24	40	ns
t_{PHL} Propagation delay time, high-to-low-level output			27	40	ns

TYPES SN54LS91, SN74LS91 8-BIT SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS

SWITCHING TIMES VOLTAGE WAVEFORMS

- NOTES: A. The generator has the following characteristics: $t_w(\text{clock}) = 500 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$, $Z_{\text{out}} \approx 50 \Omega$. For SN54LS91, $t_r = 15 \text{ ns}$, and $t_f = 6 \text{ ns}$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. $C_1 = 30 \text{ pF}$ and is used for SN54LS91 only.
E. For SN54LS91/SN74LS91, $V_{\text{ref}} = 1.3 \text{ V}$.

FIGURE 1—SWITCHING TIMES

3

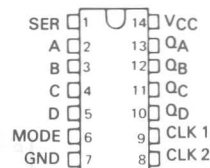
TTL DEVICES

TYPES SN5495A, SN54LS95B,
SN7495A, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

MARCH 1974 — REVISED DECEMBER 1983

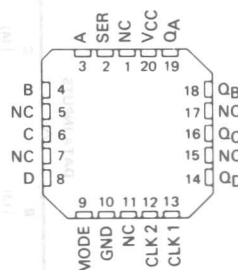
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'LS95B	36 MHz	65 mW

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A . . . J OR N PACKAGE
SN74LS95B . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS95B . . . FK PACKAGE
SN74LS95B

(TOP VIEW)



NC - No internal connection

description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

FUNCTION TABLE

MODE CONTROL	CLOCK			SERIAL	PARALLEL				OUTPUTS			
	2 (L)	1 (R)			A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	L	X	X	X	a	b	c	d	a	b	c	d
H	L	X	X	$Q_{B\uparrow}$	$Q_{C\uparrow}$	$Q_{D\uparrow}$	d	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	L	H	X	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	L	L	X	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
L	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	L	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

[†]Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

L = transition from high to low level, L = transition from low to high level

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most recent L transition of the clock.

PRODUCTION DATA

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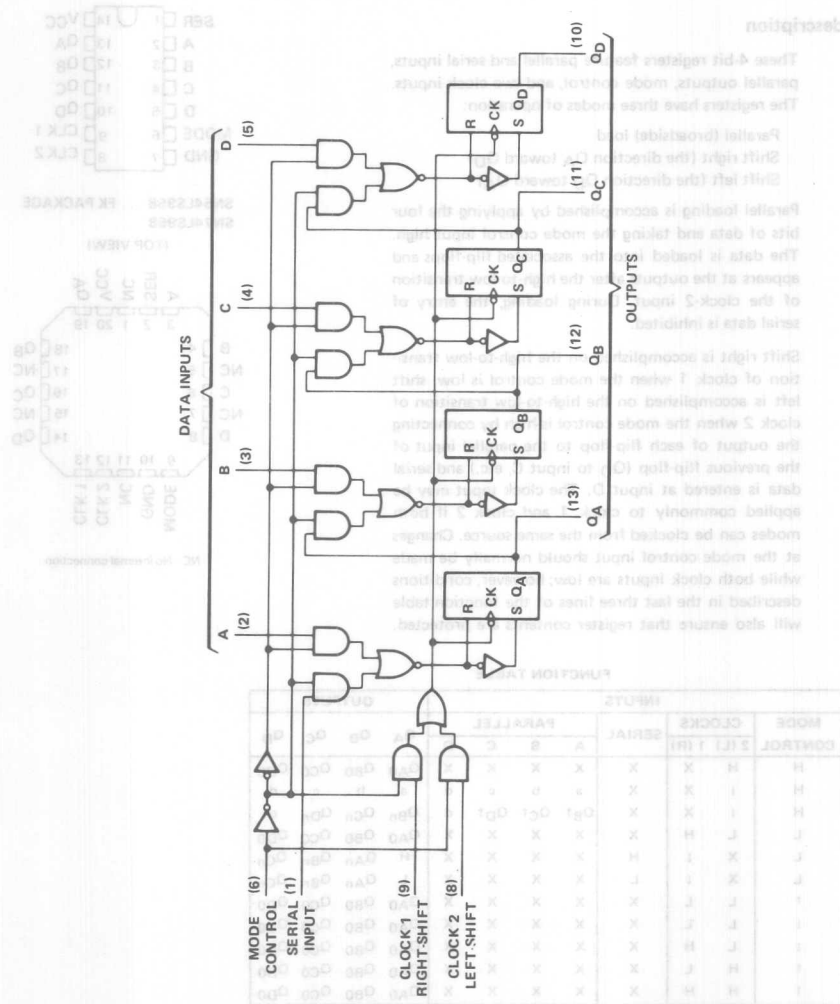
TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN5495A, SN54LS95B, SN7495A, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

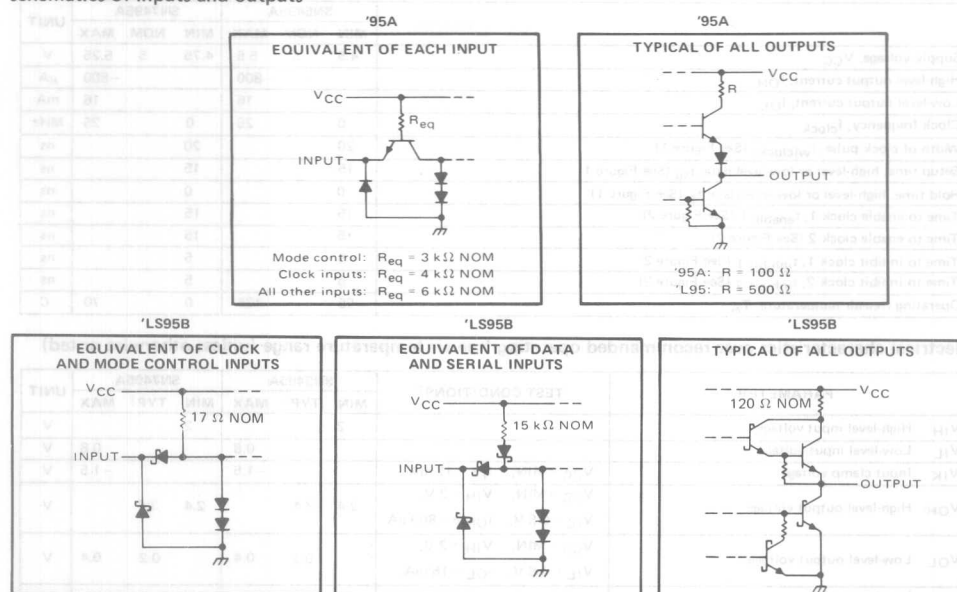
logic diagrams



3 TTL DEVICES

TYPES SN5495A, SN54LS95B, SN7495A, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	-55 to 125		0 to 70		$^{\circ}\text{C}$
Storage temperature range	-65 to 150		-65 to 150		$^{\circ}\text{C}$

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies between the clock-2 input and the mode control input of the '95A.

3

TTL DEVICES

TYPES SN5495A, SN7495A 4-BIT PARALLEL- SHIFT REGISTERS

recommended operating conditions

	SN5495A			SN7495A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{W(clock)}$ (See Figure 1)		20			20		ns
Setup time, high-level or low-level data, t_{SU} (See Figure 1)		15			15		ns
Hold time, high-level or low-level data, t_H (See Figure 1)		0			0		ns
Time to enable clock 1, $t_{enable 1}$ (See Figure 2)		15			15		ns
Time to enable clock 2 (See Figure 2)		15			15		ns
Time to inhibit clock 1, $t_{inhibit 1}$ (See Figure 2)		5			5		ns
Time to inhibit clock 2, $t_{inhibit 2}$ (See Figure 2)		5			5		ns
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5495A			SN7495A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2			40			40	μ A
		Mode control			80			80	
I_{IL}	Low-level input current	Serial, A, B, C, D, Clock 1 or 2			-1.6			-1.6	mA
		Mode control			-3.2			-3.2	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-18		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 4}$		39	63		39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{\max}	Maximum clock frequency	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Figure 1		25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32		ns

3

TTL DEVICES

TYPES SN54LS95B, SN74LS95B

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

recommended operating conditions

	SN54LS95B			SN74LS95B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_w(\text{clock})$ (see Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{su} (see Figure 1)	20			20			ns
Hold time, high-level or low-level data, t_h (see Figure 1)	20			10			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	20			20			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	20			20			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	20			20			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	20			20			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS95B			SN74LS95B			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 4		13	21		13	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

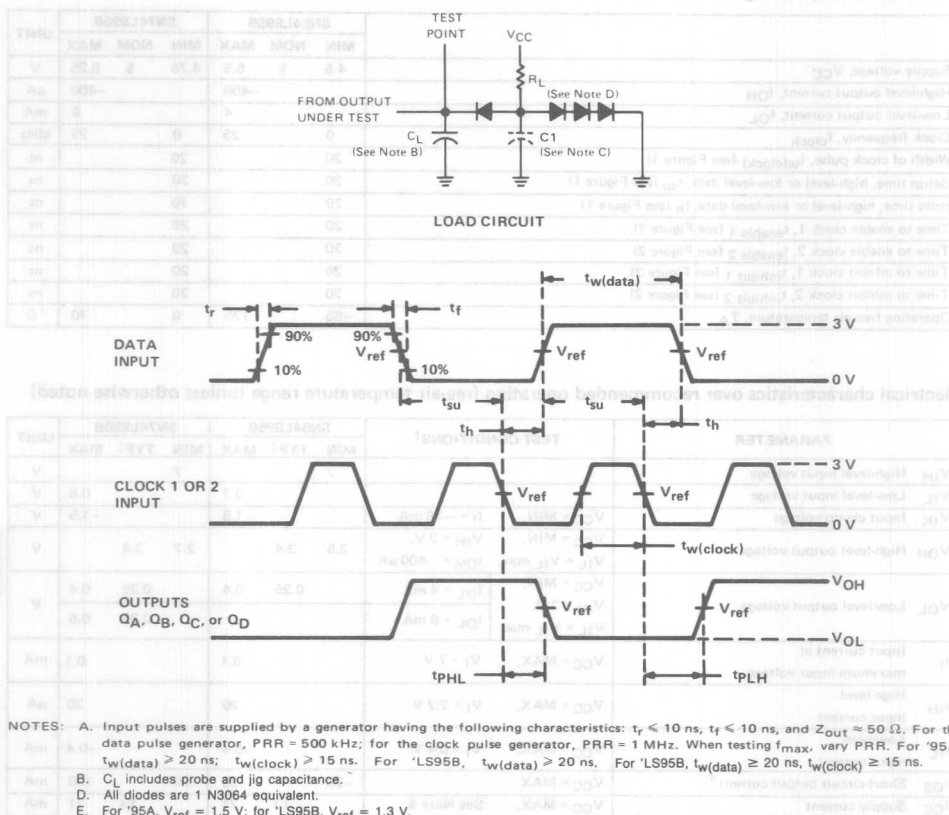
NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$, See Figure 1	25	36		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	32	ns

TYPES SN5495A, SN54LS95B, SN7495A, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION

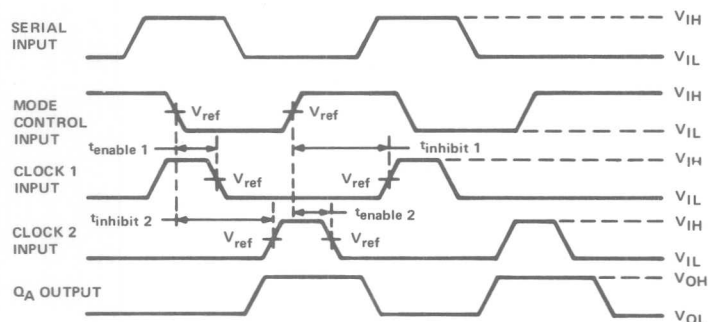


VOLTAGE WAVEFORMS
FIGURE 1-SWITCHING TIMES

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{max}	$C_L = 10 \text{ pF}$, $R_L = 1 \text{ k}\Omega$	55	55	55	ns
t_{set}		18	18	18	ns
t_{prop}		25	25	25	ns

TYPES SN5495A, SN54LS95B, SN7495A, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input A is at a low level.
 B. For '95A, $V_{ref} = 1.5\text{ V}$; for 'LS95B, $V_{ref} = 1.3\text{ V}$.

VOLTAGE WAVEFORMS
FIGURE 2-CLOCK ENABLE/INHIBIT TIMES

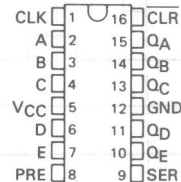
TYPES SN5496, SN54LS96 SN7496, SN74LS96 5-BIT SHIFT REGISTERS

MARCH 1974—REVISED DECEMBER 1983

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

SN5496, SN54LS96 ... J OR W PACKAGE
SN7496 ... J OR N PACKAGE
SN74LS96 ... D, J OR N PACKAGE
(TOP VIEW)

TYPE	TYPICAL	
	PROPAGATION DELAY TIME	POWER DISSIPATION
'96	25 ns	240 mW
'LS96	25 ns	60 mW



For chip carrier information on SN54LS96 and SN74LS96, contact the factory.

description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

CLEAR	PRESET ENABLE	INPUTS					CLOCK	SERIAL	OUTPUTS				
		A	B	C	D	E			QA	QB	QC	QD	QE
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	QA0	QB0	QC0	QD0	QE0
H	H	H	L	H	L	H	L	X	H	QB0	H	QD0	H
H	L	X	X	X	X	X	L	X	QA0	QB0	QC0	QD0	QE0
H	L	X	X	X	X	X	↑	H	H	QAn	QBn	QCn	QDn
H	L	X	X	X	X	X	↑	L	L	QAn	QBn	QCn	QDn

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

QA0, QB0, etc = the level of QA, QB, etc, respectively before the indicated steady-state input conditions were established.

QAn, QBn, etc = the level of QA, QB, etc, respectively before the most-recent ↑ transition of the clock.

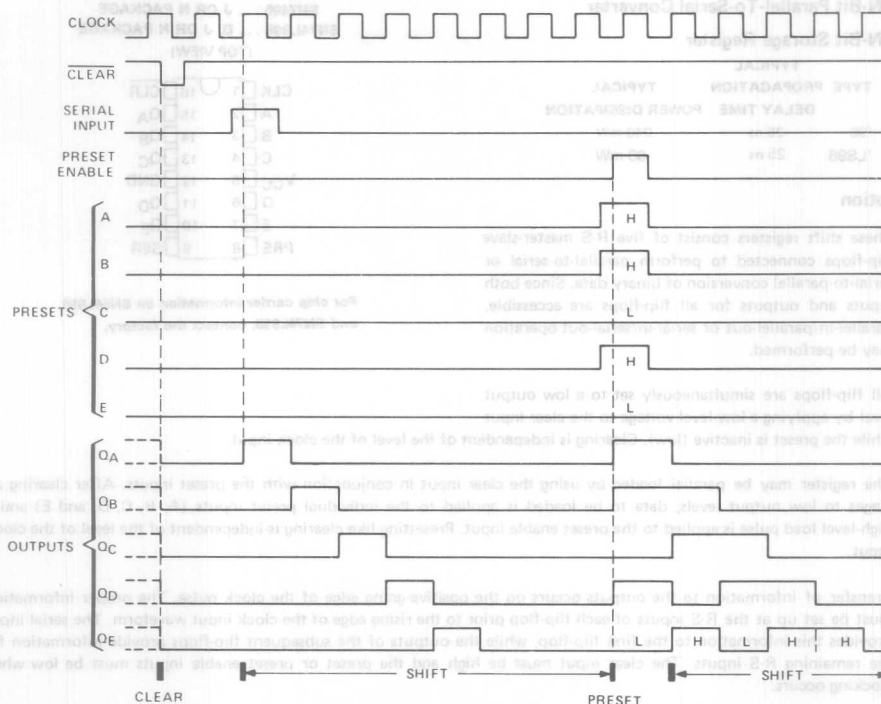
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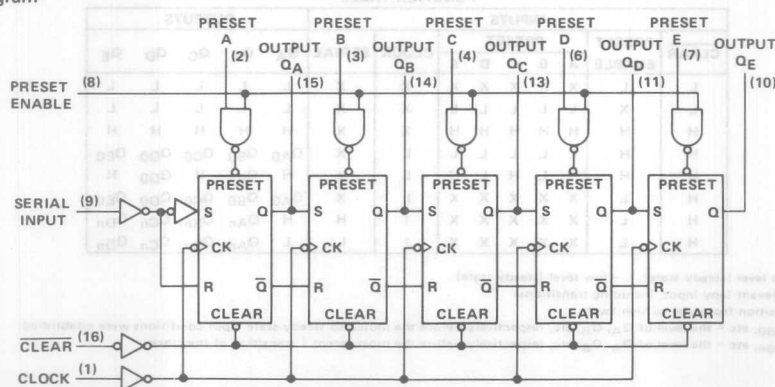


TYPES SN5496, SN54LS96
SN7496, SN74LS96
5-BIT SHIFT REGISTERS

typical clear, shift, preset, and shift sequences



logic diagram



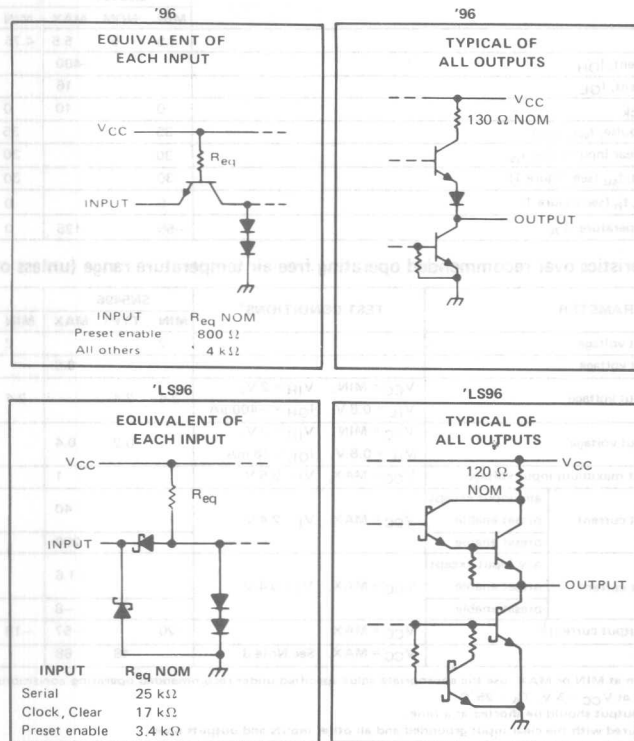
Pin numbers shown on logic notation are for D, J, or N packages.

3

TTL DEVICES

**TYPES SN5496, SN54LS96
SN7496, SN74LS96
5-BIT SHIFT REGISTERS**

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2): '96	5.5 V
'LS96	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

3

TTL DEVICES

TYPES SN5496, SN7496

5-BIT REGISTERS

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_{w(clock)}$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{su} (see Figure 1)	30			30			ns
Serial input hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN5496			SN7496			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	any input except preset enable			40			40	μ A
		pres. enable			200			200	
I_{IL}	Low-level input current	any input except preset enable			-1.6			-1.6	mA
		pres. enable			-8			-8	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-57		-18	-57		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3	48	68		48	79		mA

[†]For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock		25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable		28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			55	ns

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TTL DEVICES

TYPES SN54LS96, SN74LS96 5-BIT SHIFT REGISTERS

recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0	25	0	0	25		MHz
Width of clock input pulse, $t_{W(clock)}$	20		20				ns
Width of preset and clear input pulse, t_W	30		30				ns
Serial input setup time, t_{setup} (see Figure 1)	30		30				ns
Serial input hold time, t_{hold} (see Figure 1)	0		0				ns
Operating free-air temperature, T_A	-55	125	0	70			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS96			SN74LS96			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage			0.7			0.8		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$ <div>$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$</div>	0.25	0.4		0.25	0.4		V
I_I	Input current at maximum input voltage	Preset enable		0.5			0.5		mA
	All others			0.1			0.1		
I_{IH}	High-level input current	Preset enable		100			100		μA
	All others			20			20		
I_{IL}	Low-level input current	Preset enable		-2			-2		mA
	All others			-0.4			-0.4		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3		12	20		12	20	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

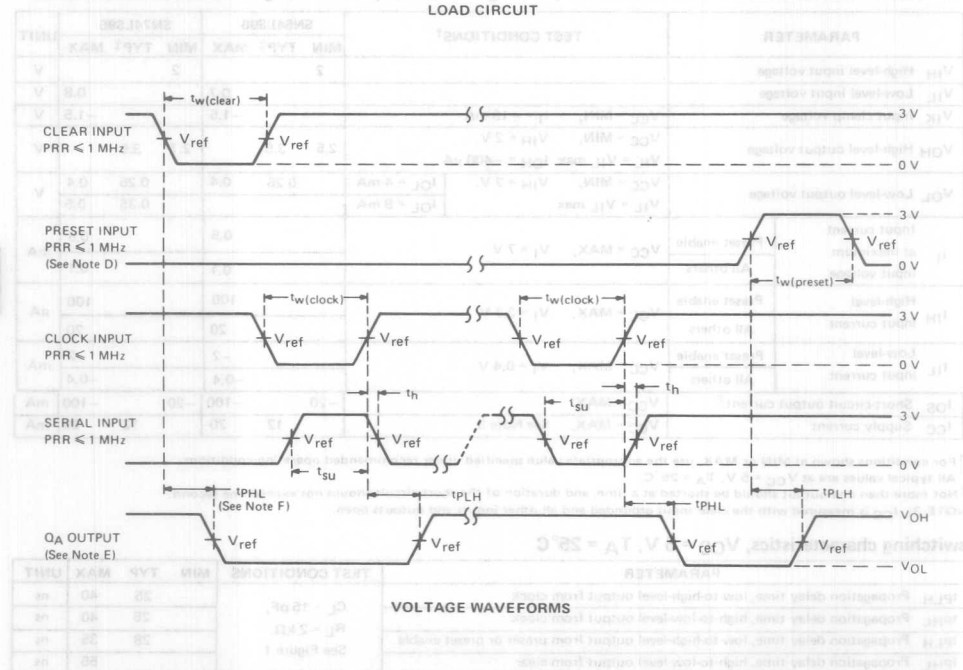
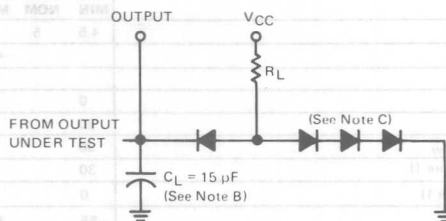
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figure 1		25	40	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				55	ns

REMIT DRIVING—1 BRUIN

5-BIT SHIFT REGISTERS



NOTES: A. Input pulses are supplied by pulse generators having the following characteristics: duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '96 $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS96 $t_r = 15$ ns, $t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
E. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.
F. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
G. For '96, $V_{ref} = 1.5$ V; for 'LS96, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

DECEMBER 1972—REVISED DECEMBER 1983

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

SN5497 . . . J OR W PACKAGE
SN7497 . . . J OR N PACKAGE

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These six-bit serial binary counters feature buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie.:

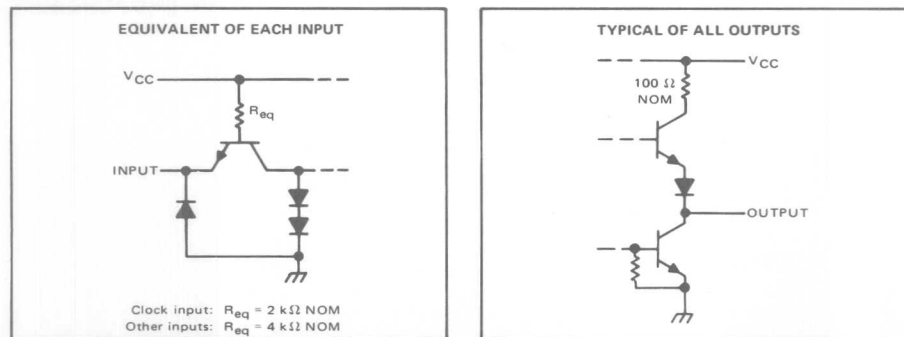
$$f_{out} = \frac{M \cdot f_{in}}{64}$$

$$\text{where: } M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$$

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

schematics of inputs and outputs



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TEXAS
INSTRUMENTS

TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

description (continued)

STATE AND/OR RATE FUNCTION TABLE (See Note A)

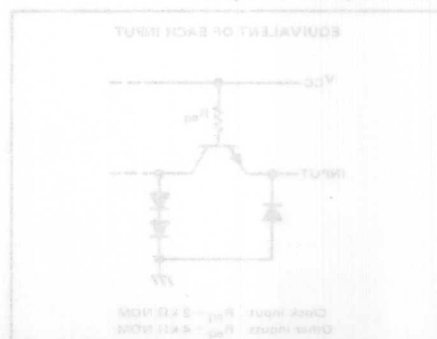
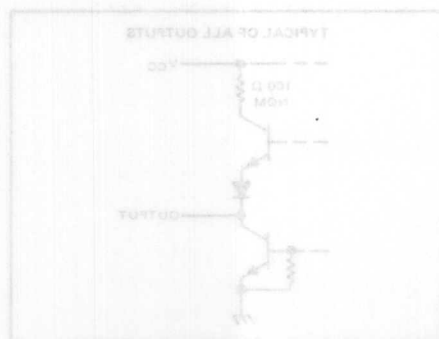
			INPUTS						OUTPUTS					
CLEAR	ENABLE	STROBE	BINARY RATE B5 B4 B3 B2 B1 B0						NUMBER OF CLOCK PULSES	UNITY/ CASCADE	LOGIC LEVEL OR NUMBER OF PULSES			NOTES
											Y	Z	ENABLE	
			H	X	H	X	X	X	X	X	X	H	L	
L	L	L	L	L	L	L	L	L	64	H	L	H	1	C
L	L	L	L	L	L	L	L	H	64	H	1	1	1	C
L	L	L	L	L	L	L	H	L	64	H	2	2	1	C
L	L	L	L	L	L	H	L	L	64	H	4	4	1	C
L	L	L	L	L	H	L	L	L	64	H	8	8	1	C
L	L	L	L	H	L	L	L	L	64	H	16	16	1	C
L	L	L	H	L	L	L	L	L	64	H	32	32	1	C
L	L	L	H	H	H	H	H	H	64	H	63	63	1	C
L	L	L	H	H	H	H	H	H	64	L	H	63	1	D
L	L	L	H	L	H	L	L	L	64	H	40	40	1	E

- NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
D. Unity/cascade is used to inhibit output Y.

$$E. f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32) f_{in}}{64} = \frac{40 f_{in}}{64} = 0.625 f_{in}$$

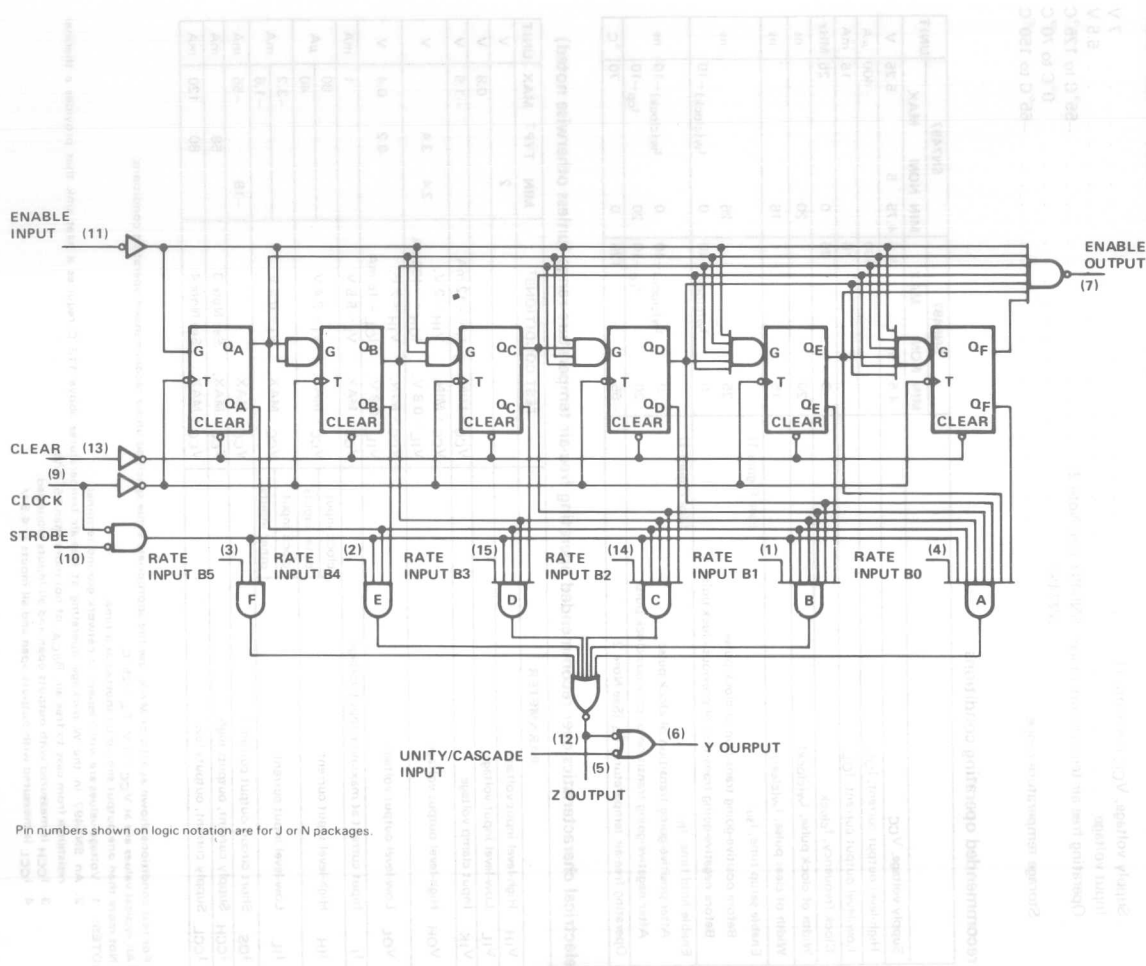
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TTL DEVICES



TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

logic diagram



TTL DEVICES

3

TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5497 (see Note 2)	–55°C to 125°C
SN7497	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

	SN5497			SN7497			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_w(\text{clock})$	20			20			ns
Width of clear pulse, $t_w(\text{clear})$	15			15			ns
Enable setup time, t_{su} : (See Figure 1)							
Before positive-going transition of clock pulse	25			25			ns
Before negative-going transition of previous clock pulse	0	$t_w(\text{clock}) - 10$		0	$t_w(\text{clock}) - 10$		
Enable hold time, t_h : (See Figure 1)							
After positive-going transition of clock pulse	0	$t_w(\text{clock}) - 10$		0	$t_w(\text{clock}) - 10$		ns
After negative-going transition of previous clock pulse	20	$t_{cp} - 10$		20	$t_{cp} - 10$		
Operating free-air temperature, T_A (See Note 2)	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage			0.8		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			80	μ A
	clock input				40	
	other inputs					
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–3.2	mA
	clock input				–1.6	
	other inputs					
I_{OS}	Short circuit output current§	$V_{CC} = \text{MAX}$	–18		–55	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = \text{MAX}, \text{ See Note 3}$		58		mA
I_{CCL}	Supply current, outputs low	$V_{CC} = \text{MAX}, \text{ See Note 4}$		80	120	mA

† For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

- NOTES:
1. Voltage values are with respect to network ground terminal.
 2. An SN5497 in the W package operating at free-air temperatures above 118°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 55°C/W.
 3. I_{CCH} is measured with outputs open and all inputs grounded.
 4. I_{CCL} is measured with outputs open and all inputs at 4.5 V.

3
TTL DEVICES

TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETERS [†]	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}	Enable	Enable			14	21	ns
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}	Strobe	Z			15	23	ns
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}	Clock	Y			20	30	ns
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}	Clock	Z			17	26	ns
t_{PLH}	Rate	Z	$C_L = 15 pF$, $R_L = 400 \Omega$, See Figure 1		6	10	ns
t_{PHL}	Rate	Z			9	14	ns
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}	Unity/Cascade	Y			6	10	ns
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}	Strobe	Y			22	33	ns
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}	Clock	Enable			22	33	ns
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}	Clear	Z			15	23	ns
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}	Any Rate Input	Y			15	23	ns

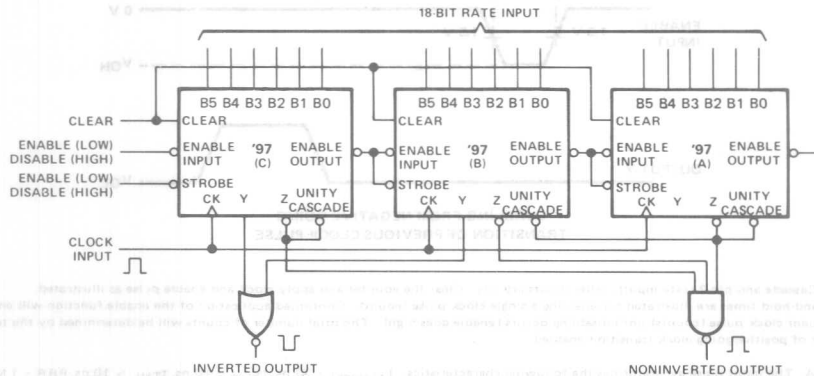
[†] f_{max} = maximum clock frequency.

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

TYPICAL APPLICATION DATA

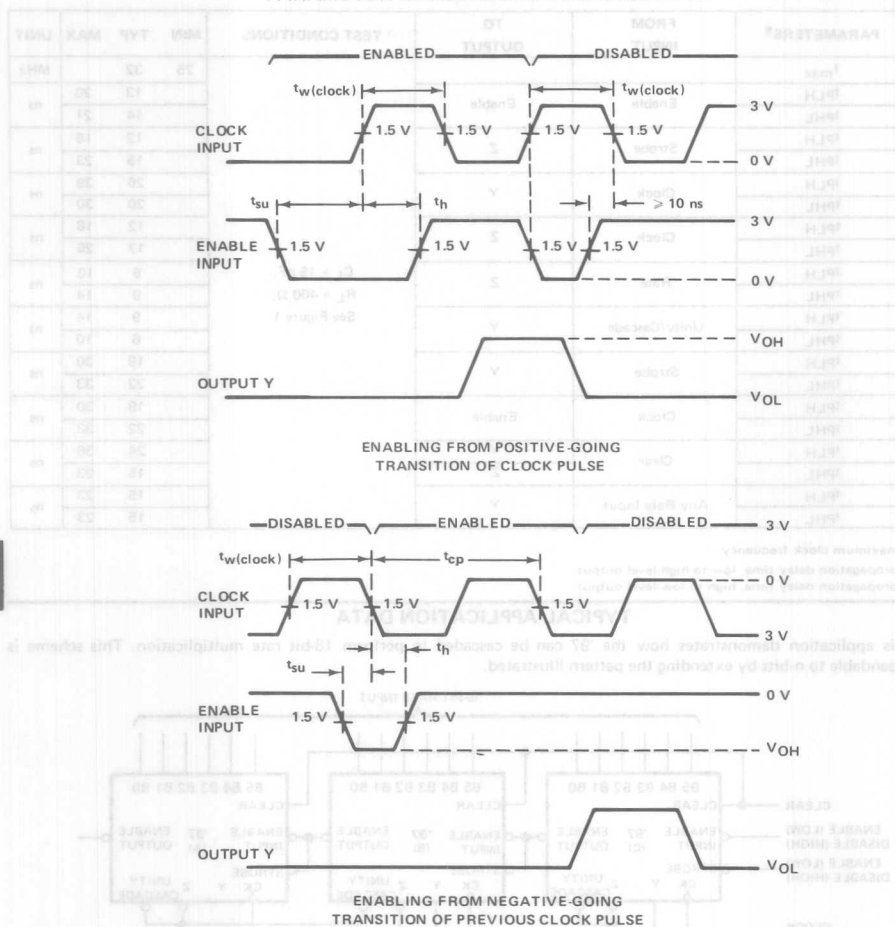
This application demonstrates how the '97 can be cascaded to perform 18-bit rate multiplication. This scheme is expandable to n-bits by extending the pattern illustrated.



As illustrated, two of the 6-bit multipliers can be cascaded by connecting the Z output of unit A to the unity cascade input of unit B, in which case, a two-input NOR gate is used to cascade the remaining multipliers. Alternatively, all three Y outputs can be cascaded with a 3-input NOR gate. The three unused unity cascade inputs can be conveniently terminated by connecting each to its Z output.

TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

PARAMETER MEASUREMENT INFORMATION



1. Unity/Cascade and pin 2 (rate input), other inputs are low. Clear the counter and apply clock and enable pulse as illustrated.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulse (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transition enabled.

NOTES: A. The input pulse generator has the following characteristics: $t_w(\text{clock}) = 20 \text{ ns}$, $t_{TLH} \leq 10 \text{ ns}$, $t_{THL} \leq 10 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

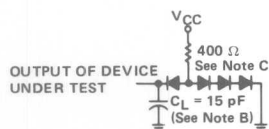
FIGURE 1—SWITCHING TIMES

3

TTL DEVICES

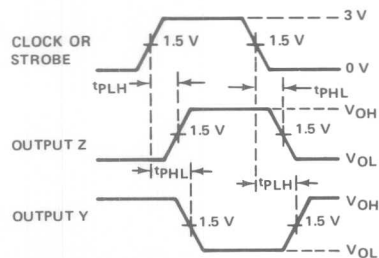
TYPES SN5497, SN7497 SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

PARAMETER MEASUREMENT INFORMATION



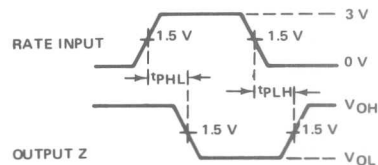
All three outputs are loaded during testing.

LOAD CIRCUIT



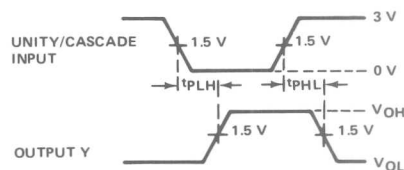
Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y



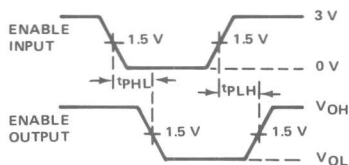
Flip-flops are at a count so that all other inputs to the gate under test are high and all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y



Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT

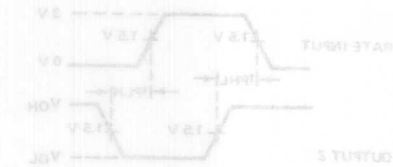
- NOTES: A. The input pulse generator has the following characteristics: $t_w(\text{clock}) = 20 \text{ ns}$, $t_{\text{PLH}} \approx 10 \text{ ns}$, $t_{\text{THL}} \approx 10 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, $Z_{\text{out}} \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES (CONTINUED)

3

TTL DEVICES

PARAMETER MEASUREMENT INFORMATION



Flip-flops are set to 0 until all other inputs are the right level. Then the rate input is high, and all other inputs are low. Input is low.

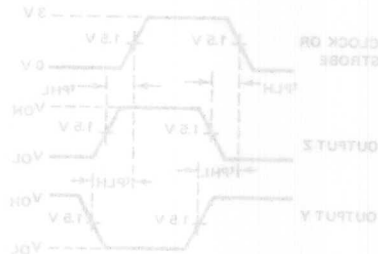
PROPAGATION DELAY TIME:
RATE INPUT TO Z



PROPAGATION DELAY TIME:
RATE INPUT TO Y



All three outputs are loaded during test up.



PROPAGATION DELAY TIME: CLOCK TO Z AND Y.
AND STROBE INPUT TO Z AND Y



Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIME:
ENABLE INPUT TO ENABLE OUTPUT

NOTES: A. The input pulse generator has the following characteristics: (a) $t_{rise} = 20$ ns, (b) $t_{fall} = 10$ ns, (c) $t_{width} = 10$ ns, (d) $t_{period} = 10$ ns, (e) $t_{jitter} = 1$ ns.
B. C_L includes probe and its connection.
C. All signals are TIOGA or equivalent.

FIGURE 1 - SWITCHING TIMES (CONTINUED)

TYPES SN54100, SN74100 8-BIT BISTABLE LATCHES

DECEMBER 1972 REVISED DECEMBER 1983

- Dependable Texas Instruments Quality and Reliability

SN54100 J OR W PACKAGE
SN74100 J OR N PACKAGE

(TOP VIEW)

NC	1	24	V _{CC}
1D1	2	23	1C
1D2	3	22	1D3
1Q2	4	21	1D4
1Q1	5	20	1Q4
NC	6	19	1Q3
GND	7	18	2Q3
2Q1	8	17	2Q4
2Q2	9	16	2D4
2D2	10	15	2D3
2D1	11	14	NC
2C	12	13	NC

NC - No internal connection

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q ₀	Q ₀

H = high level, X = irrelevant

Q₀ = the level of Q before the high-to-low transition of G

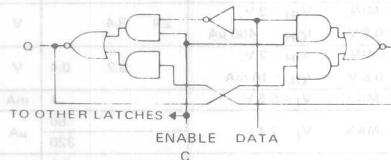
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was setup at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

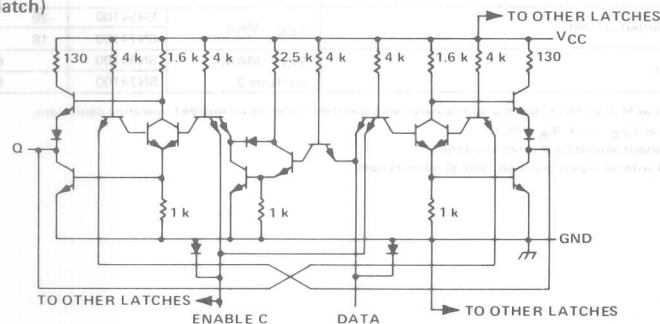
These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 40 milliwatts per latch.

The SN54100 is characterized for operation over the full military temperature range of -55°C to 125°C; the SN74100 is characterized for operation from 0°C to 70°C.

logic diagram (each latch)



schematic (each latch)



Resistor values shown are nominal and in ohms.

3

TTL DEVICES

TYPES SN54100, SN74100 8-BIT BISTABLE LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54100	-55°C to 125°C
SN74100	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter input transistor. For this circuit, this rating applies between the enable and D inputs of any latch.

recommended operating conditions

	SN54100			SN74100			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage			0.8		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	D input			80	μ A
		C input			320	μ A
I_{IL}	Low-level input current	D input			-3.2	mA
		C input			-12.8	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$				mA
		SN54100	-20		-57	
		SN74100	-18		-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$				mA
		SN54100		64	92	
		See Note 3		64	106	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

TYPES SN54100, SN74100
8-BIT BISTABLE LATCHES

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	D	Q	C _L = 15 pF, R _L = 400 Ω, See Note 4	16	30	ns	
t _{PHL}				14	25		
t _{PLH}	C	Q		16	30	ns	
t _{PHL}				7	15		

[†]t_{PLH} = propagation delay time, low to high level output

t_{PHL} = propagation delay time, high to low level output

NOTE 4: Load circuits and voltage waveforms are the same as those shown for the '75, '77, 'L75, and 'L77.

Switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN. TYP. MAX. UNIT
t_{PLH}	0	0	$C_L = 15 pF$	10
t_{PHL}				10
t_{PLH}	0	0	$R_L = 400 \Omega$	10
t_{PHL}				10
t_{PHL}	0	0	See Note 4	1
t_{PHL}				10

* t_{PLH} Propagation delay time, low to high level output.
* t_{PHL} Propagation delay time, high to low level output.
NOTE 4: Load circuit and voltage waveform are the same as those shown for the '00, '05, '10, '15, '20, and '25.

**TYPES SN54107, SN54LS107A,
SN74107, SN74LS107A
DUAL J-K FLIP-FLOPS WITH CLEAR**
REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

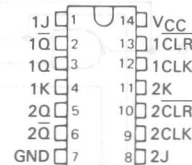
description

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low clock transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS107A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

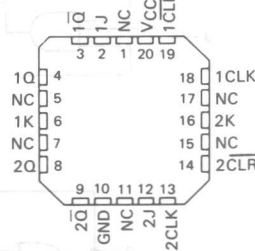
The SN54107 and the SN54LS107A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74107 and the SN74LS107A are characterized for operation from 0°C to 70°C .

SN54107, SN54LS107A ... J PACKAGE
SN74107 ... J OR N PACKAGE
SN74LS107A ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS107A ... FK PACKAGE
SN74LS107A

(TOP VIEW)



NC - No internal connection

'107
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	TOGGLE

'LS107A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	\bar{Q}_0

3

TTL DEVICES

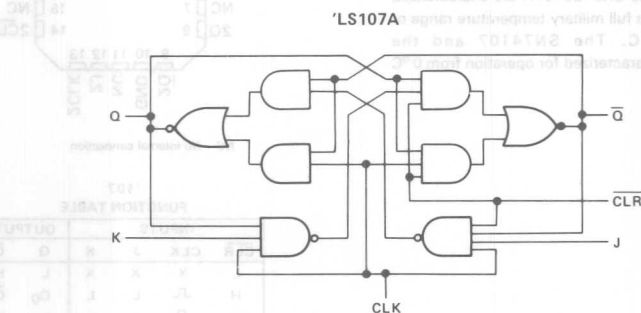
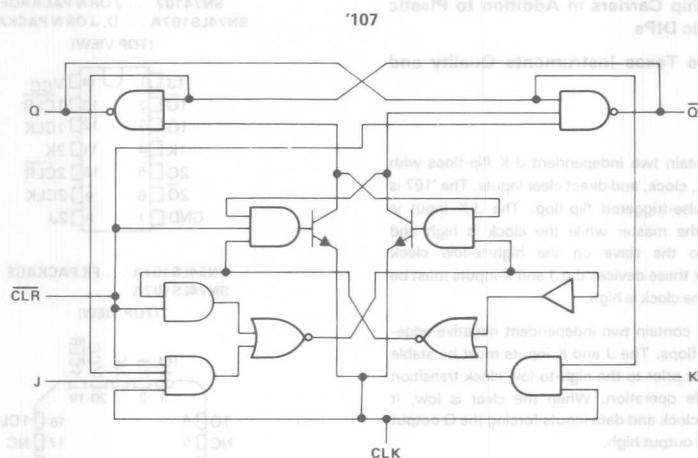
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54107, SN54LS107A, SN74107, SN74LS107A DUAL J-K FLIP-FLOPS WITH CLEAR

logic diagrams



FUNCTION TABLE

Q	Q̄	CLK	J	K
H	L	X	X	X
L	H	X	X	X
H	L	L	L	L
L	H	L	L	L
H	L	L	L	L
L	H	L	L	L
H	L	L	L	L
L	H	L	L	L

FUNCTION TABLE

Q	Q̄	CLK	J	K
H	L	X	X	X
L	H	X	X	X
H	L	L	L	L
L	H	L	L	L
H	L	L	L	L
L	H	L	L	L
H	L	L	L	L
L	H	L	L	L

3 TTL DEVICES

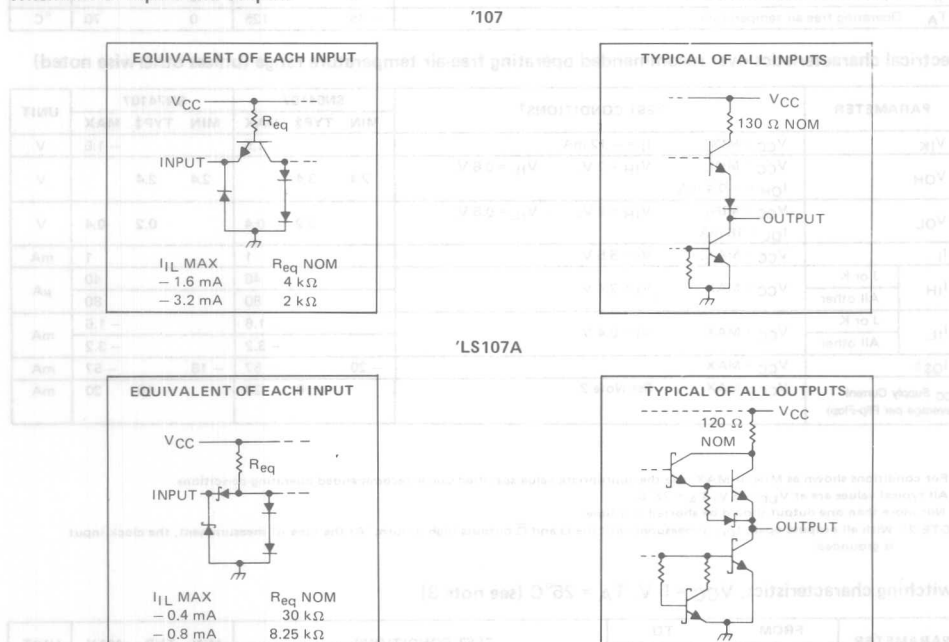
TYPES SN54107, SN54LS107A,
SN74107, SN74LS107A
DUAL J-K FLIP-FLOPS WITH CLEAR

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '107	5.5 V
'LS107A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54107, SN74107 DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

		SN54107			SN74107			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			− 0.4			− 0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration	CLK high			20			ns
		CLK low			47			
		CLR low			25			
t _{su}	Input setup time before CLK†	0			0			ns
t _h	Input hold time-data after CLK†	0			0			ns
T _A	Operating free-air temperature	− 55			125			70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54107			SN74107			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -12 mA					-1.5			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA			2.4	3.4		2.4	3.4		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA				0.2	0.4		0.2	0.4	V
I _I		V _{CC} = MAX, V _I = 5.5 V					1			1	mA
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.4 V				40			40		μA
	All other					80			80		
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V				-1.6			-1.6		mA
	All other					-3.2			-3.2		
I _{OS} §		V _{CC} = MAX			-20		-57	-18		-57	mA
I _{CC} Supply Current (average per Flip-Flop)		V _{CC} = MAX, See Note 2			10		20	10		20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				15	20		MHz
t _{PLH}	\bar{CLR}	\bar{Q}	R _L = 400 Ω, C _L = 15 pF		16	25	ns
t _{PHL}		Q			25	40	ns
t _{PLH}	CLK	Q or \bar{Q}			16	25	ns
t _{PHL}					25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS107A, SN74LS107A DUAL J-K FLIP-FLOPS WITH CLEAR

recommended operating conditions

			SN54LS107A			SN74LS107A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.7			0.8	V		
I _{OH}	High-level output current				− 0.4			0.4	mA		
I _{OL}	Low-level output current				4			8	mA		
f _{clock}	Clock frequency		0		30	0		30	MHz		
t _w	Pulse duration	CLK high	20			20			ns		
		CLR low	25			25					
t _{su}	Setup time before CLK ↓	data high or low	20			20			ns		
		CLR inactive	25			25					
t _h	Hold time-data after CLK ↓		0			20			ns		
T _A	Operating free-air temperature		− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS107A			SN74LS107A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	J or K	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
	CLR				0.3			0.3	
	CLK				0.4			0.4	
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
	CLR				60			60	
	CLK				80			80	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
	CLR or CLK				-0.8			-0.8	
I _{OS} §		V _{CC} = MAX, See Note 4	-20		-100	-20		-100	mA
I _{CC}		V _{CC} = MAX, See Note 2		4	6		4	6	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{max}					30	45		MHz
t _{PLH}	CLR or CLK	Q or \bar{Q}	R _L = 2 kΩ,	C _L = 15 pF		15	20	ns
t _{PHL}						15	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

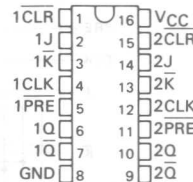
TYPES SN54109, SN54LS109A, SN74109, SN74LS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

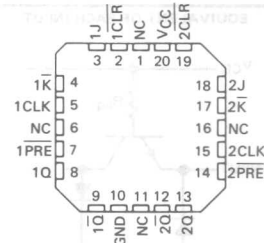
SN54109, SN54LS109A ... J OR W PACKAGE
SN74109 ... J OR N PACKAGE
SN74LS109A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS109A ... FK PACKAGE
SN74LS109A

(TOP VIEW)



description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and tying J high. They also can perform as D-type flip-flops if J and K are tied together.

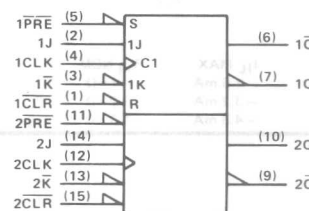
The SN54109 and SN54LS109A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74109 and SN74LS109A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	Q ₀ -bar
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	Q ₀ -bar

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

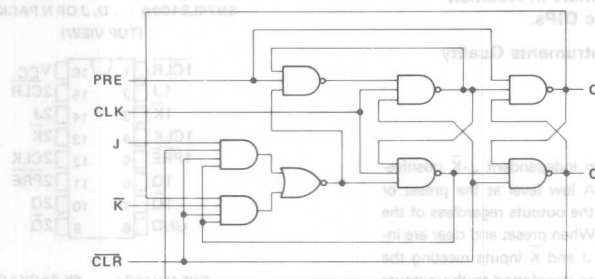
3-323

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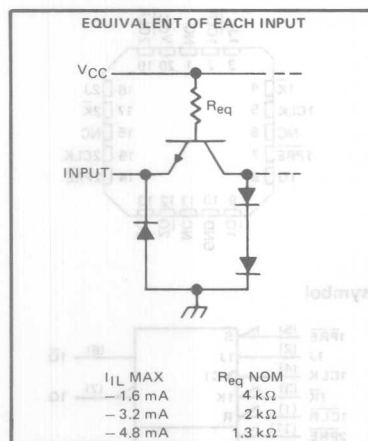
TTL DEVICES

TYPES SN54109, SN74109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

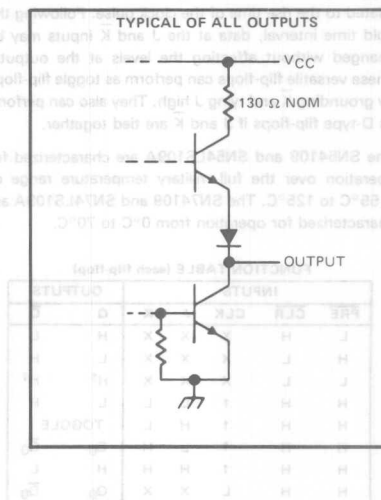
logic diagram



schematics of inputs and outputs



'109

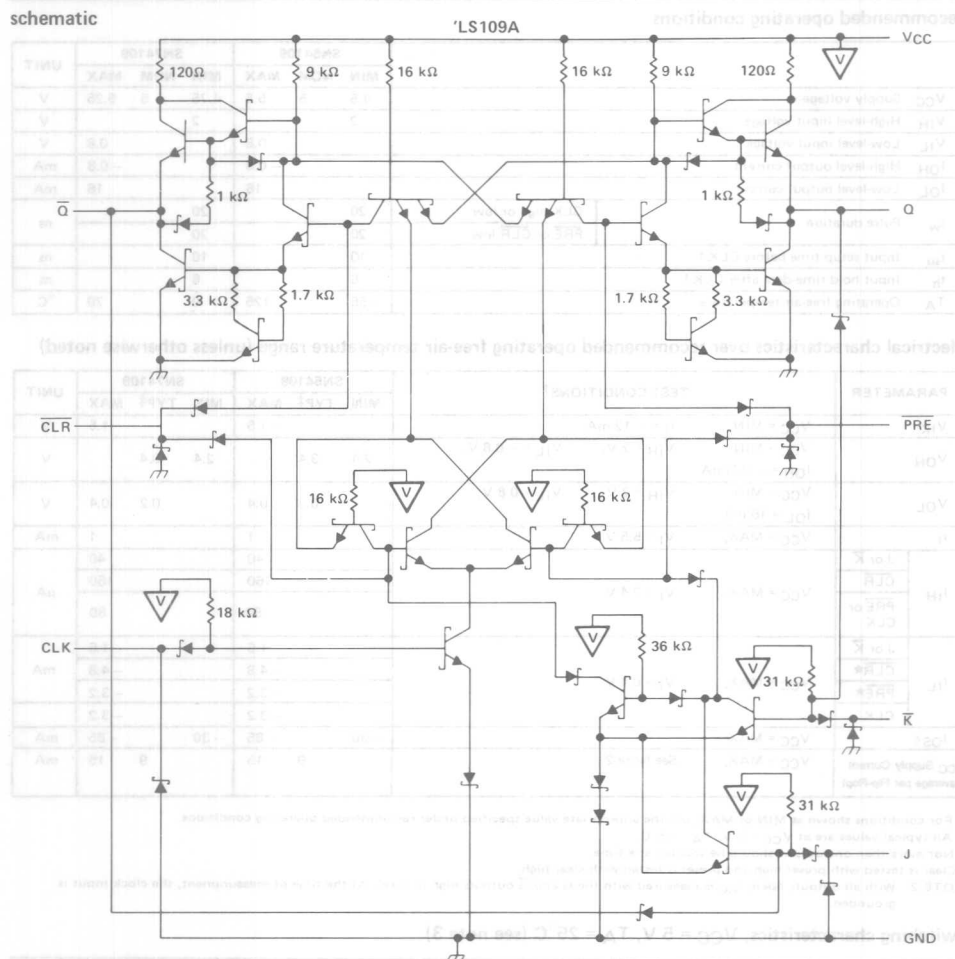


3

TTL DEVICES

TYPES SN54109, SN54LS109A,
SN74109, SN74LS109A
DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '109	5.5 V
'LS109A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54109, SN74109

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

		SN54109			SN74109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			−0.8			−0.8	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration	CLK high or low			20			ns
		PRE or CLR low			20			
t _{su}	Input setup time before CLK †	10			10			ns
t _h	Input hold time-data after CLK †	6			6			ns
T _A	Operating free-air temperature	−55			125			0 70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54109			SN74109			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = -0.8 V, I _{OH} = -0.8 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	J or K			40			40	μA
	CLR			160			160	
	PRE or CLK			80			80	
I _{IL}	J or K			-1.6			-1.6	mA
	CLR*			-4.8			-4.8	
	PRE*			-3.2			-3.2	
	CLK			-3.2			-3.2	
I _{OS} §	V _{CC} = MAX	-30		-85	-30		-85	mA
I _{CC} Supply Current (average per Flip-Flop)	V _{CC} = MAX, See Note 2		9	15		9	15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25° C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{max}				25	33		MHz
t _{PLH}	PRE	Q	R _L = 400 Ω, C _L = 15 pF	10	15		ns
t _{PHL}		Q̄		23	35		ns
t _{PLH}	CLR	Q̄		10	15		ns
t _{PHL}		Q		17	25		ns
t _{PLH}	CLK	Q or Q̄		10	16		ns
t _{PHL}		Q or Q̄		18	28		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS109A, SN74LS109A

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			SN54LS109A			SN74LS109A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.7			0.8	V		
I _{OH}	High-level output current				− 0.4			− 0.4	mA		
I _{OL}	Low-level output current				4			8	mA		
f _{clock}	Clock frequency		0		25	0		25	MHz		
t _w	Pulse duration		CLK high			25			ns		
			PRE or CLR low			25					
t _{su}	Setup time before CLK ↑		High-level data			35			ns		
			Low-level data			25					
t _h	Hold time-data after CLK ↑		5			5			ns		
T _A	Operating free-air temperature		− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS109A			SN74LS109A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA		2.5	3.4		2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA			0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA						0.35	0.5	
I _I	J, \bar{K} or CLK	V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
	CLR or PRE					0.2			0.2	
I _{IH}	J, \bar{K} or CLK	V _{CC} = MAX, V _I = 2.7 V				20			20	μA
	CLR or PRE					40			40	
I _{IL}	J, \bar{K} or CLK	V _{CC} = MAX, V _I = 0.4 V				-0.4			-0.4	mA
	CLR or PRE					-0.8			-0.8	
I _{OS} §		V _{CC} = MAX, See Note 4		-20		-100	-20		-100	mA
I _{CC}		V _{CC} = MAX, See Note 2			4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			$R_L = 2\text{ k}\Omega, \quad C_L = 15\text{ pF}$		25	33		MHz
t_{PLH}	CLR, PRE	Q or \overline{Q}				13	25	ns
t_{PHL}	or CLK					25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}		4.5	5	5.5	V
V_{IH}		2			V
V_{IL}			0.7		V
I_{OH}			0.4		mA
I_{OL}			4		mA
t_{PDR}		0	20		nS
t_{SU}		0	20		nS
t_{HD}		0	20		nS
t_{R}		0	20		nS
t_{F}		0	20		nS
t_{D}		0	20		nS
t_{A}		0	20		nS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IC}	$V_{CC} = \text{MAX}$, $I_I = 15 \text{ mA}$			1.5	V
V_{OH}	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $I_{IH} = \text{MAX}$	2.0	2.4	2.5	V
V_{OL}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.5 \text{ V}$, $I_{IL} = \text{MAX}$	0.25	0.4	0.5	V
I_{OH}	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $I_{IH} = \text{MAX}$			0.4	mA
I_{OL}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.5 \text{ V}$, $I_{IL} = \text{MAX}$			0.4	mA
I_I	$V_{CC} = \text{MAX}$, $V_I = 2 \text{ V}$			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2 \text{ V}$			0.1	mA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			0.1	mA
I_{OH}	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$			0.1	mA
I_{OL}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.5 \text{ V}$			0.1	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 2. All test values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
 3. Data shown from one output should be stored at a time, and the duration of the short circuit should not exceed one second.
 NOTE 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high or low. At the time of measurement, the clock input is grounded.
 NOTE 4: For better device characterization, the output is driven to ground, as indicated and may be performed with $V_{CC} = 2.5 \text{ V}$ and $T_A = 25^\circ\text{C}$, respectively, for the minimum and maximum values.
 Switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	CLR, PRE	Q or \bar{Q}	$R_L = 2 \text{ k}\Omega$, $C_L = 10 \text{ pF}$		12	20	nS
t_{PHL}	Q or \bar{Q}	CLR, PRE			20	40	nS

NOTE 3: See General Information section for load circuit and loading waveform.

3

TTL DEVICES

TYPES SN54111, SN74111 DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

The SN54111 and SN74111 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled to accept data only during a short period (30 nanoseconds maximum hold time) starting with, and immediately following the rising edge of the clock pulse. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. At the threshold level of the falling edge of the clock pulse, the data stored in the master will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptibility to noise is thereby effectively reduced.

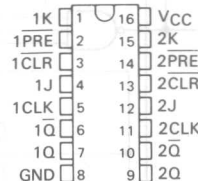
The SN54111 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74111 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

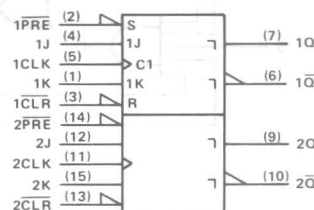
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	\downarrow	L	L	Q_0	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	

† This configuration is non-stable; that is, it will not persist when preset or clear return to their inactive (high) level.

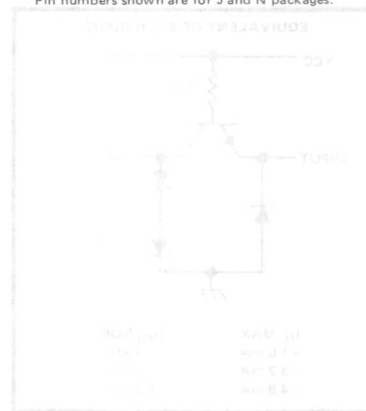
SN54111 ... J OR W PACKAGE
SN74111 ... J OR N PACKAGE
(TOP VIEW)



logic symbol



Pin numbers shown are for J and N packages.



3

TTL DEVICES

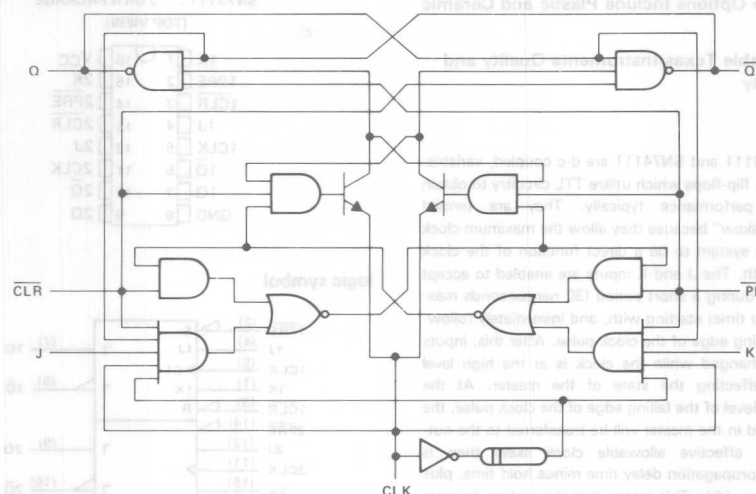
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54111, SN74111 DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

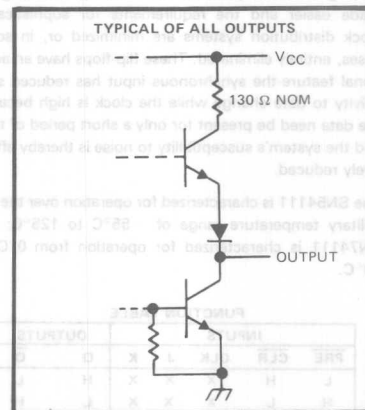
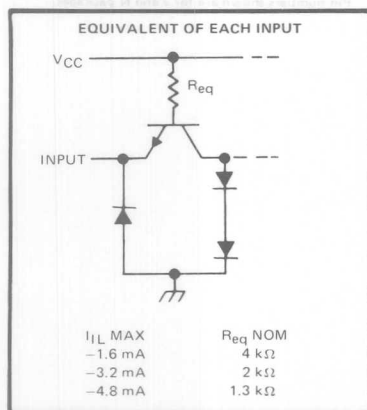
logic diagram



schematics of inputs and outputs

3

TTL DEVICES



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54111, SN74111

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

recommended operating conditions

			SN54111			SN74111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				− 0.8			− 0.8	mA
I _{OL}	Low-level output current				16			16	mA
t _w	Pulse duration	CLK high or low	25			25			ns
		PRE or CLR low	25			25			
t _{su}	Input setup time before CLK ↑		0			0			ns
t _h	Input hold time data after CLK ↑		30			30			ns
T _A	Operating free-air temperature		− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54111			SN74111			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = − 12 mA	− 1.5			− 1.5			V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = − 0.8 mA	2.4	3.4		2.4	3.4		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4		0.2	0.4		V
I _I		V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.4 V	40			40			μA
	CLR or PRE		80			80			
	CLK		120			120			
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V	− 1.6			− 1.6			mA
	CLR*		− 3.2			− 3.2			
	PRE*		− 3.2			− 3.2			
	CLK		− 4.8			− 4.8			
I _{OS} §		V _{CC} = MAX	− 20	− 57		− 18	− 57		mA
I _{CC} Supply Current (average per Flip-Flop)		V _{CC} = MAX, See Note 2	14	20.5		14	20.5		mA

\dagger For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

\ddagger All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

\S Not more than one output should be shorted at a time.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				20	25		MHz
t _{PLH}	PRE or CLR	Q or Q̄	R _L = 400 Ω, C _L = 15 pF	12	18		ns
t _{PHL}				21	30		ns
t _{PLH}	CLK	Q or Q̄		12	17		ns
t _{PHL}				20	30		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS112A, SN54S112A, SN74LS112A, SN74S112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1986

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and the SN54S112A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C .

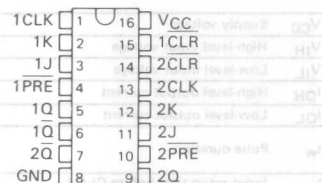
FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^{\dagger}	H^{\dagger}
H	H	\downarrow	L	L	Q_0	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	
H	H	H	X	X	Q_0	\bar{Q}_0

[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

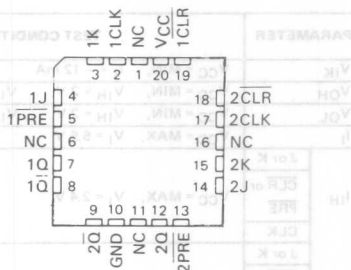
SN54LS112A, SN54S112A ... J OR W PACKAGE
SN74LS112A, SN74S112A ... D, J OR N PACKAGE

(TOP VIEW)



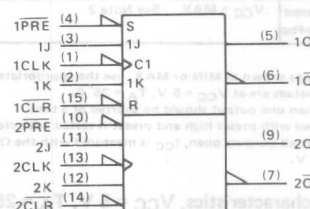
SN54LS112A, SN54S112A ... FK PACKAGE
SN74LS112A, SN74S112A

(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

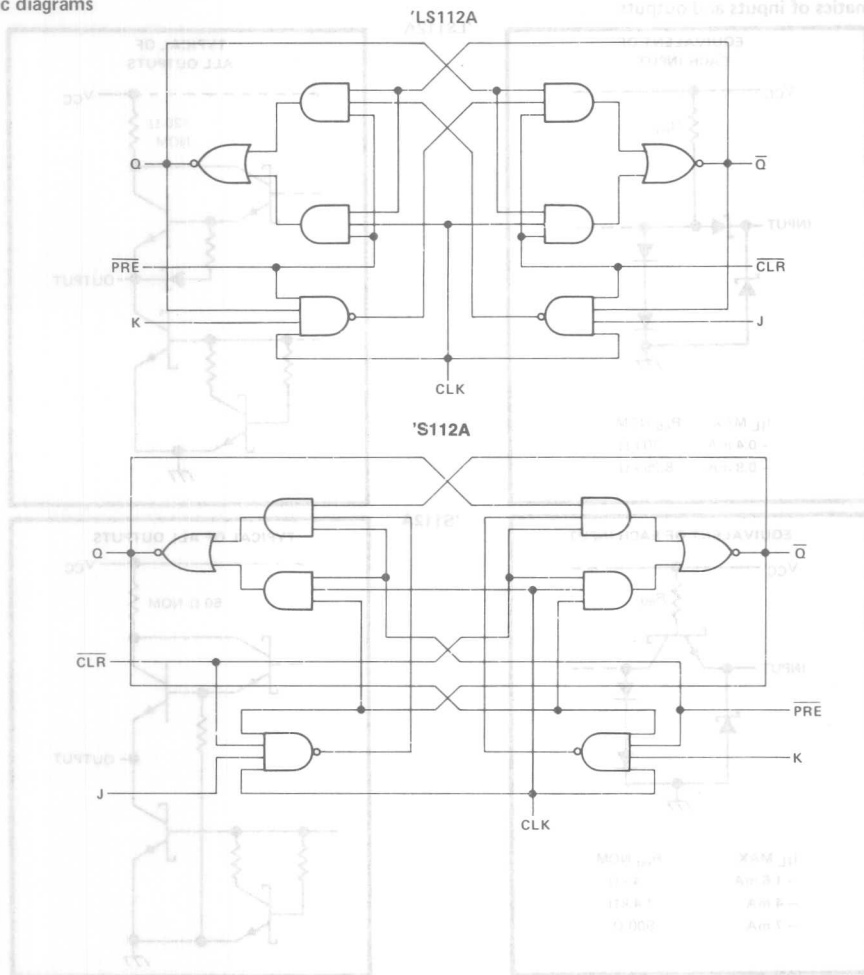
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54LS112A, SN54S112A, SN74LS112A, SN74S112A
 DUAL J-K NEGATIVE-EDGE-TRIGGERED
 FLIP-FLOPS WITH PRESET AND CLEAR

logic diagrams



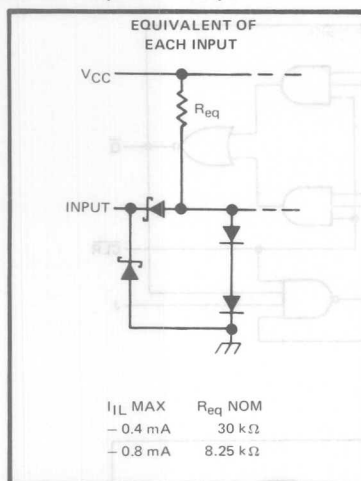
3

TTL DEVICES

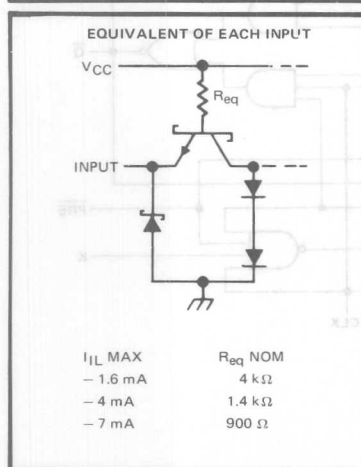
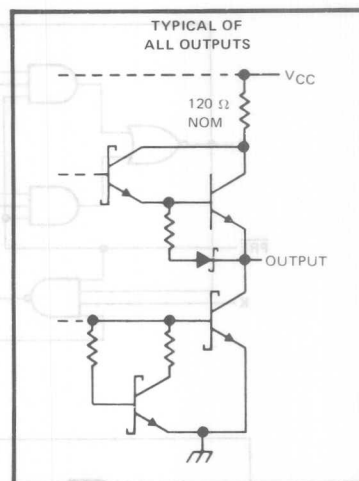
Absolute maximum ratings over operating free-air temperature range (unless otherwise noted):
 Supply voltage, V_{CC} (see Note 1) 5.5 V
 Input voltage, V_{in} (see Note 1) 5.5 V
 Operating free-air temperature range: SN54 -55°C to 125°C
 SN74 -40°C to 70°C
 Storage temperature range -65°C to 150°C

TYPES SN54LS112A, SN54S112A, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

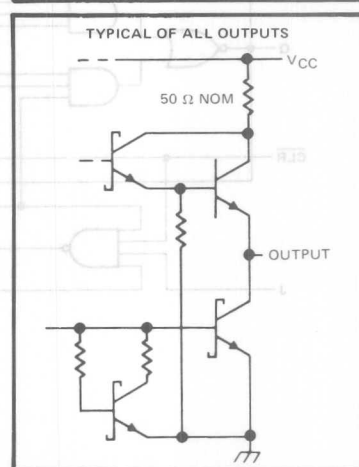
schematics of inputs and outputs



'LS112A



'S112A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS112A	7 V
'S112A	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TTL DEVICES

TYPES SN54LS112A, SN74LS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

SYMBOL	DESCRIPTION	SN54S112A			SN74S112A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage			0.8			0.8	V		
I _{OH}	High-level output current			−1			−1	mA		
I _{OL}	Low-level output current			20			20	mA		
t _w	Pulse duration	CLK high			6			ns		
		CLK low			6.5					
		PRE or CLR low			8					
t _{su}	Setup time before CLK ↓	data high or low			7			ns		
t _h	Hold time-data after CLK ↓	0			0			ns		
T _A	Operating free-air temperature	−55			125			0	70	°C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S112A			SN74S112A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, I_{OL} = 20 \text{ mA}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	J or K			50			50	μA
	All other			100			100	
I_{IL}	J or K			-1.6			-1.6	mA
	CLR*			-7			-7	
	PRE*			-7			-7	
	CLK			-4			-4	
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CC} Supply Current (average per Flip-Flop)	$V_{CC} = \text{MAX}, \text{ See Note 2}$		15	25		15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				80	125		MHz
t_{PLH}	PRE or CLR	Q or \bar{Q}	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	4	7		ns
t_{PHL}	PRE or CLR (CLK high)	\bar{Q} or Q		5	7		ns
t_{PLH}	PRE or CLR (CLK low)	\bar{Q} or Q		5	7		ns
t_{PHL}	CLK	Q or \bar{Q}		4	7		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

AS[†] TYPES SN54S112, SN74S112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS112A			SN74LS112A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		30	0		30	MHz
t _w	Pulse duration	CLK high		20	20			ns
		PRE or CLR low		25	25			ns
		data high or low		20	20			ns
t _{su}	Setup time after CLK ↓	CLR inactive		25	25			ns
		PRE inactive		20	20			ns
								ns
t _h	Hold time-data after CLK ↓	0			0			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS112A			SN74LS112A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	V
	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _I	J or K		0.3			0.3		mA
	CLR or PRE		0.4			0.4		mA
	CLK		0.4			0.4		mA
I _{IH}	J or K		20			20		μA
	CLR or PRE		60			60		μA
	CLK		80			80		μA
I _{IL}	J or K		-0.4			-0.4		mA
	All other		-0.8			-0.8		mA
I _{OS} [§]	V _{CC} = MAX, See Note 4	-20	-100		-20	-100		mA
I _{CC}	V _{CC} = MAX, See Note 2		4	6		4	6	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{max}				30	45		MHz
t _{PLH}	CLR, PRE or CLK	Q or \bar{Q}	R _L = 2 kΩ, C _L = 15 pF		15	20	ns
t _{PHL}					15	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS113A, SN54S113A, SN74LS113A, SN74S113A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

REVISED DECEMBER 1986

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset input sets the outputs regardless of the levels of the other inputs. When preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

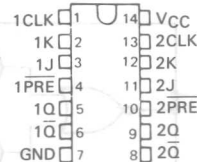
The SN54LS113A and SN54S113A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS113A and SN74S113A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	\bar{Q}
L	X	X	X	H	L
H	↓	L	L	Q ₀	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q ₀	\bar{Q}_0

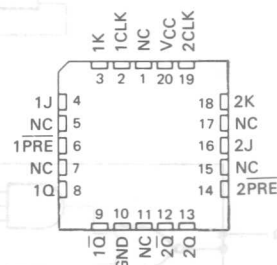
SN54LS113A, SN54S113A ... J OR W PACKAGE SN74LS113A, SN74S113A ... D, J OR N PACKAGE

(TOP VIEW)



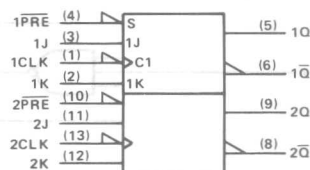
SN54LS113A, SN54S113A ... FK PACKAGE SN74LS113A, SN74S113A

(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

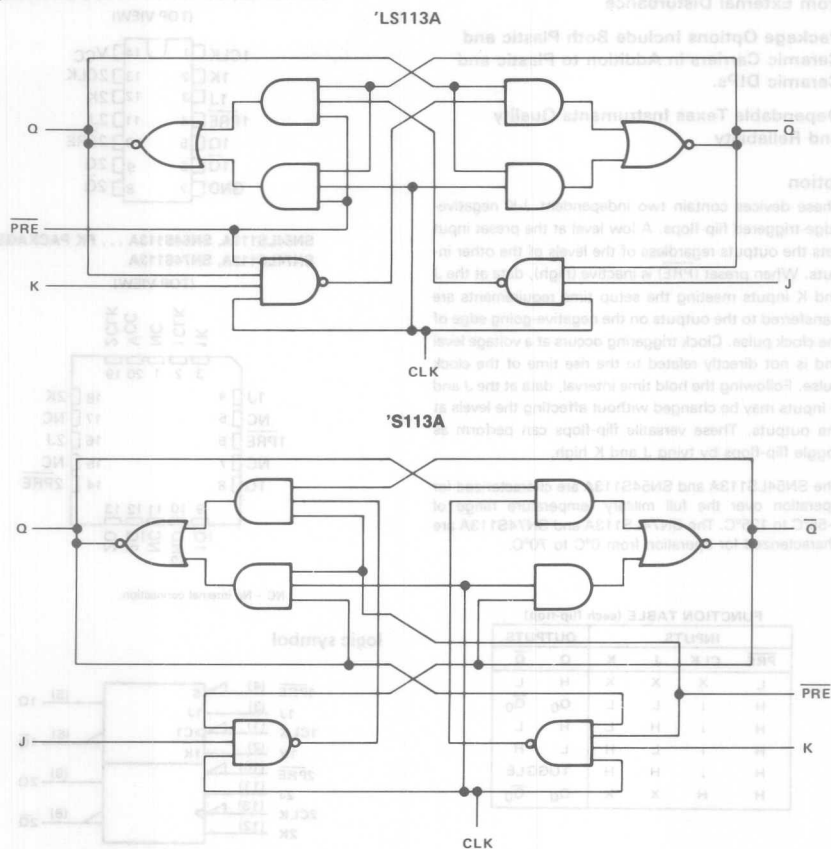
PRODUCTION DATA

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TYPES SN54LS113A, SN54S113A, SN74LS113A, SN74S113A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET

logic diagrams

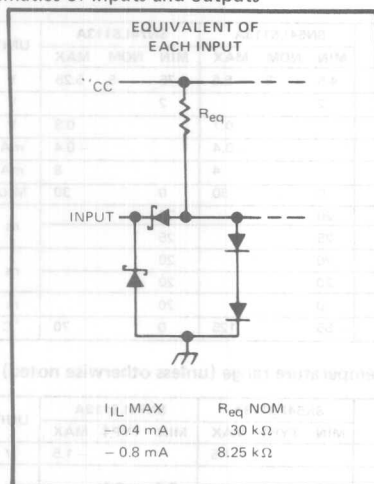


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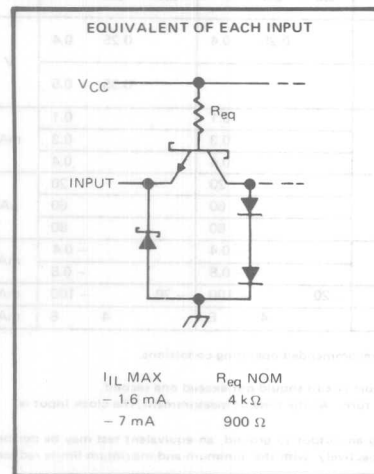
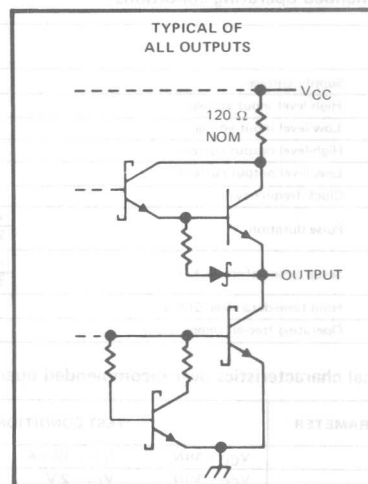
TTL DEVICES

TYPES SN54LS113A, SN54S113A, SN74LS113A, SN74S113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

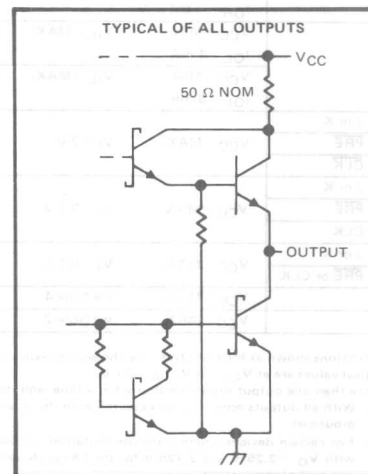
schematics of inputs and outputs



'LS113A



'S113A



3

TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS113A	7 V
'S113A	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS113A, SN74LS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54LS113A			SN74LS113A			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage			0.7			0.8	V		
I _{OH}	High-level output current			−0.4			−0.4	mA		
I _{OL}	Low-level output current			4			8	mA		
f _{clock}	Clock frequency	0		30	0		30	MHz		
t _w	Pulse duration	CLK high			20			ns		
		PRE or CLR low			25					
t _{su}	Setup time before CLK ↓	data high or low			20			ns		
		PRE inactive			20					
t _h	Hold time-data after CLK ↓	0			20			ns		
T _A	Operating free-air temperature	−55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS113A			SN74LS113A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	J or K			0.1			0.1	mA
	PRE			0.3			0.3	
	CLK			0.4			0.4	
I _{IH}	J or K			20			20	μA
	PRE			60			60	
	CLK			80			80	
I _{IL}	J or K			-0.4			-0.4	mA
	PRE or CLK			-0.8			-0.8	
I _{OS} §	V _{CC} = MAX, see Note 4	-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, see Note 2	4	6		4	6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25° C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 2 kΩ, C _L = 15 pF	30	45		MHz
t _{PLH}	PRE or CLK	Q or \bar{Q}			15	20	ns
t _{PHL}					15	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54S113A, SN74S113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54S113A			SN74S113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			− 1			− 1	mA
I _{OL}	Low-level output current			20			20	mA
t _w	Pulse duration	CLK high		6	6		ns	
		CLK low		6.5	6.5			
		PRE low		8	8			
t _{su}	Setup time before CLK ↓	data high or low		7	7		ns	
t _h	Hold time-data after CLK ↓			0	0		ns	
T _A	Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S113A			SN74S113A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA				-1.2			-1.2	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA		2.5	3.4		2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA				0.5			0.5	V
I _I		V _{CC} = MAX, V _I = 5.5 V				1			1	mA
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V				50			50	μA
	PRE or CLK					100			100	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.5 V				-1.6			-1.6	mA
	PRE					-7			-7	
	CLK					-4			-4	
I _{OS} §		V _{CC} = MAX		-40		-100	-40		-100	mA
I _{CC}	Supply Current (average per Flip-Flop)	V _{CC} = MAX, see Note 2		15	25		15	25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{max}					80	125		MHz
t _{PLH}	PRE	Q or \bar{Q}				4	7	ns
t _{PHL}	PRE (CLK high)	\bar{Q} or Q				5	7	ns
	PRE (CLK low)					5	7	
t _{PLH}	CLK	Q or \bar{Q}	R _L = 280 Ω, C _L = 15 pF			4	7	ns
t _{PHL}						5	7	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS114A, SN54S114A, SN74LS114A, SN74S114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

REVISED DECEMBER 1983

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS114A and SN54S114A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS114A and SN74S114A are characterized for operation from 0°C to 70°C .

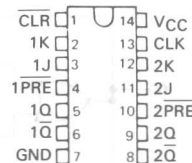
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	\bar{Q}_0

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

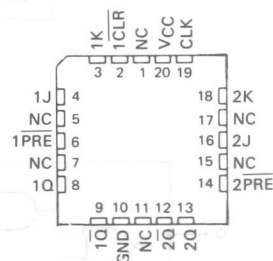
SN54LS114A, SN54S114A ... J OR W PACKAGE
SN74LS114A, SN74S114A ... D, J OR N PACKAGE

(TOP VIEW)



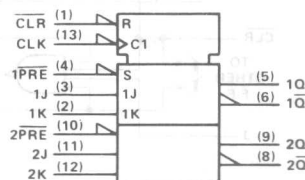
SN54LS114A, SN54S114A ... FK PACKAGE
SN74LS114A, SN74S114A

(TOP VIEW)



NC - No internal connection

logic symbol

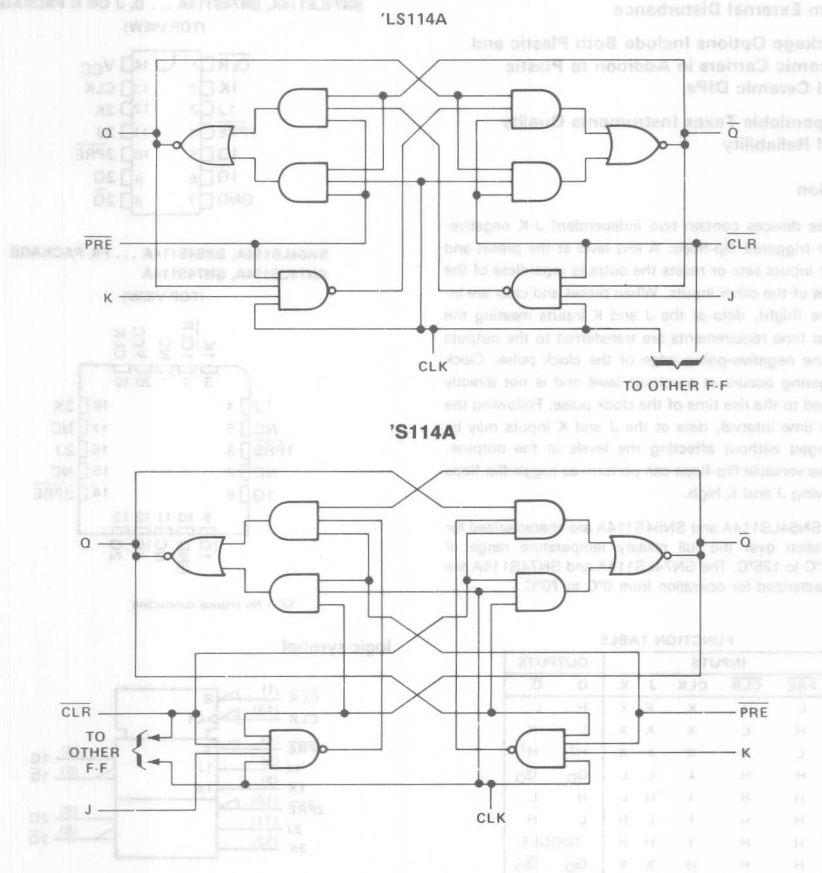


Pin numbers shown on logic notation are for D, J or N packages.

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TEXAS
INSTRUMENTS

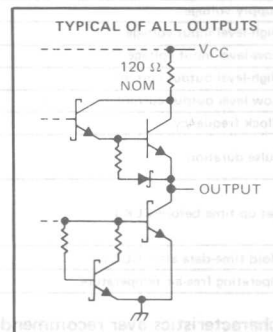
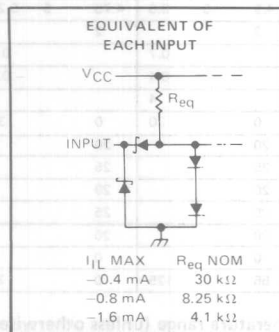
logic diagram



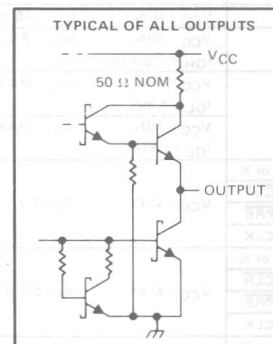
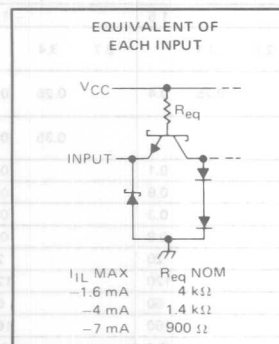
TYPES SN54LS114A, SN54S114A, SN74LS114A, SN74S114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

schematics of inputs and outputs

'LS114A



'S114A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS114A	7 V
'S114A	5.5 V
Operating free air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TTL DEVICES

TYPES SN54LS114A, SN74LS114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SN54LS114A			SN74LS114A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0	30		0	30		MHz
t_w	Pulse duration		20			20		ns
			PRE or CLR low			25		
			data high or low			20		
t_{su}	Set up time-before CLK ↓		25			25		ns
			CLR inactive			20		
			PRE inactive			20		
t_h	Hold time-data after CLK ↓	0			0			ns
T_A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS114A			SN74LS114A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5			-1.5	V
V_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$		2.5	3.4		2.7	3.4		V
V_{OL}		$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$			0.25	0.4		0.25	0.4	V
		$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$						0.35	0.5	
I_I	J or K	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.1			0.1	mA
	CLR					0.6			0.6	
	PRE					0.3			0.3	
	CLK					0.8			0.8	
I_{IH}	J or K	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				20			20	μA
	CLR					120			120	
	PRE					60			60	
	CLK					160			160	
I_{IL}	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.4			-0.4	mA
	CLR					-1.6			-1.6	
	PRE					-0.8			-0.8	
	CLK					-1.6			-1.6	
$I_{OS}§$		$V_{CC} = \text{MAX},$ see Note 4		-20		-100	-20		-100	mA
I_{CC}		$V_{CC} = \text{MAX},$ see Note 2			4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

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TTL DEVICES

TYPES SN54S114A, SN74S114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54S114A			SN74S114A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
t_w	Pulse duration			6			6	ns
				6.5			6.5	
				8			8	
t_{su}	Setup time			7			7	ns
t_h	Hold time-data after CLK↓			0			0	ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S114A			SN74S114A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	J or K			50			50	μA
	CLR			200			200	
	PRE			100			100	
	CLK			200			200	
I_{IL}	J or K			-1.6			-1.6	mA
	CLR			-14			-14	
	PRE			-7			-7	
	CLK			-8			-8	
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40	-100		-40	-100		mA
I_{CC} Supply Current (average per Flip-Flop)	$V_{CC} = \text{MAX},$ see Note 2		15 25			15 25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max}			$R_L = 280\ \Omega, \quad C_L = 15\ \text{pF}$	80	125		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$			4	7	ns
t_{PHL}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high)	$\overline{\text{Q}}$ or Q			5	7	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low)				5	7	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$			4	7	ns
t_{PHL}					5	7	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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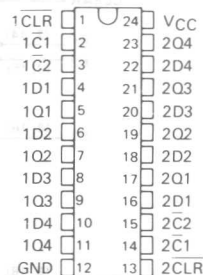
TTL DEVICES

TYPES SN54116, SN74116 DUAL 4-BIT LATCHES WITH CLEAR

DECEMBER 1972—REVISED DECEMBER 1983

- Two Independent 4-Bit Latches in a Single Package
- Separate Clear Inputs Provide One-Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading Register Implementations
- Compatible for Use with TTL Circuits
- Input Clamping Diodes Simplify System Design

SN54116 ... J OR W PACKAGE
SN74116 ... J OR N PACKAGE
(TOP VIEW)



description

These monolithic TTL circuits utilize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

The SN54116 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74116 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(EACH LATCH)

CLEAR	ENABLE		DATA	OUTPUT Q
	C1	C2		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant

Q_0 = the level of Q before these input conditions were established.

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TTL DEVICES

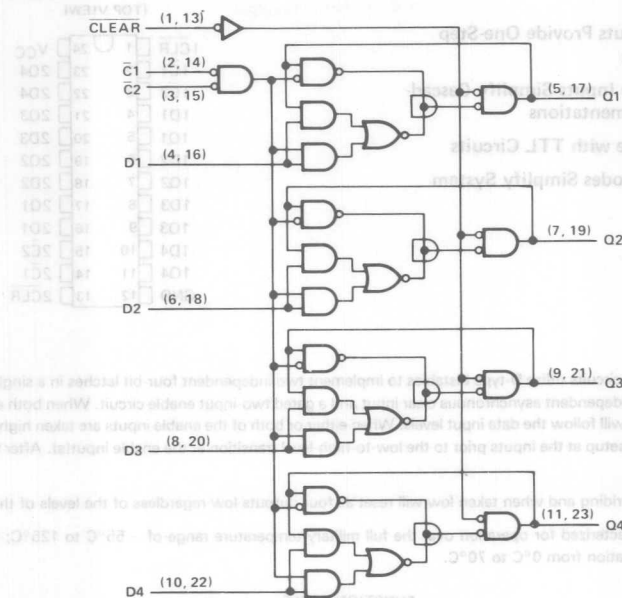
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TYPES SN54116, SN74116 DUAL 4-BIT LATCHES WITH CLEAR

logic diagram

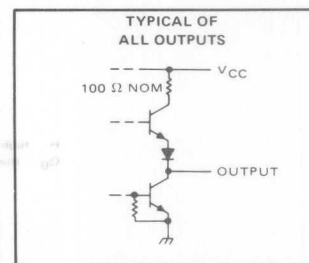
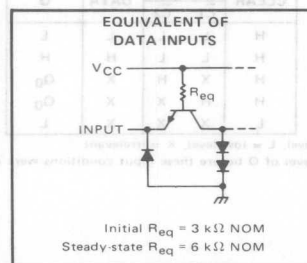
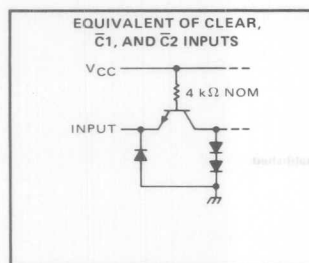


Pin numbers shown on logic notation are for J or N packages.

3

TTL DEVICES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54116 Circuits	-55°C to 125°C
SN74116 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54116, SN74116

DUAL 4-BIT LATCHES WITH CLEAR

recommended operating conditions

		SN54116			SN74116			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}		-800			-800			μA
Low-level output current, I _{OL}		16			16			mA
Input pulse width, t _W	C ₁ , C ₂	18			18			ns
	CLR	18			18			
Data setup time, t _{su}	High logic level	8			8			ns
	Low logic level	14			14			
Clear inactive-state setup time, t _{su}		8			8			ns
Data release time, high-level data, t _{release}		2			2			ns
Data hold time, low-level data, t _h		8			8			
Operating free-air temperature, T _A		-55			0			70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4			V
V_{OL}	Low level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		mA
I_{IH}	High-level input current	$\bar{C}1, \bar{C}2$, or clear	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40		μ A
		Any D			60		
I_{IL}	Low-level input current	$\bar{C}1, \bar{C}2$, or clear	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6		mA
		Any D, initial peak			-2.4		
		Any D, steady-state			-1.6		
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54116	-20		-57	mA
			SN74116	-18		-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	Condition A		60	100	mA
			Condition B		40	70	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 2: With outputs open, I_{CC} is measured for the following conditions:

A. All inputs grounded.

B. All \bar{C} inputs are grounded and all other inputs are at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$\overline{C}1$ or $\overline{C}2$	Any Q	$C_L = 15\text{ pF},$ $R_L = 400\ \Omega,$ See Figure 1		19	30	ns
t_{PHL}					15	22	
t_{PLH}	Data	Q			10	15	ns
t_{PHL}					12	18	
t_{PHL}	\overline{CLR}	Any Q			15	22	ns

TYPES SN54116, SN74116 DUAL 4-BIT LATCHES WITH CLEAR

PARAMETER MEASUREMENT INFORMATION

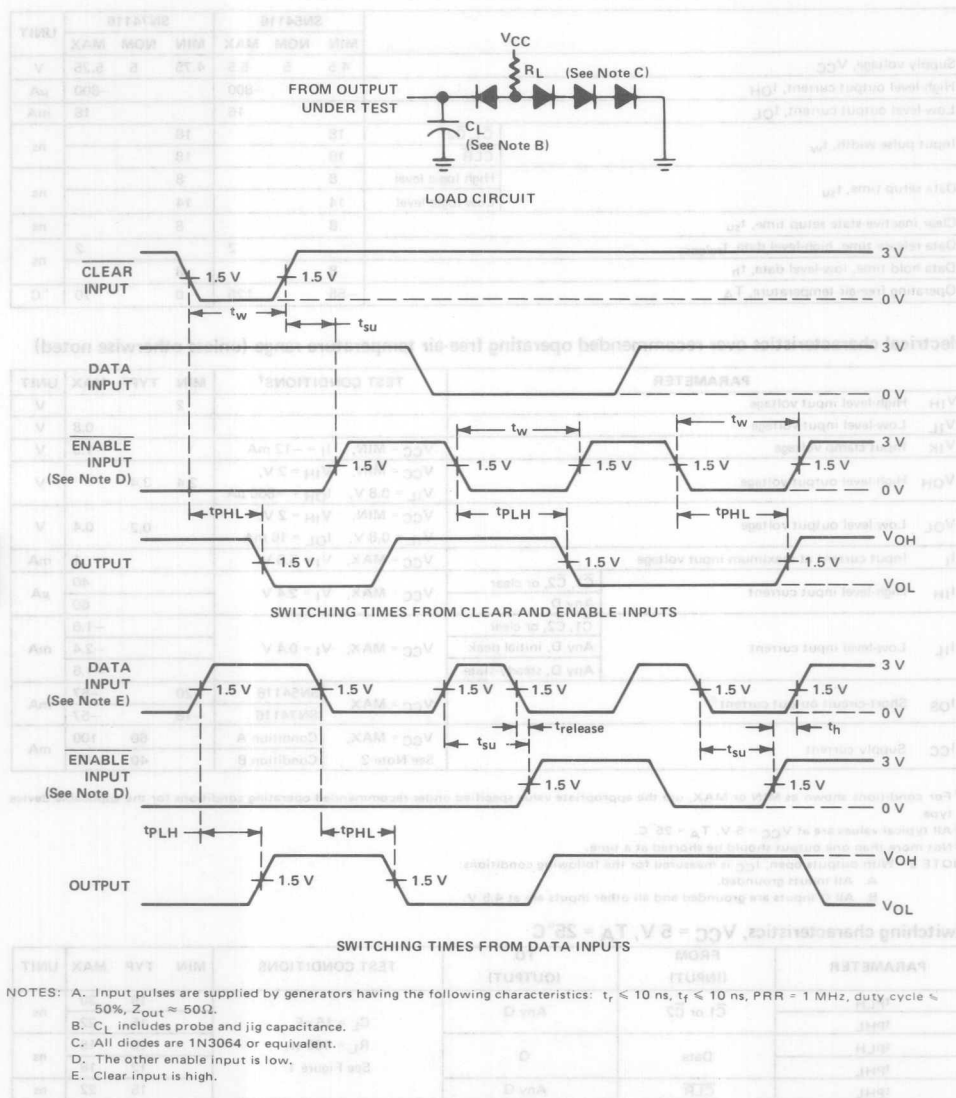


FIGURE 1

TYPES SN54120, SN74120 DUAL PULSE SYNCHRONIZERS/DRIVERS

SEPTEMBER 1971 REVISED DECEMBER 1983

- Generates Either a Single Pulse or Train of Pulses Synchronized with Control Functions
- Ideal for Implementing Sync-Control Circuits Similar to those Used in Oscilloscopes
- Latched Operation Ensures that Output Pulses Are Not Clipped
- High-Fan-Out Complementary Outputs Drive System Clock Lines Directly
- Internal Input Pull-Up Resistors Eliminate Need for External Components
- Diode-Clamped Inputs Simplify System Design
- Typical Propagation Delays:

9 Nanoseconds through One Level
16 Nanoseconds through Two Levels

description

These monolithic pulse synchronizers are designed to synchronize an asynchronous or manual signal with a system clock. Reliable response is ensured as the input signals are latched up; therefore duration of logic input is not critical and the adverse effects of contact-bounce of a manual input are eliminated. The ability to pass output pulses is started and stopped by the levels or pulses applied to the latch inputs $\bar{S}1$, $\bar{S}2$, or \bar{R} in accordance with the function table. High-speed circuitry is utilized throughout the clock paths to minimize skew with respect to the system clock.

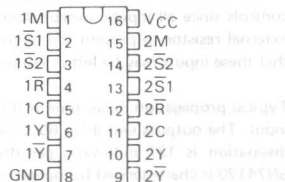
After initiation, the mode control (M) input determines whether a series of pulses or only one pulse is passed. In the absence of a stop command, the clock driver will continue to pass clock pulses as long as the mode control input is low (see Figures 2 through 4). If the mode control input is high only a single clock pulse will be passed (see Figure 5).

When the mode control is set to pass a series of pulses, the last pulse out is determined by two general rules:

- When pulses are terminated by the \bar{S} or \bar{R} inputs, conditions meeting the setup times (specified under recommended operating conditions) will dominate.
- Low-to-high-level transitions at the mode control input should be avoided during the 20-nanosecond period immediately following the negative transition of the input clock pulse as transitions during this time period may or may not allow the next pulse to pass (see Figures 4 and 5). When pulses are terminated by the mode control input, a positive transition at the mode control input meeting the high-level setup time, t_{SH} (H), (specified under recommended operating conditions) will pass that positive clock pulse then inhibit remaining clock pulses. The clock input (C) is latch-controlled ensuring that once initiated the output pulse will not be terminated until the full pulse has been passed.

SN54120 . . . J OR W PACKAGE
SN74120 . . . J OR N PACKAGE

(TOP VIEW)



FUNCTION TABLE

INPUTS			FUNCTION
\bar{R}	$\bar{S}1$	$\bar{S}2$	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	H	H	Inhibit Output Pulses
H	↓	H	Start Output Pulses
H	H	↓	Start Output Pulses
↓	H	H	Stop Output Pulses
H	H	H	Continue†

H = high level (steady state)

L = low level (steady state)

↓ = transition from H to L

X = irrelevant

† Operation initiated by last ↓ transition continues.

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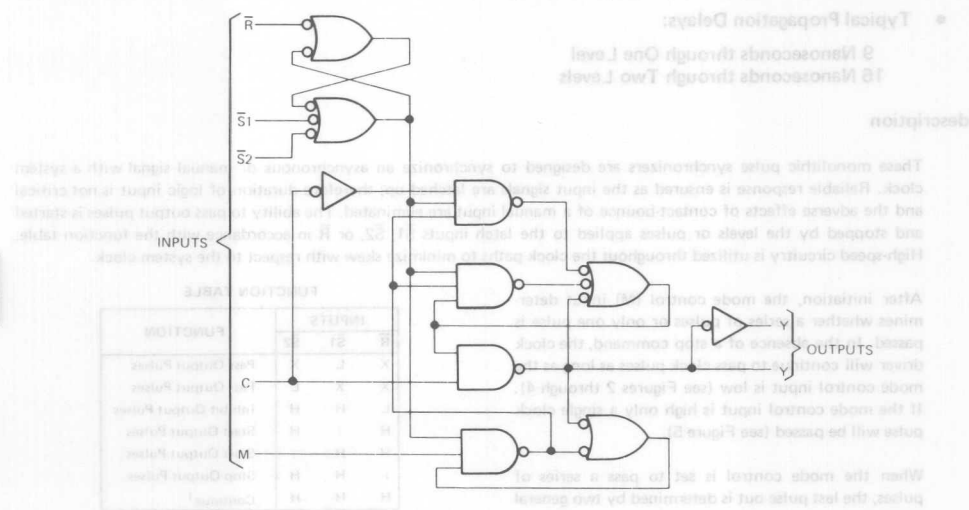
TYPES SN54120, SN74120 DUAL PULSE SYNCHRONIZERS/DRIVERS

description (continued)

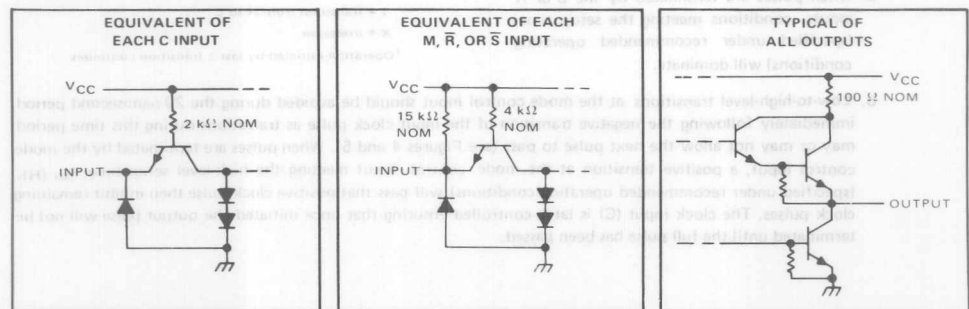
This clock driver circuit is entirely compatible for use with either digital logic circuits or mechanical switches for input controls since all inputs, except the clock, have internal pull-up resistors. This eliminates the requirement to supply an external resistor to prevent the input from floating when the control switch is open. The internal resistor also means that these inputs may be left disconnected if unused.

Typical propagation delay time is 9 nanoseconds to the \bar{Y} output and 16 nanoseconds to the Y output from the clock input. The outputs will drive 60 Series 54/74 loads at a high logic level and 30 loads at a low logic level. Typical power dissipation is 127 milliwatts per driver. The SN54120 is characterized for operation from -55°C to 125°C ; the SN74120 is characterized for operation from 0°C to 70°C .

logic diagram (each driver)



schematics of inputs and outputs



TYPES SN54120, SN74120

DUAL PULSE SYNCHRONIZERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature: SN54120 Circuits	-55°C to 125°C
SN74120 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the S1 and S2 inputs.

recommended operating conditions

				SN54120			SN74120			UNIT		
				MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, V_{CC}				4.5	5	5.5	4.75	5	5.25	V		
High-level output current, I_{OH}				-2.4			2.4			mA		
Low-level output current, I_{OL}				48			48			mA		
Setup time (see Figures 2 thru 5)	Any input except mode control, $t_{su}(H \text{ or } L)$			12			12			ns		
	Mode control	$t_{su}(H)$		0			0					
		$t_{su}(L)$		12			12					
Hold time (see Figures 3 and 5)	Any input except mode control, $t_h(H \text{ or } L)$			3			3			ns		
	Mode control, $t_h(H \text{ or } L)$			20			20					
Operating free-air temperature, T_A				-55			125			0	70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = 12 \text{ mA}$				1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = 2.4 \text{ mA}$	2.4	3.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 48 \text{ mA}$		0.2	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Clock input				80	μA
		Other inputs	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	0.12	0.2	0.36	mA
I_{IL}	Low-level input current	Clock input				3.2	mA
		Other inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			2.1	mA
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		35		90	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		51		90	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with ground applied to all inputs except R which is at 4.5 V and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

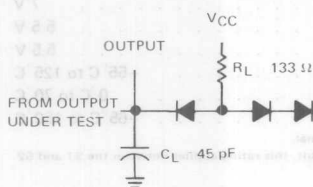
PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C	Y	$C_L = 45 \text{ pF}, R_L = 133 \Omega$ See Figure 1		14	22	ns
t_{PHL}					17	25	
t_{PLH}	C	\bar{Y}			10	16	ns
t_{PHL}					8	13	

[¶] t_{PLH} Propagation delay time, low to high level output

t_{PHL} Propagation delay time, high to low level output

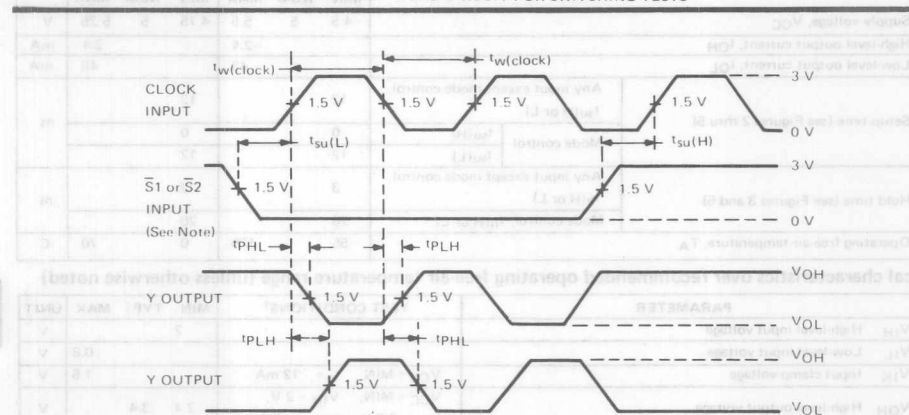
TYPES SN54120, SN74120 DUAL PULSE SYNCHRONIZERS/DRIVERS

PARAMETER MEASUREMENT INFORMATION



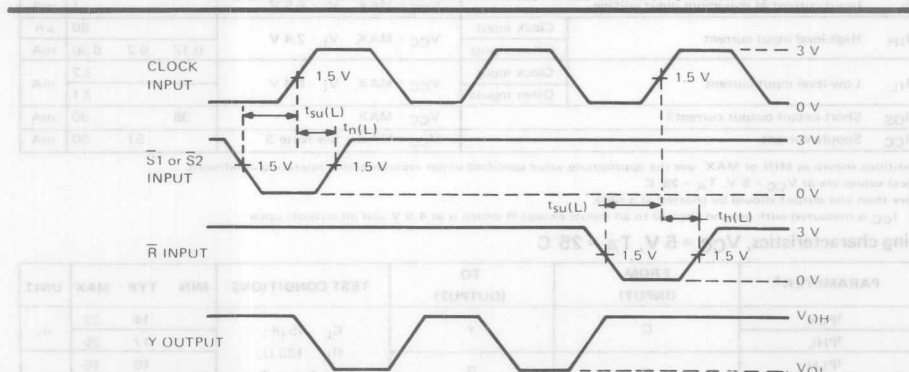
- NOTES: A. The clock input pulse in Figures 2 through 5 is supplied by a generator having the following characteristics: $t_w(\text{clock}) = 15$ ns, PRR = 1 MHz, and $Z_{out} = 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1—LOAD CIRCUIT FOR SWITCHING TESTS



NOTE: Mode control and \bar{R} inputs are low and unused \bar{S} input is high.

FIGURE 2—INITIATING AND TERMINATING PULSE TRAIN FROM S INPUTS



NOTE: Mode control input is low and unused \bar{S} input is high.

FIGURE 3—INITIATING PULSE TRAIN FROM S AND TERMINATING WITH R INPUTS

PARAMETER MEASUREMENT INFORMATION

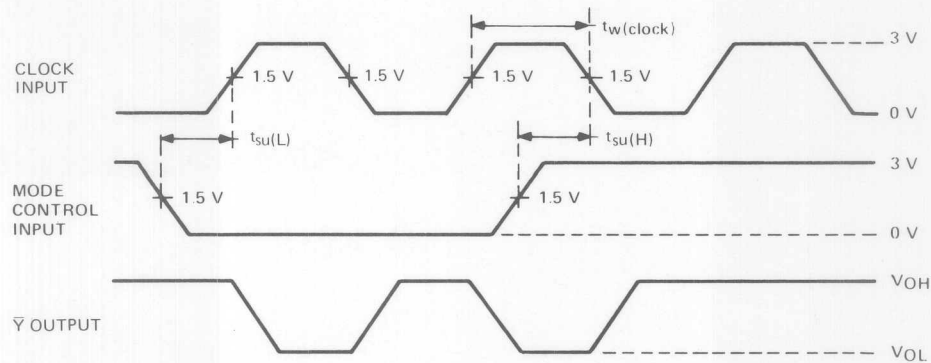


FIGURE 4—INITIATING AND TERMINATING PULSE TRAIN WITH MODE CONTROL INPUT

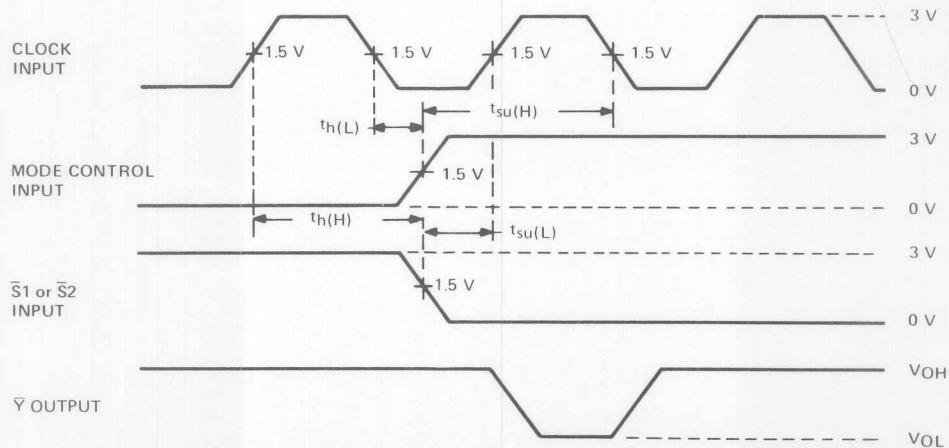
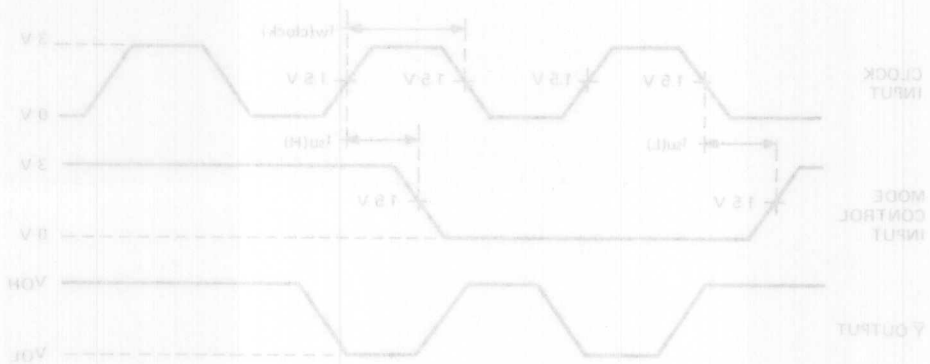


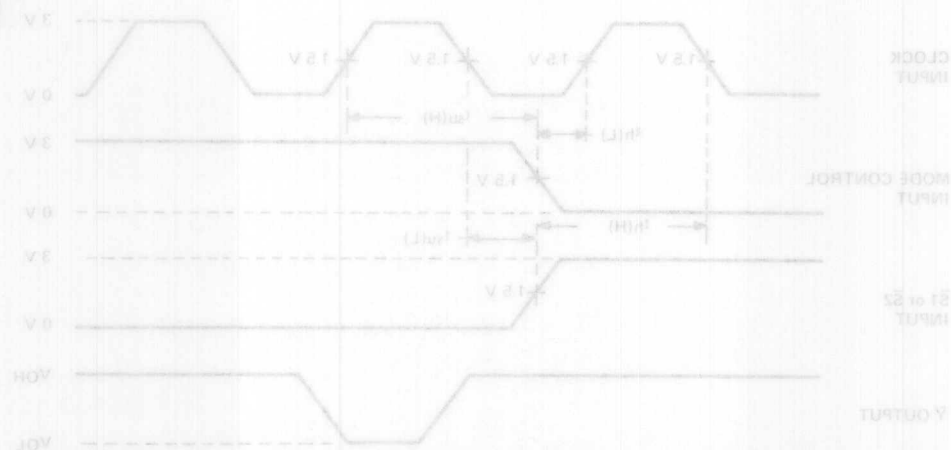
FIGURE 5—ENABLING SINGLE PULSE

PARAMETER MEASUREMENT INFORMATION



NOTE: All input and output signals are 100% duty cycle.

FIGURE 4—PULSING AND TERMINATING PULSE TRAIN WITH MODE CONTROL INPUT



NOTE: Input B is low and the output is high.

FIGURE 5—ENABLING SINGLE PULSE

3

TTL DEVICES

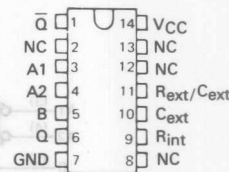
TYPES SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

REVISED MAY 1983

- Programmable Output Pulse Width
With $R_{int} \dots 35 \text{ ns Typ}$
With $R_{ext}/C_{ext} \dots 40 \text{ ns to 28 Seconds}$
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

SN54121 ... J OR W PACKAGE
SN74121 ... J OR N PACKAGE

(TOP VIEW)



NC - No internal connection.

FUNCTION TABLE			
INPUTS			OUTPUTS
A1	A2	B	Q Q̄
L	X	H	L H
X	L	H	L↑ H↑
X	X	L	L↑ H↑
H	H	X	L↑ H↑
H	L	H	[Pulse]
L	H	H	[Pulse]
L	L	H	[Pulse]
L	X	↑	[Pulse]
X	L	↑	[Pulse]

For explanation of function table symbols, see page

† These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC} , C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54121 and 2 k Ω to 40 k Ω for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_{TIn2} \approx 0.7 C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

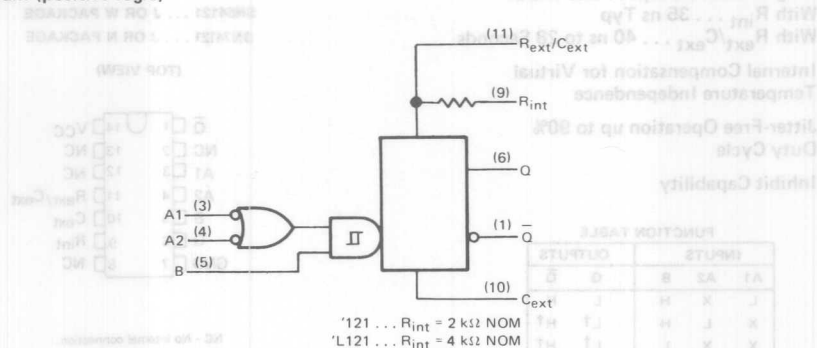
PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-359

TYPES SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

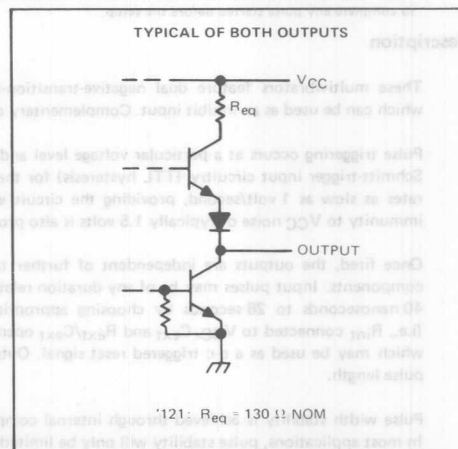
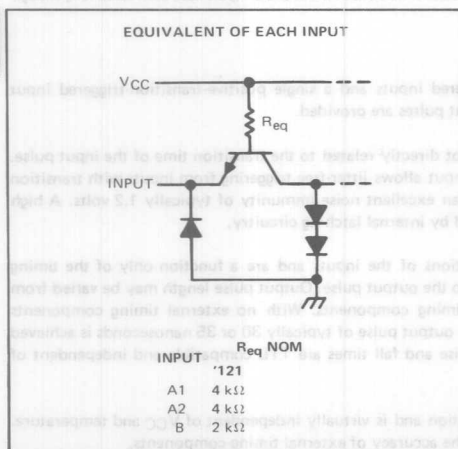
logic diagram (positive logic)



schematics of inputs and outputs

3

TTL DEVICES



TYPES SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) '121	7 V
Input voltage:	5.5 V
Operating free-air temperature range: SN54121	– 55°C to 125°C
SN74121	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54121 SN74121			UNIT	
				MIN	NOM	MAX		
V _{CC}	Supply voltage			54 Family	4.5	5	5.5	V
				74 Family	4.75	5	5.25	
I _{OH}	High-level output current						− 0.4	mA
I _{OL}	Low-level output current						16	mA
dv/dt	Rate of rise or fall of input pulse	Schmitt input, B			1			V/s
		Logic inputs, A1, A2			1			V/μs
t _{W(in)}	Input pulse width				50			ns
R _{ext}	External timing capacitance			54 Family	1.4		30	kΩ
				74 Family	1.4		40	
C _{ext}	External timing capacitance				0		1000	μF
	Duty cycle	R _T = 2 kΩ					67	%
		R _T = MAX R _{ext}					90	
T _A	Operating free-air temperature			54 Family	− 55		125	°C
				74 Family	0		70	

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TTL DEVICES

TYPES SN54121, SN74121 **MONOSTABLE MULTIVIBRATORS** **WITH SCHMITT-TRIGGER INPUTS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54121 SN74121			UNIT
		MIN	TYP‡	MAX	
V_{T+} Positive-going threshold voltage at A input	$V_{CC} = \text{MIN}$		1.4	2	V
V_{T-} Negative-going threshold voltage at A input	$V_{CC} = \text{MIN}$	0.8	1.4		V
V_{T+} Positive-going threshold voltage at B input	$V_{CC} = \text{MIN}$		1.55	2	V
V_{T-} Negative-going threshold voltage at B input	$V_{CC} = \text{MIN}$	0.8	1.35		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = \text{MAX}$	0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$	A1 or A2		40	μA
		B		80	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	A1 or A2		-1.6	mA
		B		-3.2	
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$	54 Family	-20	-55	mA
		74 Family	-18	-55	
		Quiescent	13	25	
I_{CC} Supply current	$V_{CC} = \text{MAX}$	Triggered	23	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

* Not more than one output should be shorted at a time.

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TTL DEVICES

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		'121			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level Q output from either A input	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$ for '121, See Note 2	$C_{ext} = 80 \text{ pF}$, $R_{int} \text{ to } V_{CC}$	45	70	ns	
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input			35	55	ns	
t_{PHL}	Propagation delay time, high-to-low-level \bar{Q} output from either A input			50	80	ns	
t_{PHL}	Propagation delay time, high-to-low-level \bar{Q} output from B input			40	65	ns	
$t_{w(out)}$	Pulse width obtained using internal timing resistor		$C_{ext} = 80 \text{ pF}$, $R_{int} \text{ to } V_{CC}$	70	110	150	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance		$C_{ext} = 0$, $R_{int} \text{ to } V_{CC}$	30	50		ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		$C_{ext} = 100 \text{ pF}$, $R_T = 10 \text{ k}\Omega$	600	700	800	ns
			$C_{ext} = 1 \mu\text{F}$, $R_T = 10 \text{ k}\Omega$	6	7	8	ms

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

TYPICAL CHARACTERISTICS

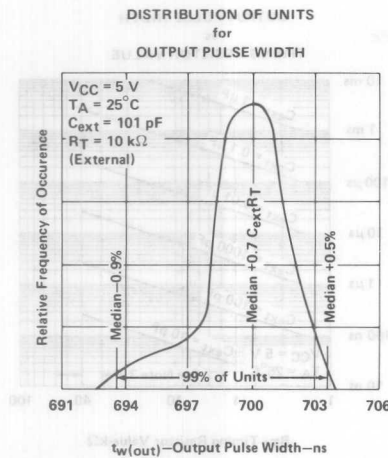


FIGURE 1

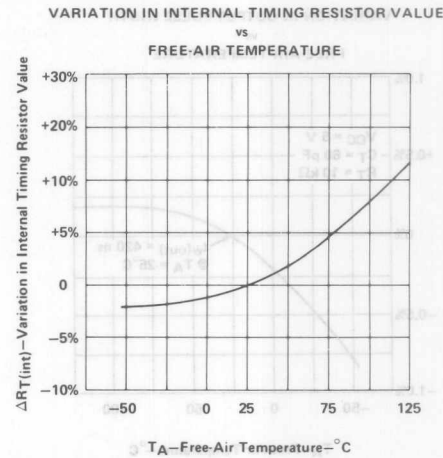


FIGURE 2

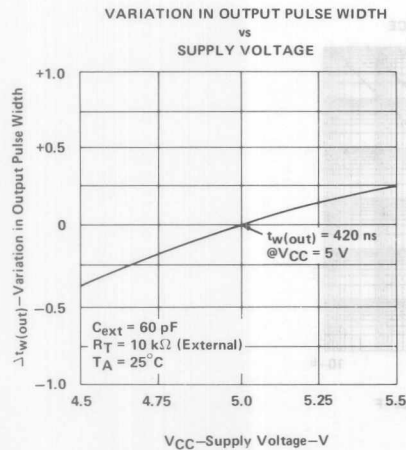


FIGURE 3

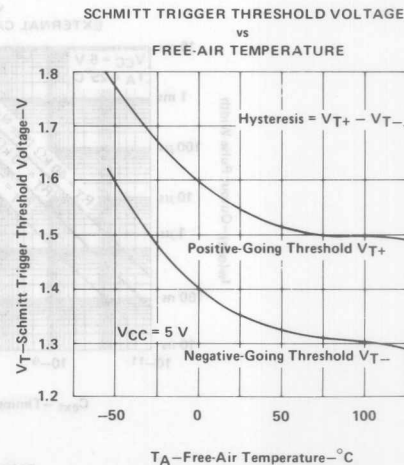


FIGURE 4

§ Data for temperatures below 0°C and above 70°C are applicable for SN54121.

TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

TYPICAL CHARACTERISTICS[§] (continued)

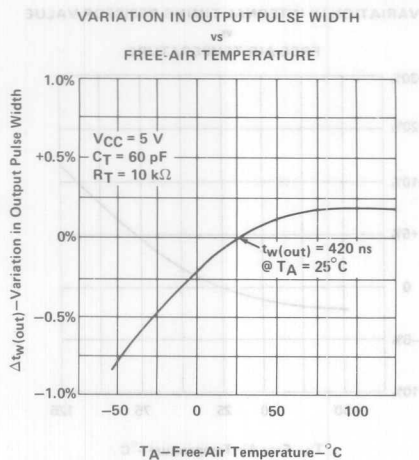


FIGURE 5

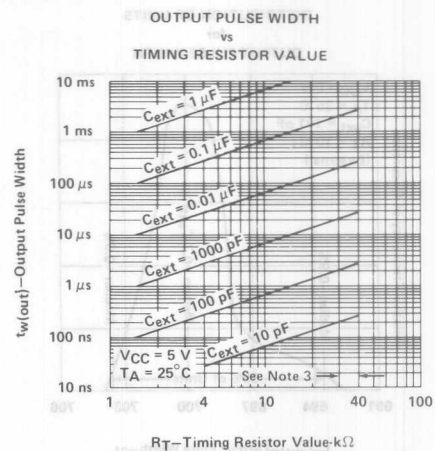


FIGURE 6

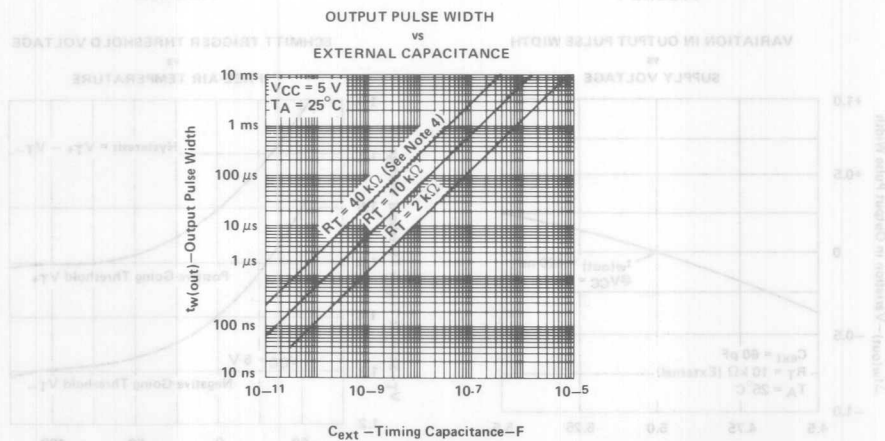


FIGURE 7

NOTE 3: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54LS121.
[§]Data for temperatures below 0°C and above 70°C are applicable for SN54121.

3

TTL DEVICES

SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

REVISED DECEMBER 1983

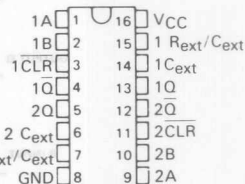
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- '122, 'L122, 'LS122 Have Internal Timing Resistors

SN54123, SN54130, SN54LS123 ... J OR W PACKAGE

SN74123, SN74130 ... J OR N PACKAGE

SN74LS123 ... D, J OR N PACKAGE

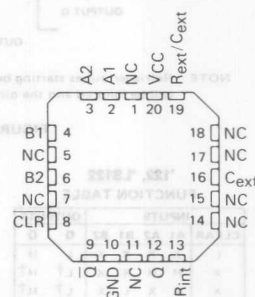
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS122 ... FK PACKAGE

SN74LS122

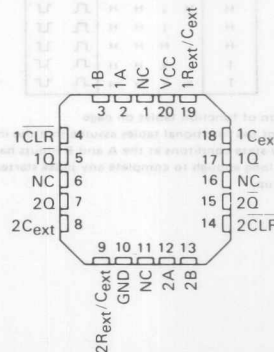
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS123 ... FK PACKAGE

SN74LS123

(TOP VIEW) (SEE NOTES 1 THRU 4)



NC No internal connection

description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

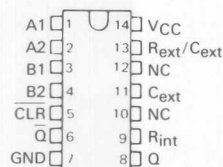
The R_{int} is nominally 10 k ohms for '122, 'LS122.

SN54122, SN54LS122 ... J OR W PACKAGE

SN74122 ... J OR N PACKAGE

SN74LS122 ... D, J OR N PACKAGE

(TOP VIEW) (SEE NOTES 1 THRU 4)



- NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122, or 'LS122, connect R_{int} to V_{CC} .
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC} .

PRODUCTION DATA

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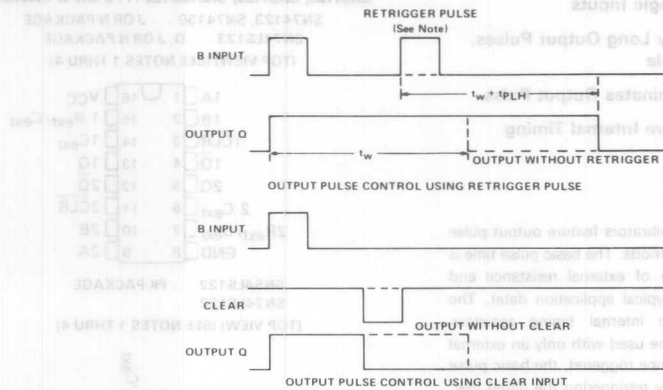


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TTL DEVICES

SN54122, SN54123, SN54130, SN54LS122, SN54LS123, SN74122, SN74123, SN74130, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

description (continued)



NOTE: Retrigger pulses starting before $0.22 C_{EXT}$ (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output pulse will remain unchanged.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

'122, 'LS122
FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L [†]	H [†]
X	X	X	L	X	L [†]	H [†]
X	X	X	X	L	L [†]	H [†]
H	L	X	†	H	U	U
H	L	X	H	†	U	U
H	X	L	†	H	U	U
H	X	L	H	†	U	U
H	H	†	†	H	U	U
H	H	†	H	†	U	U
H	†	†	†	H	U	U
H	†	†	H	†	U	U
†	X	X	X	X	U	U
†	X	L	H	H	U	U

See explanation of function tables on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

'123, '130, 'LS123
FUNCTION TABLE

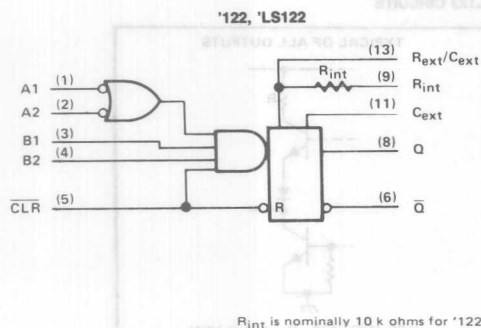
CLEAR	INPUTS		OUTPUTS	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L [†]	H [†]
X	X	L	L [†]	H [†]
H	L	†	U	U
H	†	†	U	U
H	†	H	U	U
H	H	†	U	U

3

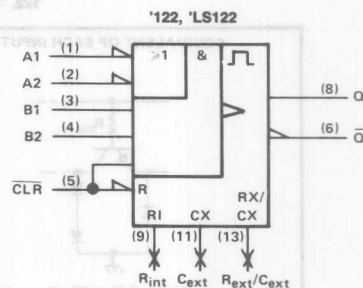
TTL DEVICES

**SN54122, SN54123, SN54130, SN54LS122, SN54LS123,
SN74122, SN74123, SN74130, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

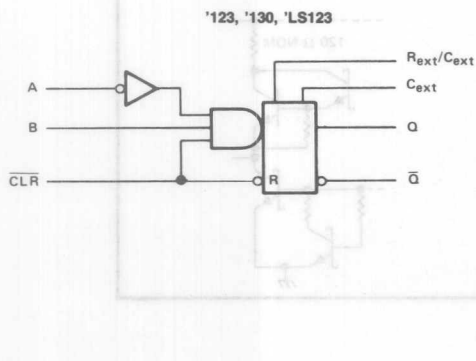
logic diagram



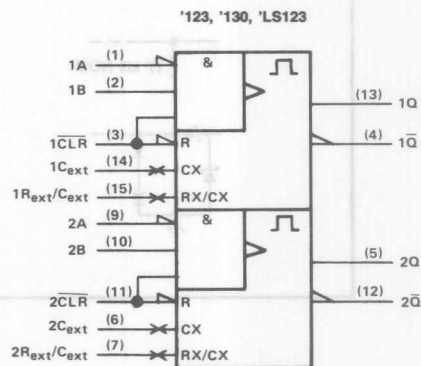
logic symbol



logic diagram (each multivibrator)



logic symbol

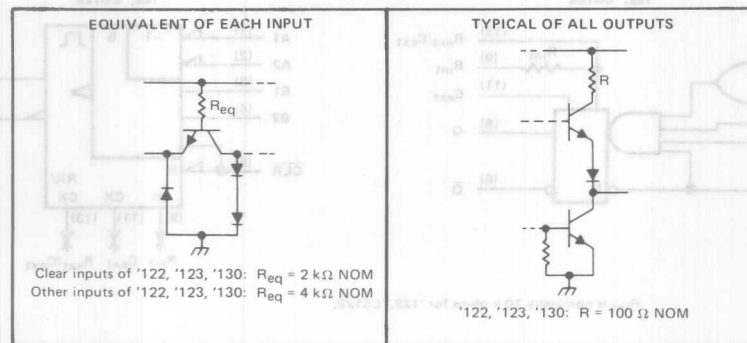


Pin numbers shown on logic notation are for D, J or N packages.

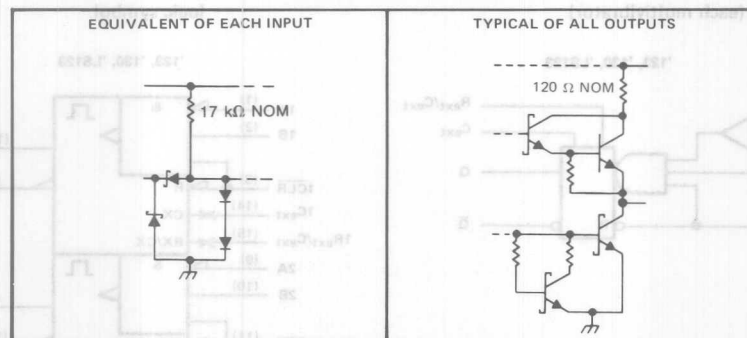
**SN54122, SN54123, SN54130, SN54LS122, SN54LS123,
SN74122, SN74123, SN74130, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

schematics of inputs and outputs

'122, '123, '130, 'L123 CIRCUITS



'LS122, 'LS123 CIRCUITS



3

TTL DEVICES

TYPES SN54122, SN54123, SN54130, SN74122, SN74123, SN74130 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Pulse width, t_W	40			40			ns
External timing resistance, R_{ext}	5		25	5		50	k Ω
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'122			'123, '130			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -800 \mu\text{A}$, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 16 \text{ mA}$, See Note 1		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	Data inputs			40			40	μ A
	Clear input			80			80	μ A
I_{IL} Low-level input current	Data inputs			-1.6			-1.6	mA
	Clear input			-3.2			-3.2	mA
I_{OS} Short-circuit output current*	$V_{CC} = \text{MAX}$, See Note 5	-10		-40	-10		-40	mA
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX}$, See Notes 6 and 7	23		36	46		66	mA

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

* Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q. C_{ext} is open to measure V_{OH} at \bar{Q} , V_{OL} at Q, or I_{OS} at \bar{Q} .
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{ext} = 0.02 \mu\text{F}$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of '122 is open.

7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{ext} = 0.02 \mu\text{F}$, and $R_{ext} = 25 \text{ k}\Omega$. R_{int} of '122 is open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, see note 8

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122, '130			'123			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	$C_{ext} = 0$, $C_L = 15 \text{ pF}$, $R_{ext} = 5 \text{ k}\Omega$, $R_L = 400 \Omega$	22	33		22	33		ns
	B	Q		19	28		19	28		
t_{PHL}	A	\bar{Q}		30	40		30	40		ns
	B	\bar{Q}		27	36		27	36		
t_{PHL}	Clear	\bar{Q}		18	27		18	27		ns
t_{PLH}	Clear	Q		30	40		30	40		
t_{WQ} (min)	A or B	Q	$C_{ext} = 1000 \text{ pF}$, $C_L = 15 \text{ pF}$, $R_{ext} = 10 \text{ k}\Omega$, $R_L = 400 \Omega$	45	65		45	65		ns
t_{WQ}	A or B	Q		3.08	3.42	3.76	2.76	3.03	3.37	μ s

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{WQ} = width of pulse at output Q

NOTE 8: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	k Ω
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX}, \text{ See Note 13}$		6	11		6	11	mA
			12	20		12	20	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 12. To measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at Q, ground R_{ext}/C_{ext} , apply 2 V to B and clear, and pulse A from 2 V to 0 V.

13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ (see note 8)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_{ext} = 0, R_{ext} = 5 \text{ k}\Omega, C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	23	33		ns
	B	Q		23	44		
t_{PHL}	A	Q		32	45		ns
	B	Q		34	56		
t_{PLH}	Clear	Q	$C_{ext} = 1000 \text{ pF}, R_{ext} = 10 \text{ k}\Omega, C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	20	27		ns
	Clear	Q		28	45		
$t_{wQ} \text{ (min)}$	A or B	Q		116	200		ns
t_{wQ}	A or B	Q		4	4.5	5	μ s

§ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{wQ} = width of pulse at output Q

NOTE 8: See General Information Section for load circuits and voltage waveforms.

**TYPES SN54122, SN54123, SN54130,
SN74122, SN74123, SN74130
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse widths when $C_{ext} \leq 1000$ pF, See Figures 4 and 5.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

where

K is 0.32 for '122, 0.28 for '123, '130

R_T is in $K\Omega$ (internal or external timing resistance.)

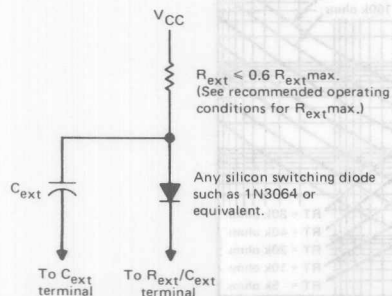
C_{ext} is in pF

t_w is in nanoseconds

To prevent reverse voltage across C_{ext} , it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

$$t_w = K_D \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

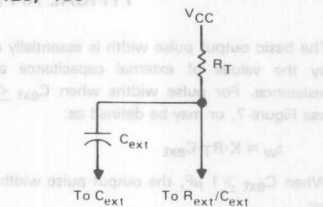
K_D is 0.28 for '122, 0.25 for '123, '130



**TIMING COMPONENT CONNECTIONS WHEN
 $C_{ext} > 1000$ pF AND CLEAR IS USED**

FIGURE 2

Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.



**TIMING COMPONENT CONNECTIONS
FIGURE 3**

**'122, '123, '130
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE**

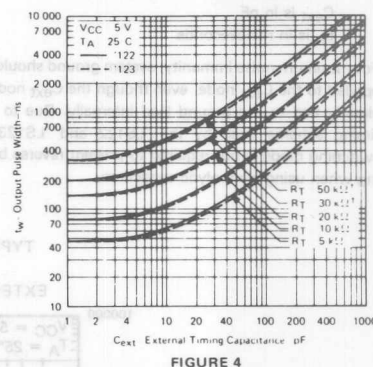


FIGURE 4

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' and SN54L' circuits.

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TTL DEVICES

TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF, use Figure 7, or may be defined as:

$$t_w \approx K \cdot R_T \cdot C_{ext}$$

When $C_{ext} \geq 1$ μ F, the output pulse width is defined as:

$$t_w \approx 0.33 \cdot R_T \cdot C_{ext}$$

Where

K is multiplier factor, see Figure 8
 R_T is in K ohms (internal or external timing resistance)
 C_{ext} is in pF
 t_w is in nanoseconds

For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.

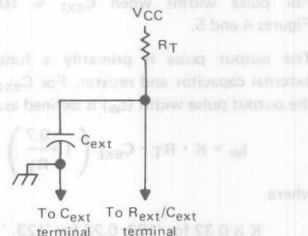
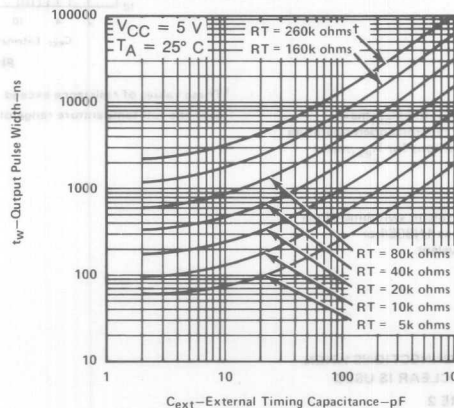


FIGURE 6
TIMING COMPONENT CONNECTIONS

'LS122, 'LS123
TYPICAL OUTPUT PULSE WIDTH
VS
EXTERNAL TIMING CAPACITANCE



[†] This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 7

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TTL DEVICES

TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123†

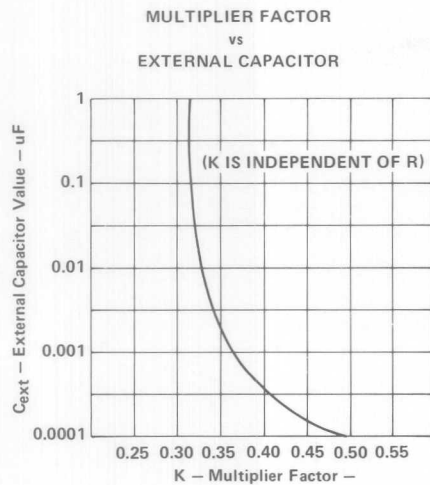


FIGURE 8

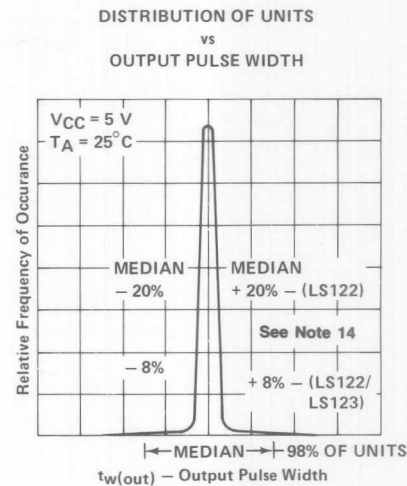


FIGURE 9

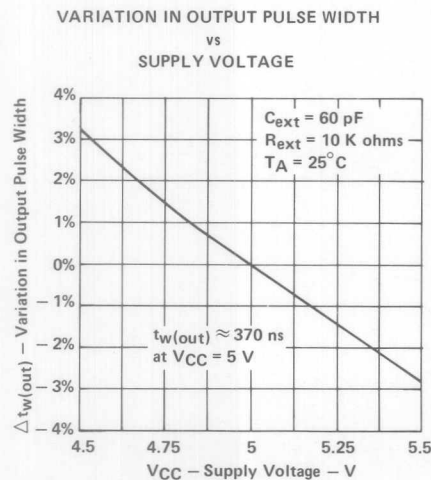


FIGURE 10

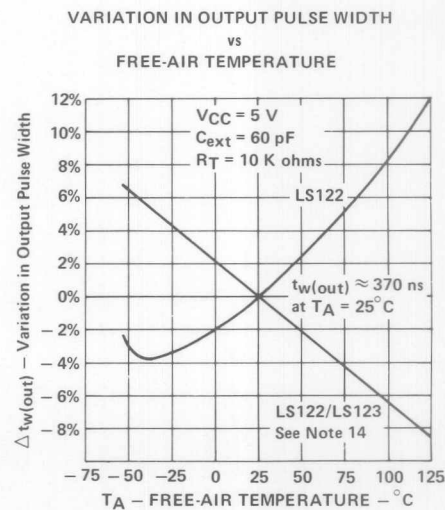


FIGURE 11

NOTE 14: For the 'LS122, the internal timing resistor, R_{int} , was used. For the 'LS122/123, an external timing resistor was used for R_T .
†Data for temperatures below $0^\circ C$ and above $70^\circ C$ and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS122 and SN54LS123 only.

TYPICAL APPLICATION DATA FOR 'LS123, 'ALS123

MULTIPLIER FACTOR
vs
EXTERNAL CAPACITOR

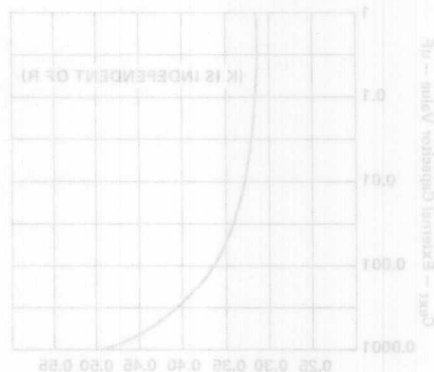


FIGURE 8

DISTRIBUTION OF UNITS
vs
OUTPUT PULSE WIDTH

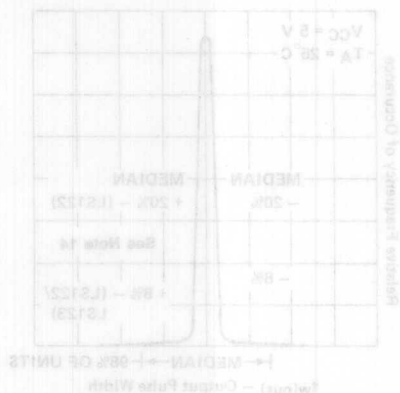


FIGURE 9

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

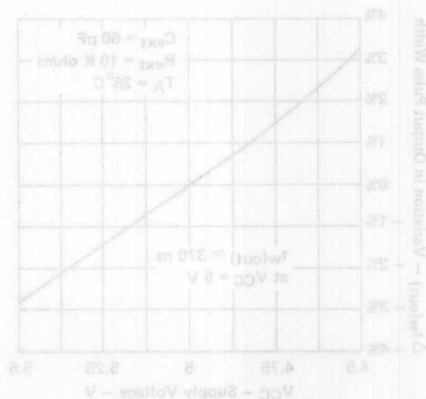


FIGURE 10

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE AIR TEMPERATURE

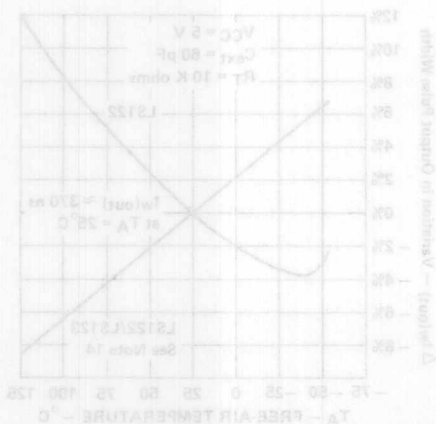


FIGURE 11

NOTE 14: For the LS123, the internal timing network, R_{int} and C_{int} are used. For the ALS123, an external timing network is used for R_{ext} . Values for temperatures below 0°C and above 125°C and for supply voltages below 4.5 V and above 5.5 V are not applicable for SN74LS123 and SN74ALS123 only.

3 TTL DEVICES

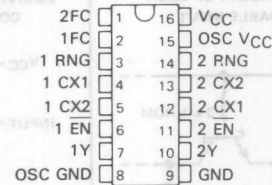
TYPES SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

MARCH 1974 — REVISED DECEMBER 1983

- Two Independent VCO's in a 16-Pin Package
- Output Frequency Set by Single External Component:
 - Crystal for High-Stability Fixed-Frequency Operation
 - Capacitor for Fixed- or Variable-Frequency Operation
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges
- Typical f_{max} 85 MHz
Typical Power Dissipation 525 mW
- Frequency Spectrum . . . 1 Hz to 60 MHz

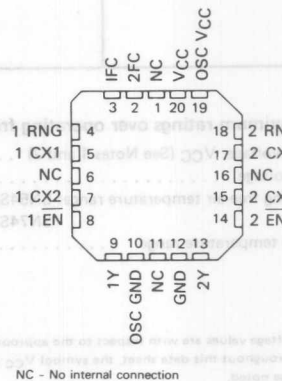
SN54S124 . . . J OR W PACKAGE
SN74S124 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54S124 . . . FK PACKAGE
SN74S124

(TOP VIEW)



NC - No internal connection

description

The 'S124 features two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. Under the conditions used in Figure 3, the output frequency can be approximated as follows:

$$f_o = \frac{5 \times 10^{-4}}{CX}$$

where: f_o = output frequency in hertz

CX = external capacitance in farads.

logic

While the enable input is low, the output is enabled.
While the enable input is high, the output is high.

These devices can operate from a single 5-volt supply. However, one set of supply-voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set (V_{CC} and GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system.

The enable input of these devices starts or stops the output pulses when it is low or high, respectively. The internal oscillator of the 'S124 is started and stopped by the enable input. The enable input is one standard load; it and the buffered output operate at standard Schottky-clamped TTL levels.

The pulse synchronization-gating section ensures that the first output pulse is neither clipped nor extended. Duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54S124 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74S124 is characterized for operation from 0°C to 70°C .

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

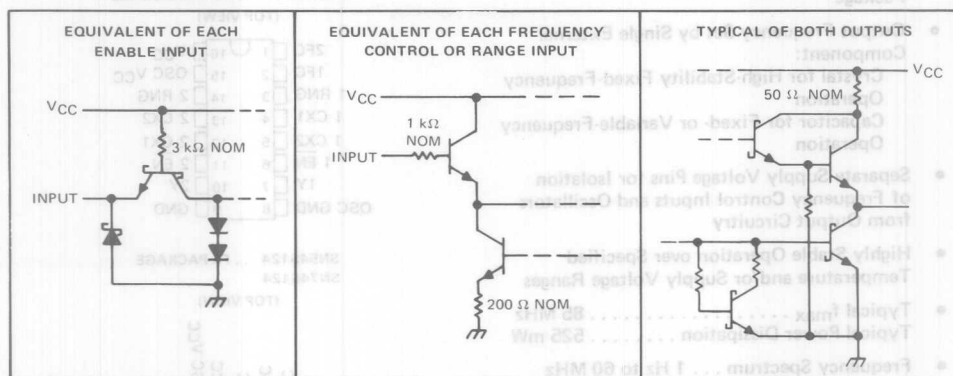
3-375

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TTL DEVICES

TYPES SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Notes 1 and 2)	7V
Input voltage	5.5 V
Operating free-air temperature range: SN54S124	-55°C to 125°C
SN74S124	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to the appropriate ground terminal.
2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and \overline{V}_{CC} terminals, unless otherwise noted.

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TTL DEVICES

TYPES SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

recommended operating conditions

	SN54S124			SN74S124			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	1		5	1		5	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Output frequency (enabled), f_O	1			1			Hz
		60			60		MHz
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage at enable			2			V
V_{IL}	Low-level input voltage at enable					0.8	V
V_{IK}	Input clamp voltage at enable	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S* SN74S*	2.5 2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
I_I	Input current	Freq control or range $V_{CC} = \text{MAX}$	$V_I = 5 \text{ V}$ $V_I = 1 \text{ V}$		10 1	50 15	μA
I_I	Input current at maximum input voltage	Enable $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Enable $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				50	μA
I_{IL}	Low-level input current	Enable $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$				2	mA
I_{OS}	Short-circuit output current‡	$V_{CC} = \text{MAX}$		-40		-100	mA
I_{CC}	Supply current, total into V_{CC} and $\ominus V_{CC}$	$V_{CC} = \text{MAX}$, See Note 3 $V_{CC} = \text{MAX}, T_A = 125^\circ\text{C}$, See Note 3	W package only		105	150	mA
						110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the outputs disabled and open.

switching characteristics, $V_{CC} = 5 \text{ V}, R_L = 280 \Omega, C_L = 15 \text{ pF}, T_A = 25^\circ\text{C}$ (see note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_O	Output frequency	$C_X = 2 \text{ pF}$	$V_{I(freq)} = 4 \text{ V}, V_{I(rng)} = 1 \text{ V}$ $V_{I(freq)} = 1 \text{ V}, V_{I(rng)} = 5 \text{ V}$	60 25	85 40		MHz
	Output duty cycle	$C_X = 8.3 \text{ pF}$ to $500 \mu\text{F}$			50%		
t_{PHL}	Propagation delay time, high-to-low-level output from enable	$f_O = 1 \text{ Hz}$ to 20 MHz			1.4 $t_O(\text{Hz})$		s
		$f_O = 20 \text{ MHz}$			70		ns

NOTE 4: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

TYPICAL APPLICATION DATA

free-running oscillator

Free-running oscillators can be implemented for most systems by setting the output frequency of the VCO with either a capacitor or a crystal. If excitation is provided with a capacitor the frequency control and/or range inputs can be used to vary the output frequency.

When the 'S124 is excited with a crystal, low-frequency response (< 1 MHz) can be improved if a relatively small capacitor (5 to 15 pF) is paralleled with the crystal. When operated at the fundamental frequency of a crystal, the frequency control input should be high (≈ 5 V) and the range input should be low (grounded) for maximum stability over temperature and supply voltage variations.

phase-locked loops

A basic crystal-controlled phase-locked loop is illustrated in Figure 1. This application can be used for implementation of:

- A highly stable fixed-frequency clock generator.
- A highly stable fixed- or variable-frequency synthesizer.
- A highly efficient "slave-clock" system for synchronizing off-card, remote, or data-interfacing clock systems.

With fixed division rates for both M and N, the output frequency (f_o) will be stable at $f_o = \frac{N}{M} f_1$. Obviously, either M or N, or both, could be programmable counters in which case the output frequency (f_o) will be a variable frequency dependent on the instantaneous value of $\frac{N}{M} f_1$.

The crystal-controlled VCO can be operated up to 60 MHz with an accuracy that is dependent on the crystal. At the higher frequencies, response of the phase comparator can become a limiting factor and one of the following approaches may be necessary to extend the operating frequency range.

- Frequencies $\frac{f_1}{M}$ and $\frac{f_1}{N}$ can be divided equally by the same constant (K) also shown in Figure 1. The constant can be any value greater than unity ($K > 1$), and should be selected to yield frequency ranges that can be handled adequately by the phase-comparator and filter. The output frequency (f_o) retains the same relationship as previously explained because now:

$$f_o = \frac{KN}{KM} f_1 = \frac{N}{M} f_1$$

- In another method, the comparison of $\frac{f_1}{M}$ and $\frac{f_1}{N}$ can be performed with either an SN54LS85/SN74LS85 or SN54S85/SN74S85. The resultant $A > B$ and $A < B$ outputs from the 'LS85 or 'S85 permit the detector to be simplified to a charge-pump circuit. See Figure 2.

3

TTL DEVICES

TYPES SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

TYPICAL APPLICATION DATA

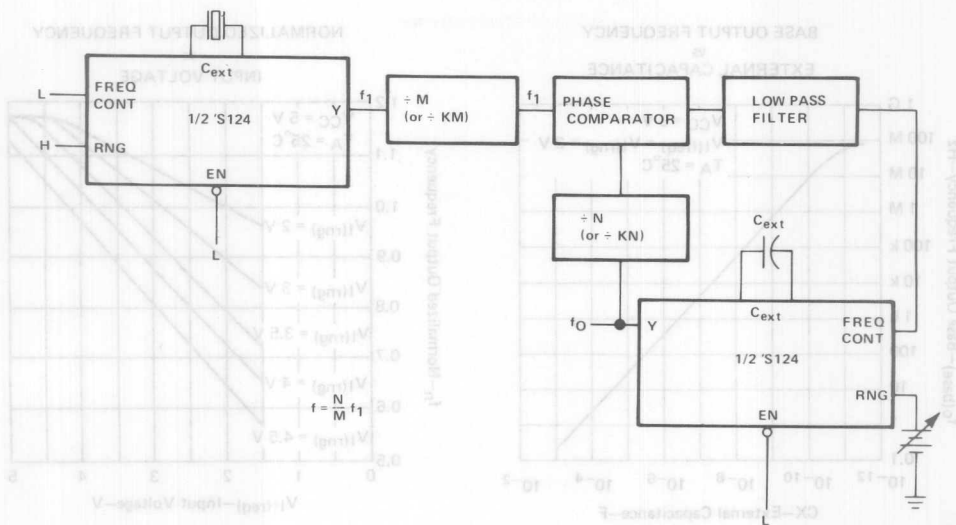


FIGURE 1—PHASE-LOCKED LOOP

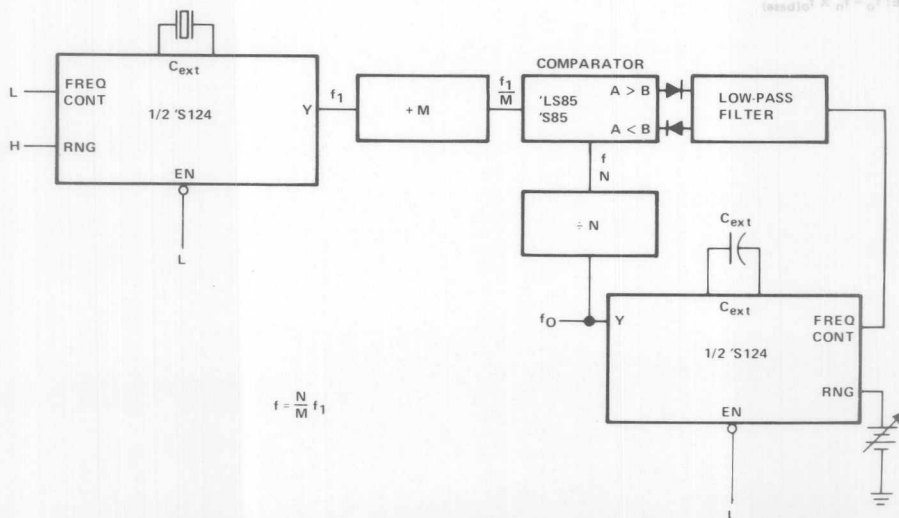


FIGURE 2—HIGH-FREQUENCY PHASE-LOCKED LOOP

TYPES SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

TYPICAL CHARACTERISTICS

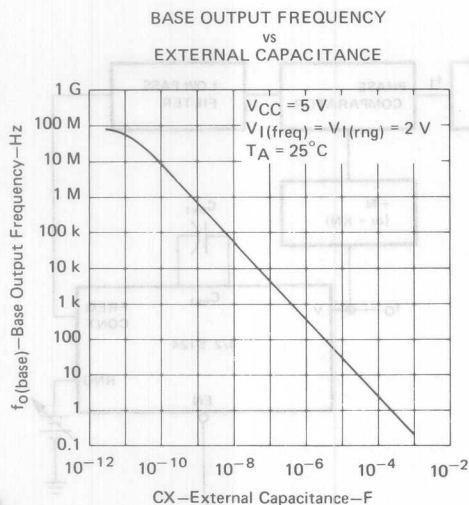


FIGURE 3

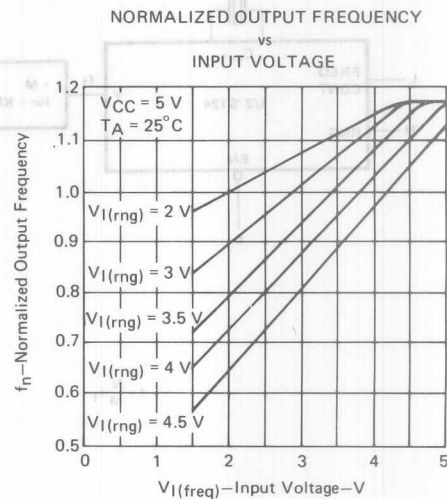


FIGURE 4

NOTE: $f_o = f_n \times f_o(\text{base})$

3

TTL DEVICES

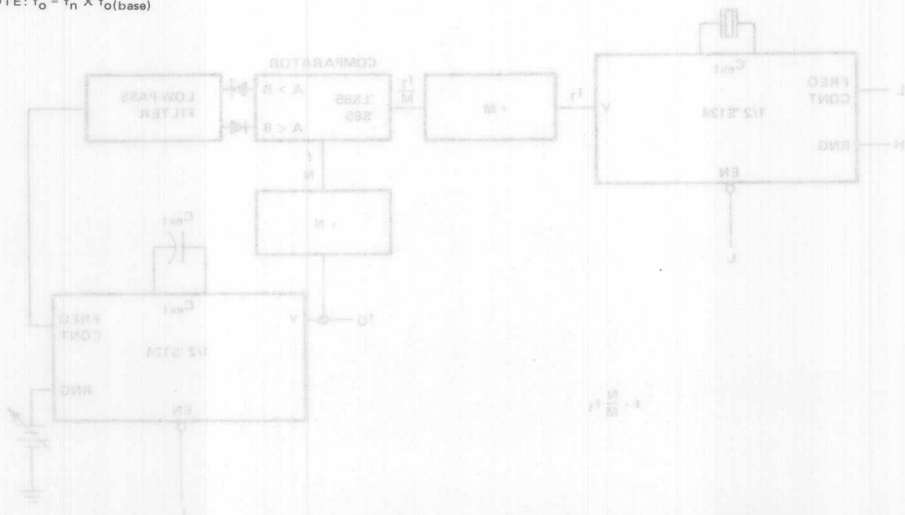


FIGURE 3—HIGH-FREQUENCY PHASE-LOCKED LOOP

TYPES SN54125, SN54126, SN54LS125A, SN54LS126A, SN74125, SN74126, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

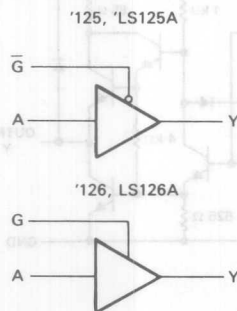
REVISED DECEMBER 1983

- Quad Bus Buffers
- 3-State Outputs
- Separate Control for Each Channel

description

These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pull-up resistors, when disabled, both output transistors are turned off presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The '125 and 'LS125A outputs are disabled when \bar{G} is high. The '126 and 'LS126A outputs are disabled when G is low.

logic diagram (each gate)



positive logic $Y = A$

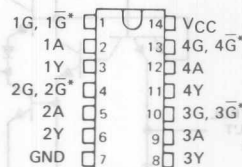
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '125, '126	5.5 V
'LS125A, 'LS126A	7 V
Operating free-air temperature range: SN54'	-55° C to 125° C
SN74'	0° C to 70° C
Storage temperature range	-65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

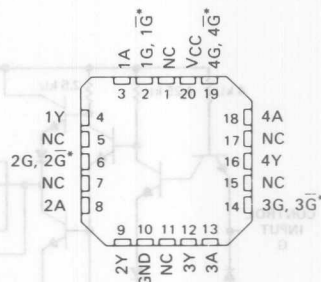
SN54125, SN54126, SN54LS125A,
SN54LS126A ... J OR W PACKAGE
SN74125, SN74126 ... J OR N PACKAGE
SN74LS125A, SN74LS126A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS125A, SN54LS126A ... FK PACKAGE
SN74LS125A, SN74LS126A

(TOP VIEW)



* \bar{G} on '125, 'LS125; G on 126, 'LS126

NC No internal connection

3

TTL DEVICES

PRODUCTION DATA

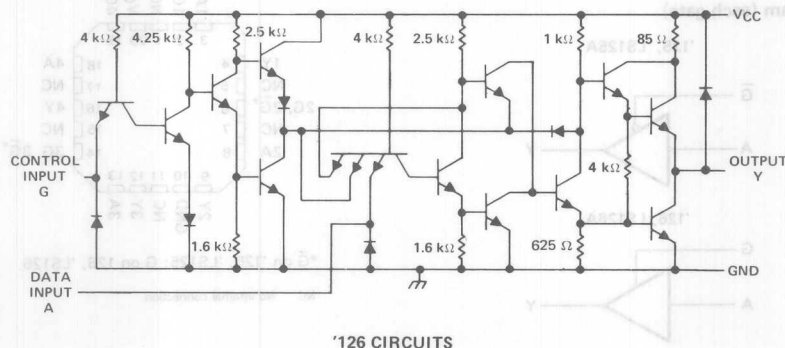
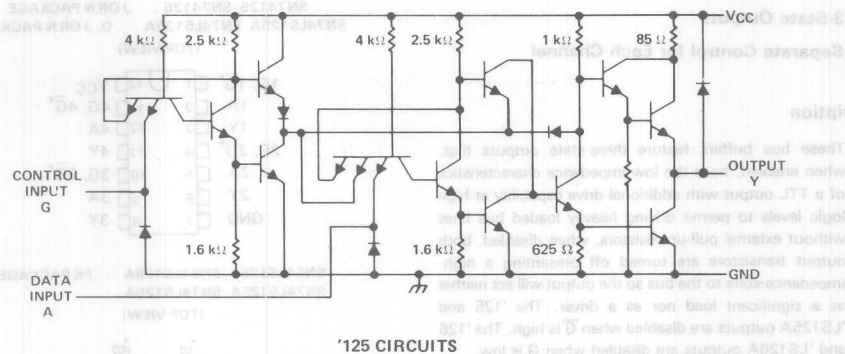
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-381

TYPES SN54125, SN54126, SN74125, SN74126 QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

schematics (each gate)



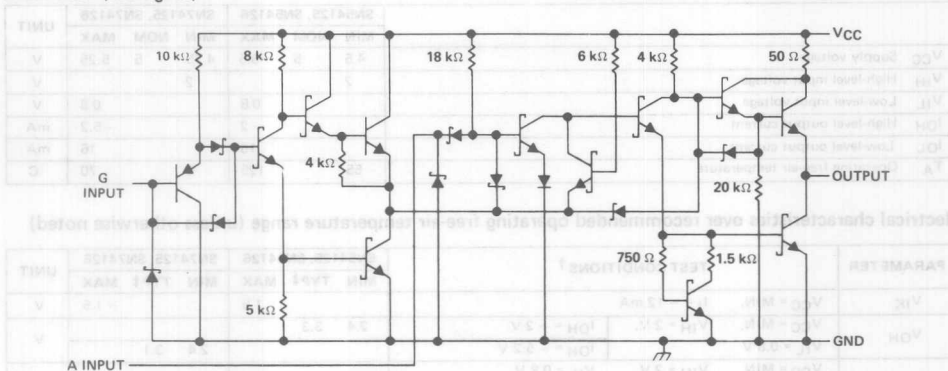
Resistor values shown are nominal.

3

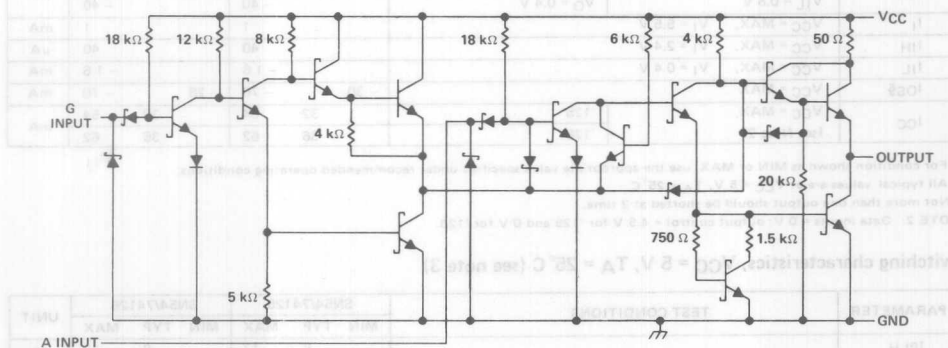
TTL DEVICES

TYPES SN54LS125A, SN54LS126A, SN74LS125A, SN74LS126A QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

schematics (each gate)



'LS125A CIRCUITS



'LS126A CIRCUITS

Resistor values shown are nominal.

3

TTL DEVICES

TYPES SN54125, SN54126, SN74125, SN74126 QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54125, SN54126			SN74125, SN74126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			− 2			− 5.2	mA
I _{OL}	Low-level output current			16			16	mA
T _A	Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54125, SN54126			SN74125, SN74126			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = − 12 mA				− 1.5			− 1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = − 2 V		2.4	3.3					V
	V _{IL} = 0.8 V, I _{OH} = − 5.2 V					2.4	3.1		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA				0.4			0.4	V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V				40			40	μA
	V _{IL} = 0.8 V, V _O = 0.4 V			− 40			− 40		
I _I	V _{CC} = MAX, V _I = 5.5 V				1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V				40			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V				− 1.6			− 1.6	mA
I _{OS§}	V _{CC} = MAX		− 30		− 70	− 28		− 70	mA
I _{CC}	V _{CC} = MAX, (see Note 2)	'125		32	54		32	54	mA
		'126		36	62		36	62	

† For condition shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at 2 time.

NOTE 2: Data inputs = 0 V; output control = 4.5 V for '125 and 0 V for '126.

switching characteristics, V_{CC} = 5 V, T_A = 25° C (see note 3)

PARAMETER	TEST CONDITIONS		SN54/74125			SN54/74126			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	R _L = 400 Ω, C _L = 50 pF		8	13		8	13		ns
t _{PHL}			12	18		12	18		ns
t _{PZH}			11	17		11	18		ns
t _{PZL}			16	25		16	25		ns
t _{PHZ}	R _L = 400 Ω, C _L = 5 pF		5	8		10	16		ns
			7	12		12	18		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

Ceramic Dips
Package Options Include Plastic and

		SN54LS125A SN54LS126A			SN74LS125A SN74LS126A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			− 1			− 2.6	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	− 55		125	0		70	°C

Model 15418 is designed to drive 20 mm lines.

PARAMETER	TEST CONDITIONS†		SN54LS125A SN54LS126A		SN74LS125A SN74LS126A		UNIT
			MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V _{IK}	V _{CC} = MIN, I _I = - 18 mA			- 1.5		- 1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V	V _{IL} = 0.7 V, I _{OH} = - 1 mA	2.4				V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V	V _{IL} = 0.8 V, I _{OH} = - 2.6 mA			2.4		
		V _{IL} = 0.7 V, I _{OL} = 12 mA	0.25	0.4			
		V _{IL} = 0.8 V, I _{OL} = 12 mA			0.25	0.4	V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V	V _{IL} = 0.7 V					
		V _O = 2.4 V		20			
		V _O = 0.4 V		- 20			
		V _{IL} = 0.8 V					
		V _O = 2.4 V				20	
		V _O = 0.4 V				- 20	μA
I _I	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20		20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	†LS125A-G inputs		- 0.2		- 0.2	mA
		†LS125A-A inputs; †LS126A-A1 inputs		- 0.4		0.4	mA
I _{OS} §	V _{CC} = MAX		- 40	- 225	40	225	mA
I _{CC}	V _{CC} = MAX, (see Note 2)	†LS125A		11		11	20
		†LS126A		12		12	22

recommended operating conditions.

recommended operating conditions.

circuit should not exceed one second.

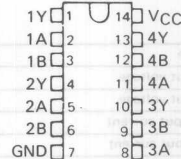
circuit should not exceed one second.

PARAMETER	TEST CONDITIONS		SN54/74LS125A			SN54/74LS126A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 667 \, \Omega$,	$C_L = 45 \, pF$	9	15		9	15	ns	
t_{PHL}			7	18		8	18	ns	
t_{PZH}			12	20		16	25	ns	
t_{PZL}			15	25		21	35	ns	
t_{PHZ}	$R_L = 667 \, \Omega$,	$C_L = 5 \, pF$	20			25		ns	
t_{PLZ}			20			25		ns	

- **Package Options Include Plastic and Ceramic DIPs**

- Dependable Texas Instruments Quality and Reliability

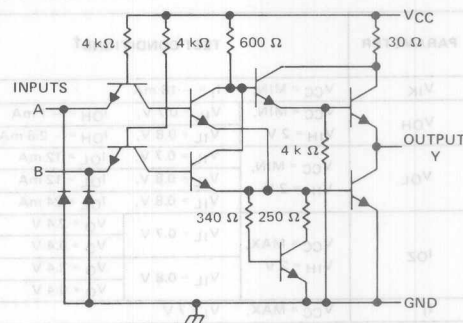
(TOP VIEW)



These devices contain four independent 2-input-NOR line drivers. They perform the Boolean function $Y = \overline{A+B}$. The SN54128 is designed to drive 75 ohm lines. The SN74128 is designed to drive 50 ohm lines.

The SN54128 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74128 is characterized for operation from 0°C to 70°C .

schematic (each driver)



Resistor values shown are nominal

logic diagram (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1).....	7 V
Input voltage.....	5.5 V
Operating free-air temperature range: SN54'.....	-55°C to 125°C
SN74'.....	0°C to 70°C
Storage temperature range.....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54128, SN74128
LINE DRIVERS

recommended operating conditions

		SN54128			SN74128			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-29			-42.4	mA
I _{OL}	Low-level output current			48			48	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -2.4 mA	2.4	3.4		V
	V _{CC} = MIN, V _{IL} = 0.4 V, I _{OH} = -13.2 mA	2.4			
	V _{CC} = MIN, V _{IL} = 0.4 V, I _{OH} = MAX	2			
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 48 mA		0.26	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6	mA
I _{OS} §	V _{CC} = MAX	-70		-180	mA
I _{CCH}	V _{CC} = MAX		12	21	mA
I _{CCL}	V _{CC} = MAX		33	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 133 Ω, C _L = 50 pF		6	9	ns
t _{PHL}					8	12	ns
t _{PLH}			R _L = 133 Ω, C _L = 150 pF		10	15	ns
t _{PHL}					12	18	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN74128		SN74129		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5	4.5	5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
I_{OH}	High-level output current	-25		-25		mA
I_{OL}	Low-level output current	-48		-48		mA
T_A	Operating free-air temperature	-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -15 \text{ mA}$			1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -2.4 \text{ mA}$		2.4	3.4	V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.4 \text{ V}$, $I_{OH} = -13.5 \text{ mA}$		2.4		V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.4 \text{ V}$, $I_{OH} = \text{MAX}$		2		V
	$V_{CC} = \text{MIN}$, $V_{IL} = 2 \text{ V}$, $I_{OH} = 48 \text{ mA}$		0.55	0.4	V
V_{OL}	$V_{CC} = \text{MAX}$, $V_I = 2.5 \text{ V}$			1	mA
I_I	$V_{CC} = \text{MAX}$, $V_I = 2.5 \text{ V}$			40	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.5 \text{ V}$			1.5	mA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			10	mA
I_{OZ}	$V_{CC} = \text{MAX}$		-10		mA
V_{CEH}	$V_{CC} = \text{MAX}$		15		mA
V_{CEL}	$V_{CC} = \text{MAX}$		25		mA

1 For switching times as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2 All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
3 Test waveforms are shown in Figure 1.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 100 \Omega$, $C_L = 50 \text{ pF}$	8	15	25	ns
t_{PHL}							
t_{PLH}			$R_L = 100 \Omega$, $C_L = 150 \text{ pF}$	10	25	40	ns
t_{PHL}							

NOTE 3: See General Information Section for load circuit and waveform definitions.

TYPES SN54132, SN54LS132, SN54S132, SN74132, SN74LS132, SN74S132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

REVISED DECEMBER 1983

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

description

Each circuit functions as a 2-input NAND gate, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clear, jitter-free output signals.

The SN54132, SN54LS132, and SN54S132 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74132, SN74LS132, and SN74S132 are characterized for operation from 0°C to 70°C .

logic diagram (each gate)

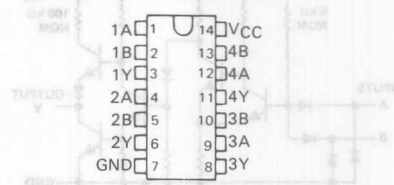


positive logic

$$Y = \overline{AB}$$

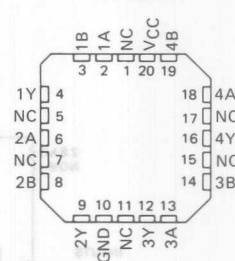
SN54132, SN54LS132, SN54S132 ... J OR W PACKAGE
SN74132 ... J OR N PACKAGE
SN74LS132, SN74S132 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS132, SN54S132 ... FK PACKAGE
SN74LS132, SN74S132

(TOP VIEW)



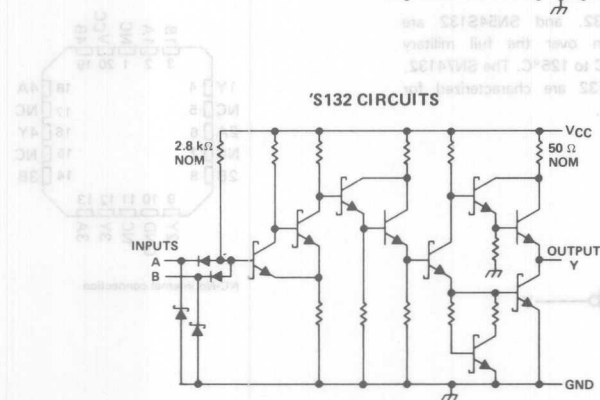
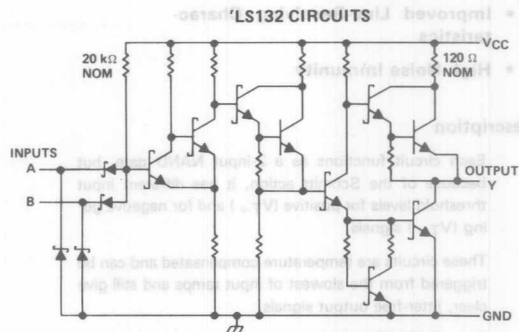
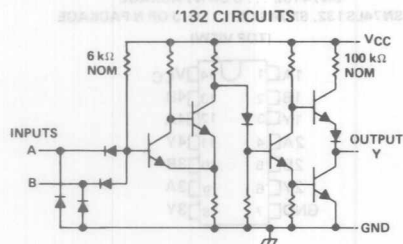
NC-No internal connection

3

TTL DEVICES

**TYPES SN54132, SN54LS132, SN54S132,
SN74132, SN74LS132, SN74S132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS**

schematics



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '132, 'S132	5.5 V
'LS132	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltages values are with respect to network ground terminal.

3

TTL DEVICES

SN54132, SN74132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54132			SN74132			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-0.8			-0.8	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{T+}	$V_{CC} = 5\text{ V}$	1.5	1.7	2	V
V_{T-}	$V_{CC} = 5\text{ V}$	0.6	0.9	1.1	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$	0.4	0.8		V
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12\text{ mA}$			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_I = 0.6\text{ V}$, $I_{OH} = -0.8\text{ mA}$	2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_I = 2\text{ V}$, $I_{OL} = 16\text{ mA}$		0.2	0.4	V
I_{T+}	$V_{CC} = 5\text{ V}$, $V_I = V_{T+}$		-0.43		mA
I_{T-}	$V_{CC} = 5\text{ V}$, $V_I = V_{T-}$		-0.56		mA
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5\text{ V}$			1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.4\text{ V}$			40	μA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$		-0.8	-1.2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$		-18	-55	mA
I_{CCH}	$V_{CC} = \text{MAX}$		15	24	mA
I_{CCL}	$V_{CC} = \text{MAX}$		26	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400\ \Omega$, $C_L = 15\text{ pF}$		15	22	ns
t_{PHL}					15	22	ns

3

TTL DEVICES

TYPES SN54LS132, SN74LS132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS132			SN74LS132			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS132			SN74LS132			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	$V_{CC} = 5\text{ V}$	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	$V_{CC} = 5\text{ V}$	0.5	0.8	1	0.5	0.8	1	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$	0.4	0.8		0.4	0.8		V
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_I = 0.5\text{ V}, I_{OH} = -0.4\text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_I = 1.9\text{ V}, I_{OL} = 4\text{ mA}$ $I_{OL} = 8\text{ mA}$	0.25	0.4		0.25	0.4		V
I_{T+}	$V_{CC} = 5\text{ V}, V_I = V_{T+}$	-0.14			-0.14			mA
I_{T-}	$V_{CC} = 5\text{ V}, V_I = V_{T-}$	-0.18			-0.18			mA
I_I	$V_{CC} = \text{MAX}, V_I = 7\text{ V}$		0.1			0.1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7\text{ V}$		20			20		µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{ V}$		-0.4			-0.4		mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CCH}	$V_{CC} = \text{MAX}$	5.9	11		5.9	11		mA
I_{CCL}	$V_{CC} = \text{MAX}$	8.2	14		8.2	14		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$	15	22		ns
t_{PHL}				15	22		ns

3

TTL DEVICES

TYPES SN54S132, SN74S132 QUADRUPL 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

recommended operating conditions

	SN54S132			SN74S132			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S132			SN74S132			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{T+}	V _{CC} = 5 V	1.6	1.77	1.9	1.6	1.77	1.9	V
V _{T-}	V _{CC} = 5 V	1.1	1.22	1.4	1.1	1.22	1.4	V
Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5 V	0.2	0.55		0.2	0.55		V
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _I = 1.1 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _I = 1.9 V, I _{OL} = 20 mA			0.5			0.5	V
I _{T+}	V _{CC} = 5 V, V _I = V _{T+}	-0.9			-0.9			mA
I _{T-}	V _{CC} = 5 V, V _I = V _{T-}	-1.1			-1.1			mA
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX		28	44		28	44	mA
I _{CCL}	V _{CC} = MAX		44	68		44	68	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

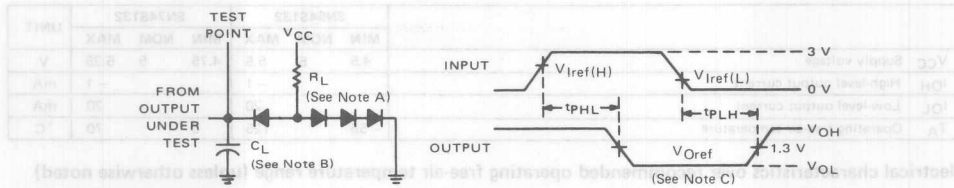
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 280 Ω, C _L = 15 pF		7	10.5	ns
t _{PHL}					8.5	13	ns

3

TTL DEVICES

SN74132, SN74LS132, SN74S132

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES:

- All diodes are 1N3064 or equivalent.
- C_L includes probe and jig capacitance.
- Generator characteristics and reference voltages are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I\text{ ref(H)}}$	$V_{I\text{ ref(L)}}$	$V_{O\text{ ref}}$
SN54/SN74'	50	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS/SN74LS'	50	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V
'S132	50	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V

FIGURE 1

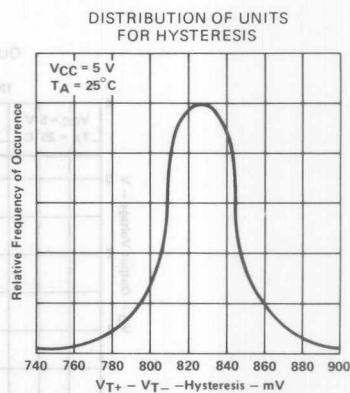
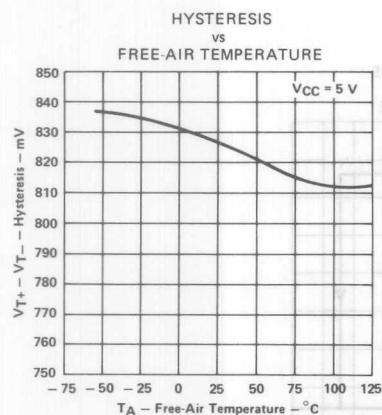
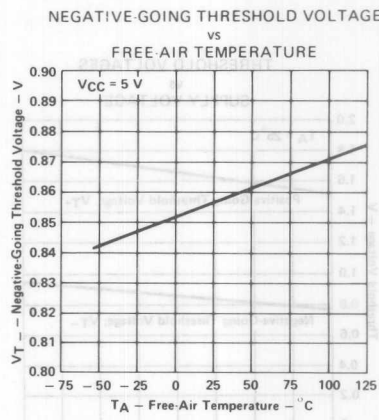
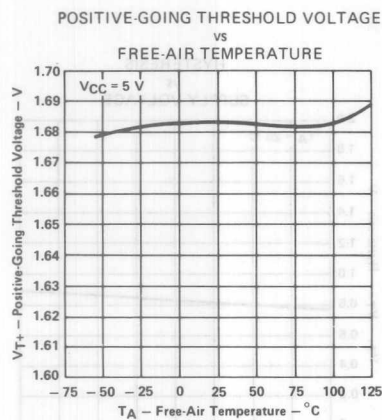
FIGURE 1

3

TTL DEVICES

TYPES SN54132, SN74132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

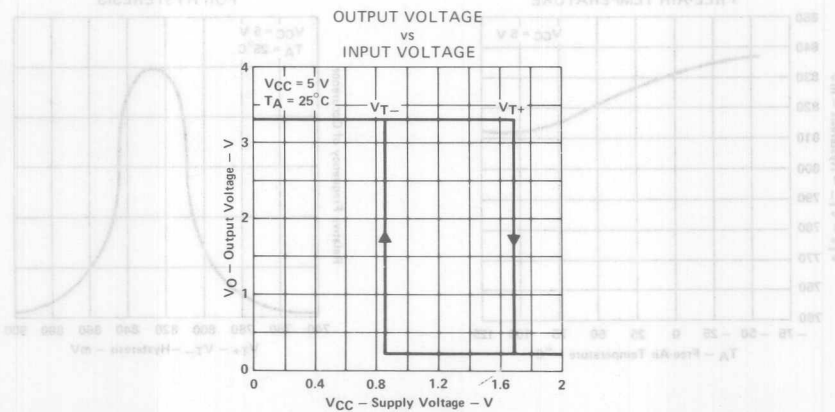
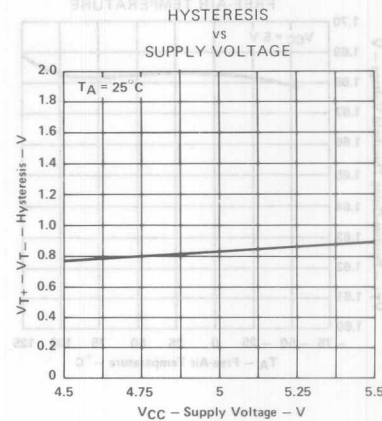
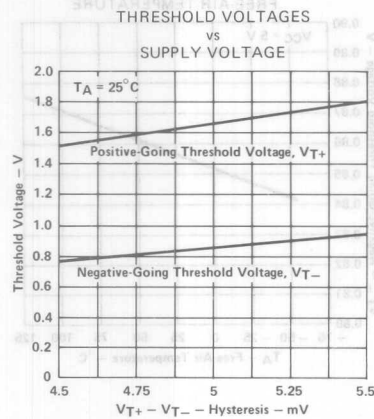
TYPICAL CHARACTERISTICS OF '132 CIRCUITS



† Data for temperatures below 0°C and 70°C and supply below 4.75 V and above 5.25 V are applicable for SN54132 only.

TYPES SN54132, SN74132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

TYPICAL CHARACTERISTICS OF '132 CIRCUITS



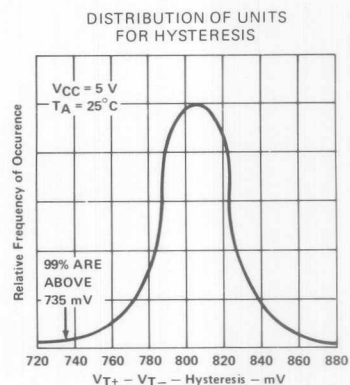
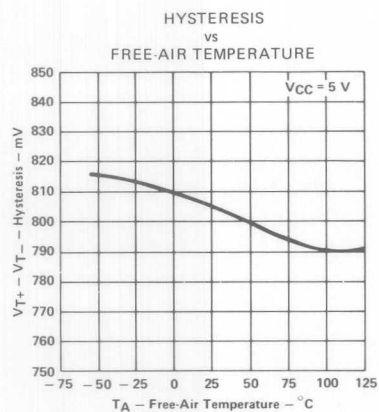
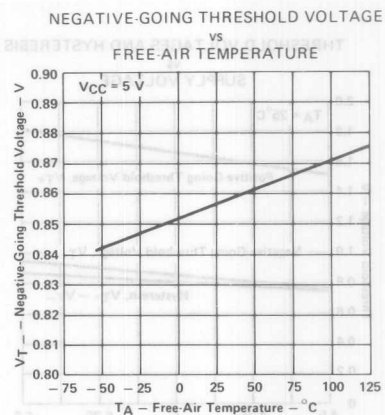
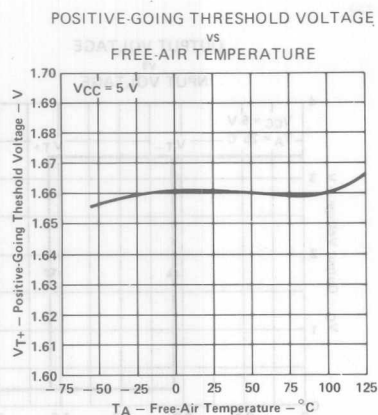
† Data for temperatures below 0°C and 70°C and supply below 4.75 V and above 5.25 V are applicable for SN54132 only.

3

TTL DEVICES

TYPES SN54LS132, SN74LS132 QUADRUPL 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

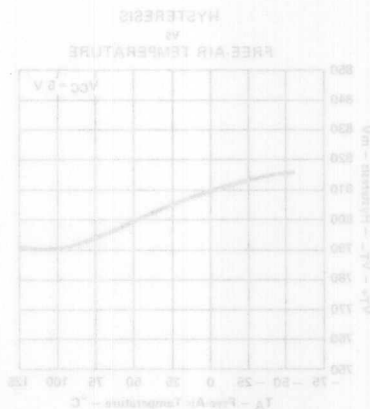
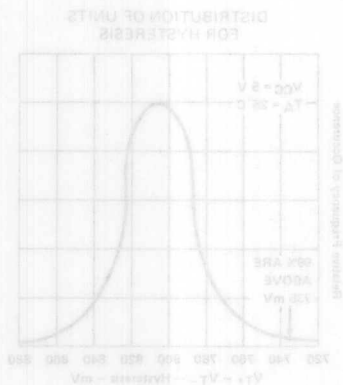
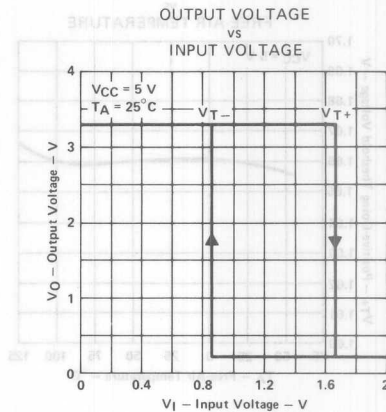
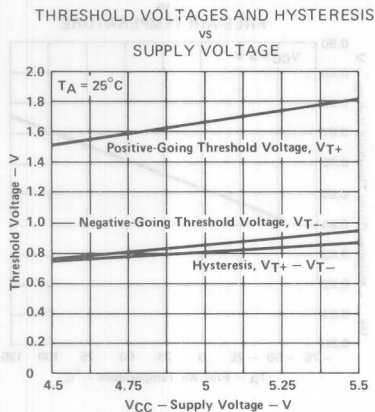
TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS



[†] Data for temperatures below 0 $^{\circ}\text{C}$ and above 70 $^{\circ}\text{C}$ and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS132 only.

TYPES SN54LS132, SN74LS132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

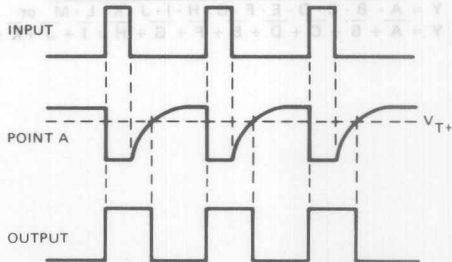
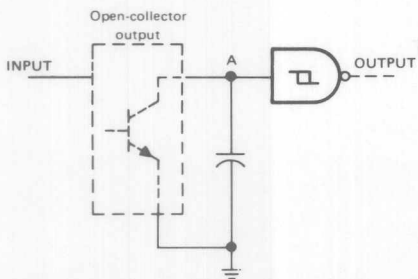
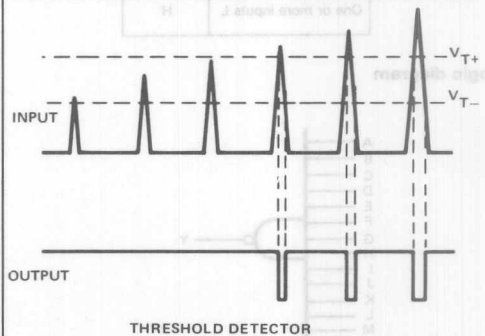
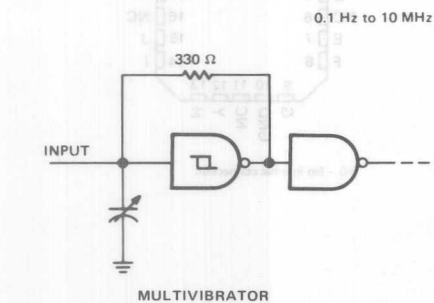
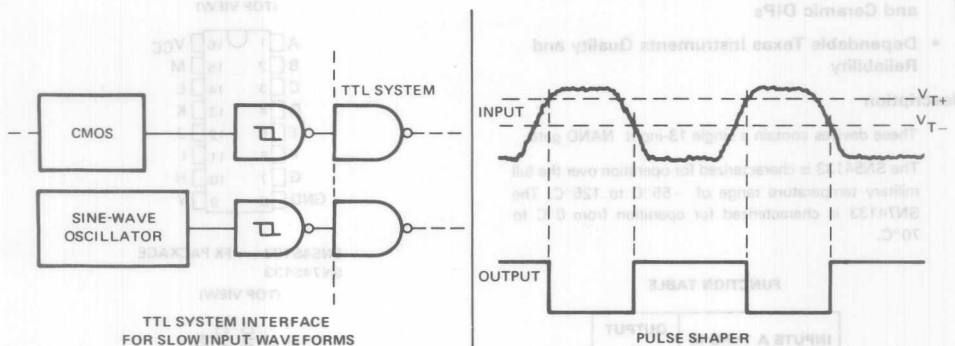
TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS



† Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS132 only.

TYPES SN54132, SN54LS132, SN54S132,
SN74132, SN74LS132, SN74S132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

TYPICAL APPLICATION DATA



3
TTL DEVICES

TYPES SN54S133, SN74S133 13-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

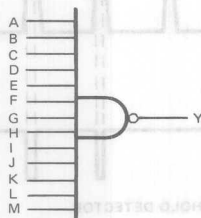
These devices contain a single 13-input NAND gate.

The SN54S133 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74S133 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

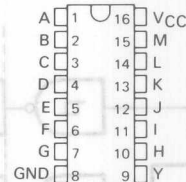
logic diagram



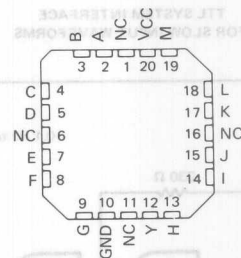
positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M} \text{ or } Y = \overline{A + B + C + D + E + F + G + H + I + J + K + L + M}$$

SN54S133 ... J OR W PACKAGE
SN74S133 ... D, J OR N PACKAGE
(TOP VIEW)



SN54S133 ... FK PACKAGE
SN74S133
(TOP VIEW)



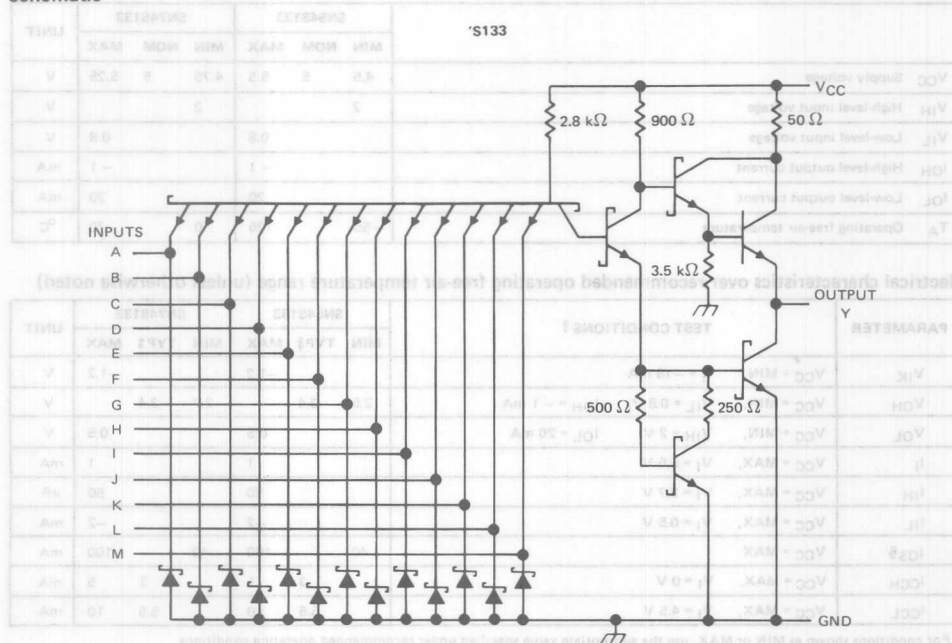
NC - No internal connection

3

TTL DEVICES

TYPES SN54S133, SN74S133 13-INPUT POSITIVE-NAND GATES

schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54S133, SN74S133 13-INPUT POSITIVE-NAND GATES

recommended operating conditions

	SN54S133			SN74S133			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S133			SN74S133			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50			50	μA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		3	5		3	5	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		5.5	10		5.5	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 280 Ω, C _L = 15 pF		4	6	ns
t _{PHL}					4.5	7	ns
t _{PLH}			R _L = 280 Ω, C _L = 50 pF		5.5		ns
t _{PHL}					6.5		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S134, SN74S134 12-INPUT POSITIVE-NAND GATES WITH 3-STATE OUTPUTS

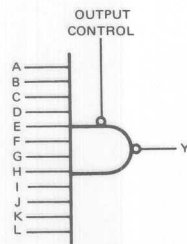
REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'S134 feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded lines without external pull-up resistors. When disabled, both output transistors are turned off presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The 'S134 outputs are disabled when G is high.

logic diagram

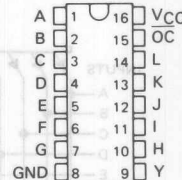


positive logic

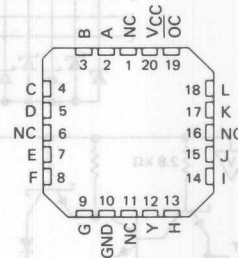
$$Y = \overline{ABCDEFGHIJKL}$$

Output is off (disabled) when output control is high.

SN54S134 ... J OR W PACKAGE
SN74S134 ... D, J OR N PACKAGE
(TOP VIEW)



SN54S134 ... FK PACKAGE
SN74S134
(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

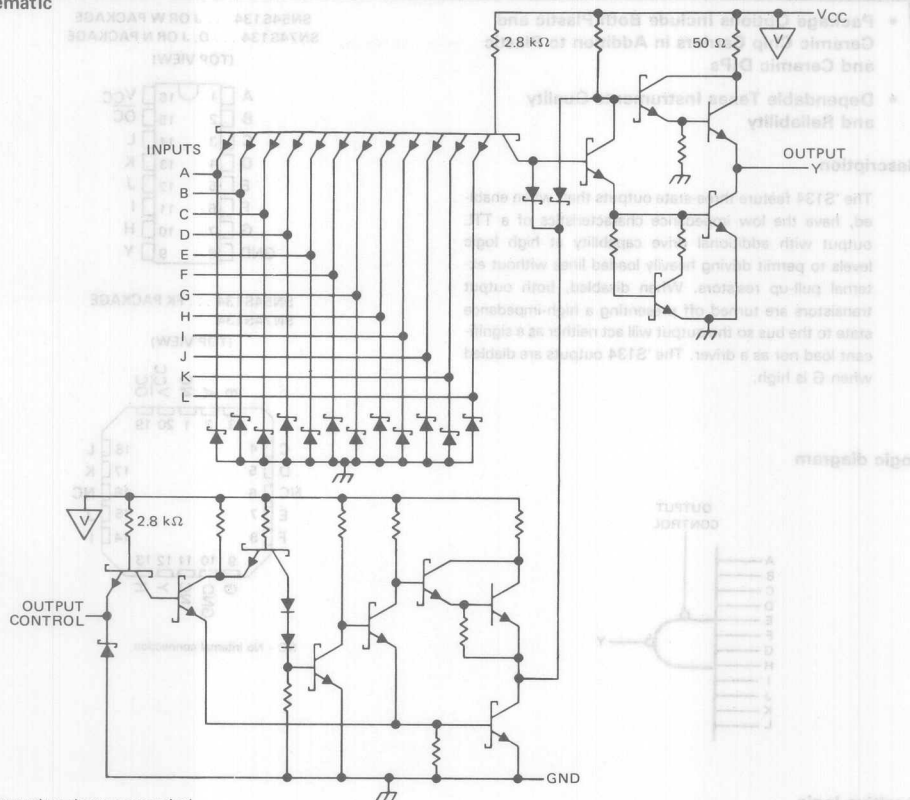
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54S134, SN74S134 12-INPUT POSITIVE-NAND GATES WITH 3-STATE OUTPUTS

schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

recommended operating conditions

		SN54S134			SN74S134			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-2			-6.5	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S134			SN74S134			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V	I _{OH} = -2 mA	2.4	3.4					V
	V _{IL} = 0.8 V	I _{OH} = -6.5 mA				2.4	3.2		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA	V _{IL} = 0.8 V			0.5			0.5	V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = 0.8 V	V _O = 2.4 V			50			50	μA
		V _O = 0.5 V			-50			-50	
I _I	V _{CC} = MAX, V _I = 5.5 V				1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				50			50	μA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V				-2			-2	mA
I _{OS} §	V _{CC} = MAX		-40	-100	-40	-100			mA
I _{CC}	V _{CC} = MAX	Outputs high		7	13		7	13	mA
		Outputs low		9	16		9	16	
		Outputs disabled		14	25		14	25	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

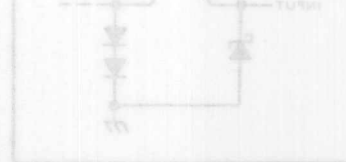
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	TEST CONDITIONS		SN54S134			SN74S134			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	R _L = 280 Ω, C _L = 15 pF		4		6	4		6	ns
t _{PLH}	R _L = 280 Ω, C _L = 50 pF		5.5			5.5			ns
t _{PHL}	R _L = 280 Ω, C _L = 15 pF		5		7.5	5		7.5	ns
t _{PHL}	R _L = 280 Ω, C _L = 50 pF		7			7			ns
t _{PZH}	R _L = 280 Ω, C _L = 50 pF		13		19.5	13		19.5	ns
t _{PZL}			14		21	14		21	ns
t _{PHZ}	R _L = 280 Ω, C _L = 5 pF		5.5		8.5	5.5		8.5	ns
t _{PLZ}			9		14	9		14	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.



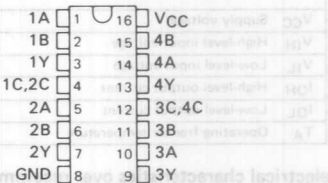
TYPES SN54S135, SN74S135 QUADRUPLE EXCLUSIVE-OR/NOR GATES

DECEMBER 1972—REVISED DECEMBER 1983

- Fully Compatible with Most TTL and TTL MSI Circuits
- Fully Schottky Clamping Reduces Delay Times . . . 8 ns Typical
- Can Operate as Exclusive-OR Gate (C Input Low) or as Exclusive-NOR Gate (C Input High)

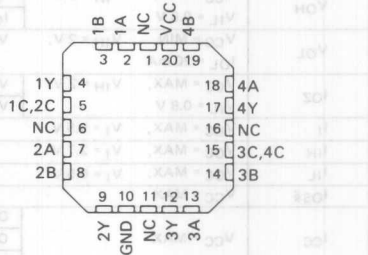
SN54S135 . . . J OR W PACKAGE
SN74S135 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54S135 . . . FK PACKAGE
SN74S135

(TOP VIEW)



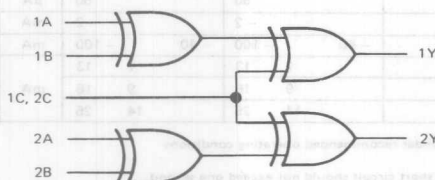
NC - No internal connection

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = high level, L = low level

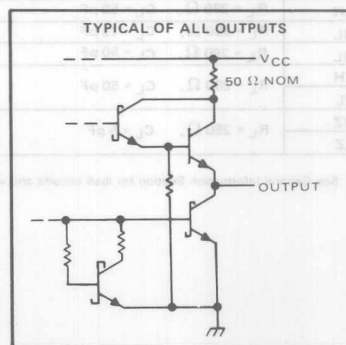
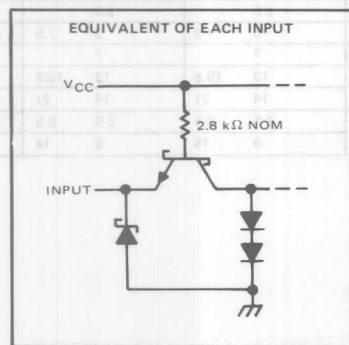
logic diagram (one half)



positive logic

$$Y = A \oplus B \oplus C = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

schematics of inputs and outputs



Resistor values shown are nominal.

3

TTL DEVICES

TYPES SN54S135, SN74S135 QUADRUPLE EXCLUSIVE-OR/NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S135	-55°C to 125°C
SN74S135	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S135			SN74S135			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S [*]	2.5	3.4	V
		SN74S [*]	2.7	3.4	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2		65	99	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER†	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A or B	B or A = L, C = L	C _L = 15 pF, R _L = 280 Ω, See Note 3	8.5	13	ns	
t _{PHL}				11	15		
t _{PLH}	A or B	B or A = H, C = L		8	12	ns	
t _{PHL}				9	13.5		
t _{PLH}	A or B	B or A = L, C = H		10	15	ns	
t _{PHL}				6.5	10		
t _{PLH}	A or B	B or A = H, C = H		8.5	12	ns	
t _{PHL}				7	13		
t _{PLH}	C	A = B		8	12	ns	
t _{PHL}				9.5	14.5		
t _{PLH}	C	A ≠ B		7.5	11.5	ns	
t _{PHL}				8	12		

[¶] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

QUADUPLE EXCLUSIVE-OR/INCR GATES TYPED SN54S133, SN74S133

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	
supply voltage, V_{CC} (see Note 1)	5.5 V
input voltage	5.5 V
operating free-air temperature range: SN54S133	-55°C to 125°C
SN74S133	-55°C to 70°C
storage temperature range	-55°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54S133	SN74S133
supply voltage, V_{CC}	4.5 to 5.5	4.5 to 5.5
high-level output current, I_{OH}	-1 mA	-1 mA
low-level output current, I_{OL}	20 mA	20 mA
operating free-air temperature, T_A	-55 to 125	-55 to 70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		3		V
V_{IL}	Low-level input voltage		0.8		V
V_{IK}	Input clamp voltage		-1.5		V
V_{OH}	High-level output voltage	$V_{CC} - \text{MIN.}, I_L = -18 \text{ mA}$ $V_{CC} = \text{MIN.}, V_{IH} = 3 \text{ V}, I_{OH} = -1 \text{ mA}$	5.0	5.4	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN.}, V_{IH} = 3 \text{ V}, I_{OL} = 20 \text{ mA}$ $V_{CC} = \text{MIN.}, V_{IH} = 3 \text{ V}, I_{OL} = 20 \text{ mA}$	0.5	0.8	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX.}, V_I = 5 \text{ V}$		1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX.}, V_I = 3 \text{ V}$		50	µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX.}, V_I = 0.5 \text{ V}$		-5	mA
I_{OZ}	Short-circuit output current	$V_{CC} = \text{MAX.}$	-40	-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX.}$ (see Note 2)	60	80	mA

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 Test values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
 Input more than one output should be loaded at a time and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A = L, C = L		9.5	13	ns
t_{PHL}	A or B	B or A = H, C = L		8	13	ns
t_{PLH}	A or B	B or A = L, C = H		8.5	13	ns
t_{PHL}	A or B	B or A = H, C = H		8.5	13	ns
t_{PLH}	C	A = B		8.5	13	ns
t_{PHL}	C	A = B		8.5	13	ns

t_{PLH} propagation delay time, low-to-high level output
 t_{PHL} propagation delay time, high-to-low level output
 NOTE 2: See General Information Section for test circuit and voltage waveform.

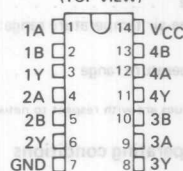
3 TTL DEVICES

DECEMBER 1972—REVISED DECEMBER 1983

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

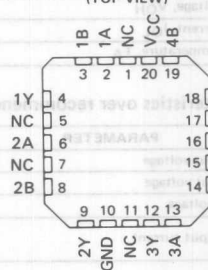
SN54136, SN54LS136 . . . J OR W PACKAGE
SN74136 . . . J OR N PACKAGE
SN74LS136 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS136 . . . FK PACKAGE
SN74LS136

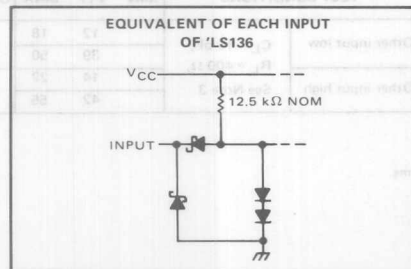
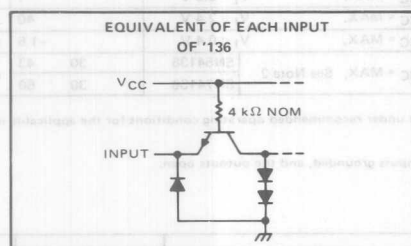
(TOP VIEW)



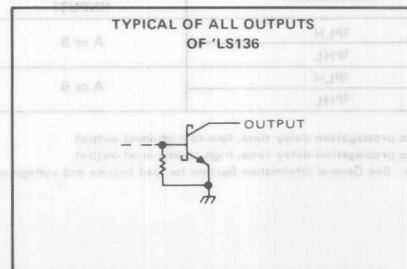
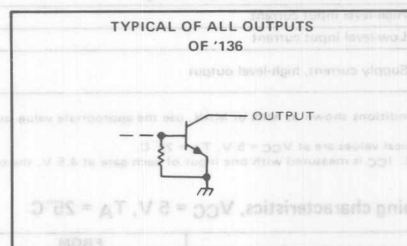
positive logic

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

schematics of inputs and outputs



Resistor values shown are nominal.



3

TTL DEVICES

TYPES SN54136, SN74136
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES
WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54136	-55°C to 125°C
SN74136	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54136			SN74136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -8 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 5.5 \text{ V}$			250	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current, high-level output	$V_{CC} = \text{MAX}$, See Note 2	SN54136	30	43	mA
		SN74136	30	50	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER [†]	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Other input low	C _L = 15 pF, R _L = 400 Ω	12	18	ns	
t _{PHL}				39	50		
t _{PLH}	A or B	Other input high	See Note 3	14	22	ns	
t _{PHL}				42	55		

‡ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS136, SN74LS136 **QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES** **WITH OPEN-COLLECTOR OUTPUTS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS136	-55°C to 125°C
SN74LS136	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS136			SN74LS136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS136			SN74LS136			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.2			0.2		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		40			40		µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8			-0.8		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.1	10		6.1	10		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	A or B	Other input low	CL = 15 pF, RL = 2 kΩ, (See Note 3)		18	30	ns
tPHL					18	30	
tPLH	A or B	Other input high			18	30	ns
tPHL					18	30	

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS138, SN74LS138 QUADUPLE 3-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS138	-55°C to 125°C
SN74LS138	0°C to 70°C
Storage temperature range	-65°C to 180°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS138		SN74LS138		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	5	4.5	5	V
High-level output voltage, V_{OH}	2.5		2.5		V
Low-level output current, I_{OL}	4		4		mA
Operating free-air temperature, T_A	-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LS138		SN74LS138		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH} High-level input voltage			2		2		V
V_{IL} Low-level input voltage			0.3		0.3		V
V_{IC} Input clamp voltage			-1.8		-1.8		V
I_{OH} High-level output current			100		100		µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL}(\text{max.})$ $V_{OH} = 2.5 \text{ V.}$		0.32	0.4	0.25	0.4	V
	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL}(\text{max.})$ $I_{OL} = 8 \text{ mA.}$		0.32	0.4	0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX.}$ $V_I = 3 \text{ V.}$		0.3		0.3		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX.}$ $V_I = 3 \text{ V.}$		40		40		µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX.}$ $V_I = 0.4 \text{ V.}$		-0.5		-0.5		mA
I_{CC} Supply current	$V_{CC} = \text{MAX.}$ See Note 2		6.1	10	5	10	mA

For conditions within MIN or MAX, use the appropriate value specified under recommended operating conditions for the condition type.
TA typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
NOTE 2: I_{CC} is measured with one input to each gate at 0 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM INPUT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		Other input low	Other input high (see Note 3)				
t_{PLH}	A or B	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$		18	30		ns
t_{PHL}	A or B			18	30		ns

t_{PLH} = propagation delay time, low to high-level output
 t_{PHL} = propagation delay time, high to low-level output
NOTE 3: See General Information Section for test circuit and voltage waveform.

3 TTL DEVICES

TYPES SN54LS137, SN74LS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLXERS WITH ADDRESS LATCHES

D2416, JUNE 1978—REVISED DECEMBER 1983

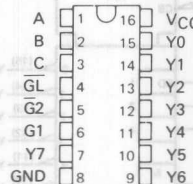
- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Enable Inputs to Simplify Cascading
- Low Power Dissipation . . . 65 mW Typ

description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input (\overline{GL}) is low, the 'LS137 acts as a decoder/demultiplexer. When \overline{GL} goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as \overline{GL} remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

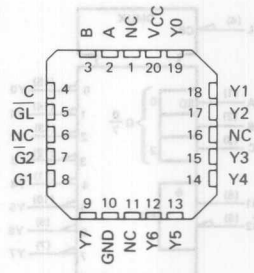
SN54LS137 . . . J OR W PACKAGE
SN74LS137 . . . D, J OR N PACKAGE

(TOP VIEW)



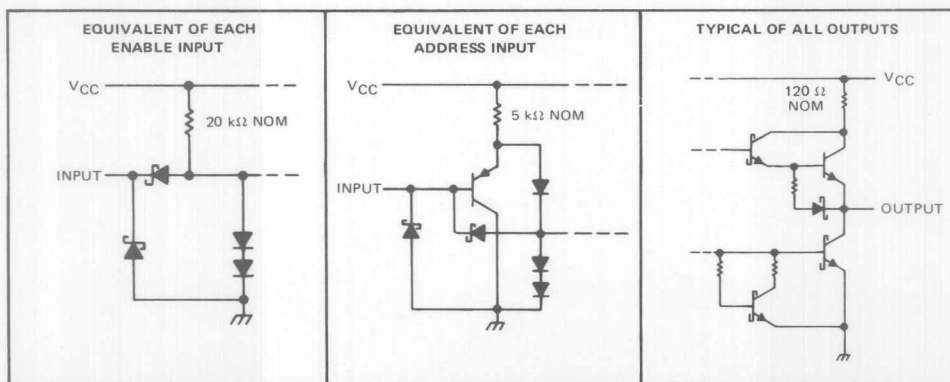
SN54LS137 . . . FK PACKAGE
SN74LS137

(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

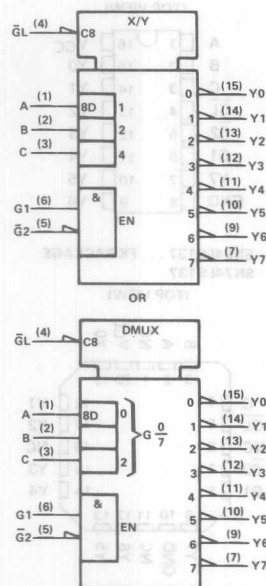
3-413

3

TTL DEVICES

TYPES SN54LS137, SN74LS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

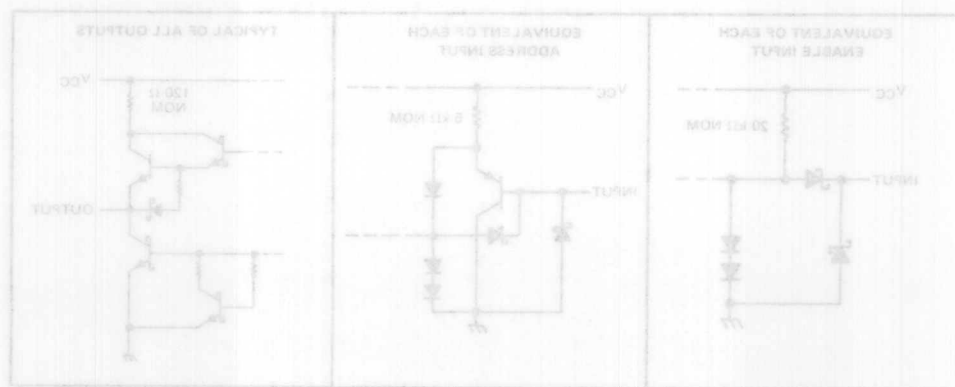
FUNCTION TABLE

INPUTS					OUTPUTS								
ENABLE			SELECT										
GL	G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	L	H	H	L	H	H	H	H
L	H	L	H	L	H	L	H	H	H	L	H	H	H
L	H	L	H	H	L	L	H	H	H	L	H	H	H
L	H	L	H	H	H	L	H	H	H	L	H	H	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant. The L2137 is a 3-state device. High and low levels are indicated by the L2137. The L2137 is a 3-state device. High and low levels are indicated by the L2137. The L2137 is a 3-state device. High and low levels are indicated by the L2137.

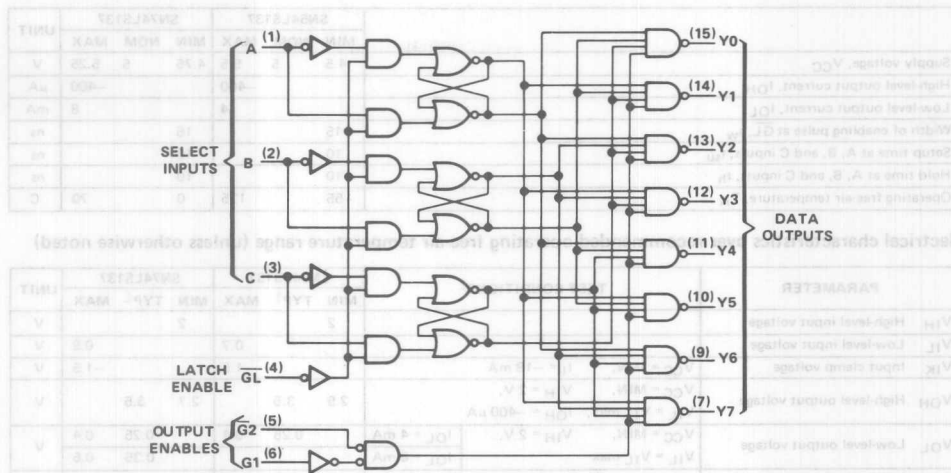
3

TTL DEVICES



TYPES SN54LS137, SN74LS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

logic diagram (positive logic)



Pin numbers shown on logic notation are for D, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS137	-55°C to 125°C
SN74LS137	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C	Y	3	$C_L = 50 \text{ pF}$	11	13	15	ns
t_{PHL}	A, B, C	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns
t_{PLH}	Enable G1	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns
t_{PHL}	Enable G1	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns
t_{PLH}	Enable G2	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns
t_{PHL}	Enable G2	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns
t_{PLH}	Enable GL	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns
t_{PHL}	Enable GL	Y	3	$C_L = 50 \text{ pF}$	10	12	14	ns

TYPES SN54LS137, SN74LS137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

WITH ADDRESS LATCHES

recommended operating conditions

	SN54LS137			SN74LS137			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse at GL, t_W	15			15			ns
Setup time at A, B, and C inputs, t_{SU}	10			10			ns
Hold time at A, B, and C inputs, t_H	10			10			ns
Operating free-air temperature, T_A	-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS137			SN74LS137			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage					0.7			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = −18 mA				−1.5			V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = −400 μA	2.5	3.5		2.7	3.5		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA		0.25	0.4	0.25		V
		I _{OL} = 8 mA				0.35		
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1			mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V				20			μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V	Enable		−0.4		−0.4		mA
		A, B, C		−0.2		−0.2		
I _{OS} Short-circuit output current§	V _{CC} = MAX	−20			−100			mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2				11		18	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$, see note 3

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C	Y	2	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 3	11	17	ns	
t_{PHL}			4		25	38		
t_{PLH}	A, B, C	Y	3		16	24	ns	
t_{PHL}			3		19	29		
t_{PLH}	Enable $\overline{G}2$	Y	2		13	21	ns	
t_{PHL}			2		16	27		
t_{PLH}	Enable G1	Y	3		14	21	ns	
t_{PHL}			3		18	27		
t_{PLH}	Enable $\overline{G}L$	Y	3		18	27	ns	
t_{PHL}			4		25	38		

t_{PLH} = propagation delay time, low to high-level output.

t_{PHL} = propagation delay time, high to low-level output.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS138, SN54S138A, SN74LS138, SN74S138A

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1972 — REVISED APRIL 1985

- Designed Specifically for High-Speed: Memory Decoders Data Transmission Systems
- 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Schottky-Clamped for High Performance

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

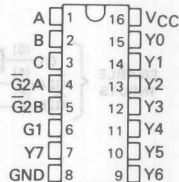
The 'LS138 and 'S138A decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS138 and SN74S138A are characterized for operation from 0°C to 70°C.

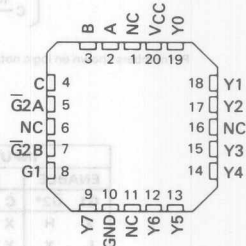
SN54LS138, SN54S138A ... J OR W PACKAGE
SN74LS138, SN74S138A ... D, J OR N PACKAGE

(TOP VIEW)



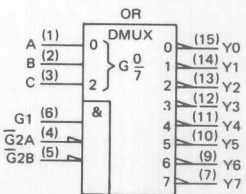
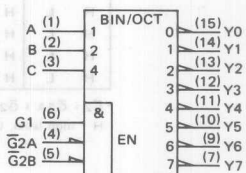
SN54LS138, SN54S138A ... FK PACKAGE
SN74LS138, SN74S138A

(TOP VIEW)



NC - No internal connection

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

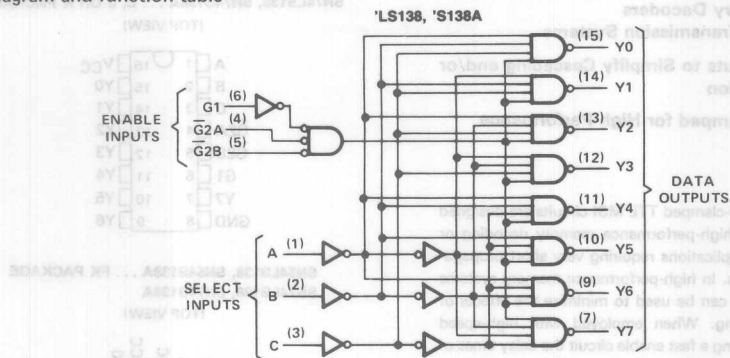
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54LS138, SN54S138A, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

logic diagram and function table



'LS138, 'S138A
FUNCTION TABLE

INPUTS				OUTPUTS								
ENABLE		SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1	G2*	C	B	A								
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	L	H	H	H	H
H	L	H	H	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	H	H	L	H	H

*G2 = G2A + G2B

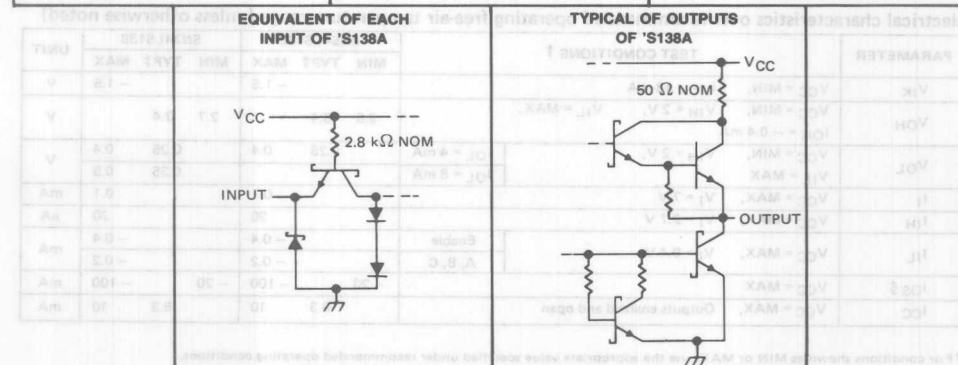
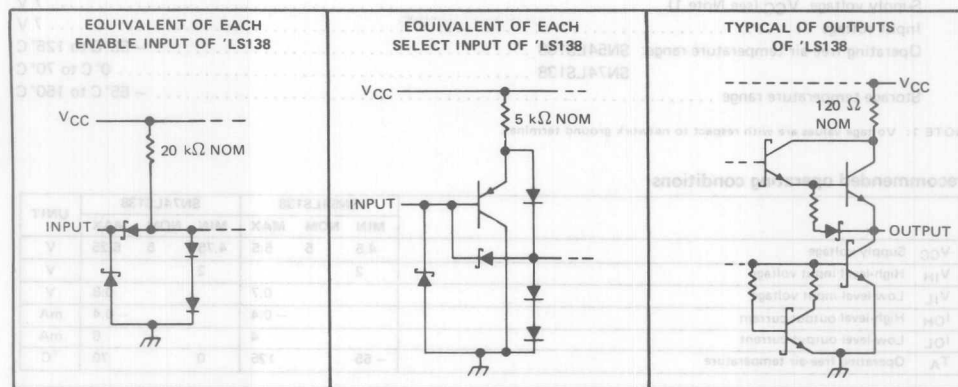
H = high level, L = low level, X = irrelevant

3

TTL DEVICES

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

schematics of inputs and outputs



TYPES SN54LS138, SN74LS138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS138	— 55° C to 125° C
SN74LS138	0° C to 70° C
Storage temperature range	— 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS138			SN74LS138			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			— 0.4			— 0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	— 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †		SN54LS138			SN74LS138			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				— 1.5			— 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$		2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	Enable			— 0.4			— 0.4	mA
		A, B, C			— 0.2			— 0.2	
$I_{OS} §$	$V_{CC} = \text{MAX}$		— 20		— 100	— 20		— 100	mA
I_{CC}	$V_{CC} = \text{MAX},$ Outputs enabled and open			6.3	10		6.3	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS138 SN74LS138			UNIT
					MIN	TYP	MAX	
tPLH	Binary Select	Any	2	RL = 2 kΩ, CL = 15 pF, See Note 2	11	20	ns	
tPHL					18	41	ns	
tPLH			3		21	27	ns	
tPHL					20	39	ns	
tPLH	Enable	Any	2		12	18	ns	
tPHL					20	32	ns	
tPLH			3		14	26	ns	
tPHL					13	38	ns	

† t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S138A, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLXERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S138A	–55°C to 125°C
SN74S138A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S138A			SN74S138A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–1			–1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†				SN54S138A SN74S138A		UNIT
					MIN	MAX	
V_{IK}	$V_{CC} = \text{MIN.}$	$I_I = 18 \text{ mA}$			–1.2		V
V_{OH}	$V_{CC} = \text{MIN.}$	$V_{IH} = 2 \text{ V.}$	$V_{IL} = 0.8 \text{ V.}$	$I_{OH} = -1 \text{ mA}$	SN54S* 2.5 SN74S* 2.7	3.4 3.4	V
V_{OL}	$V_{CC} = \text{MIN.}$	$V_{IH} = 2 \text{ V.}$	$V_{IL} = 0.8 \text{ V.}$	$I_{OL} = 20 \text{ mA}$		0.5	V
I_I	$V_{CC} = \text{MAX.}$	$V_I = 5.5 \text{ V}$				1	mA
I_{IH}	$V_{CC} = \text{MAX.}$	$V_I = 2.7 \text{ V}$				50	μA
I_{IL}	$V_{CC} = \text{MAX.}$	$V_I = 0.5 \text{ V}$				–2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$				–40	–100	mA
I_{CC}	$V_{CC} = \text{MAX.}$	Outputs enabled and open			SN54S* 49 SN74S* 49	74 74	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

*All typical values are at $V_{CC} = 5 \text{ V. } T_A = 25^\circ\text{C.}$

§Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V, } T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S138A SN74S138A			UNIT	
					MIN	TYP	MAX		
tPLH	Binary Select	Any	2	RL = 280 Ω, CL = 15 pF, See Note 2		4.5	7	ns	
tPHL						7	10.5		
tPLH			3			7.5	12	ns	
tPHL						8	12		
tPLH	Enable	Any	2			5	8	ns	
tPHL						7	11		
tPLH			3			7	11	ns	
tPHL						7	11		

† t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

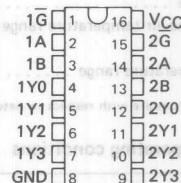
NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS139A, SN54S139A, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULPLEXERS

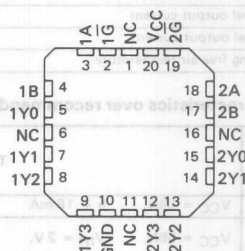
REVISED APRIL 1985

- Designed Specifically for High-Speed: Memory Decoders Data Transmission Systems
- Two Fully Independent 2-to-4-Line Decoders/Demultiplexers
- Schottky Clamped for High Performance

SN54LS139A, SN54S139A ... J OR W PACKAGE
SN74LS139A, SN74S139A ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS139A, SN54S139A ... FK PACKAGE
SN74LS139A, SN74S139A
(TOP VIEW)



NC - No internal connection

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and the SN54S139A are characterized for operation range of -55°C to 125°C . The SN74LS139A and the SN74S139A are characterized for operation from 0°C to 70°C .

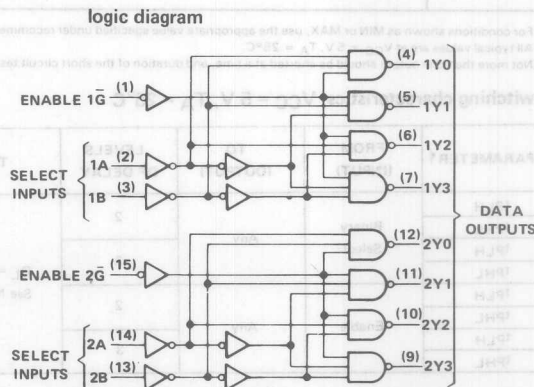
3

TTL DEVICES

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT		Y0	Y1	Y2	Y3
\bar{G}	B A					
H	X X		H	H	H	H
L	L L		L	H	H	H
L	L H		H	L	H	H
L	H L		H	H	L	H
L	H H		H	H	H	L

H = high level, L = low level, X = irrelevant



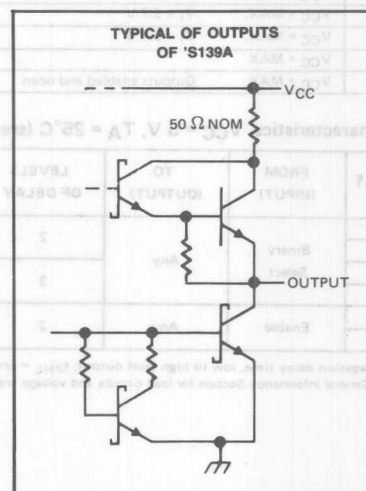
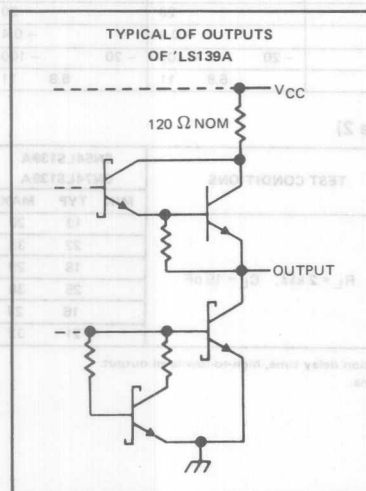
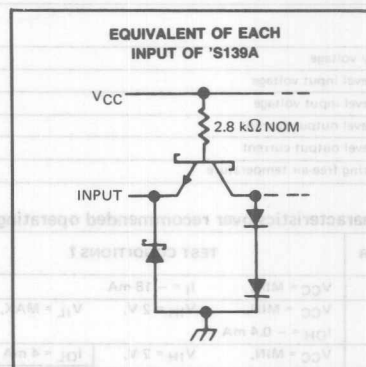
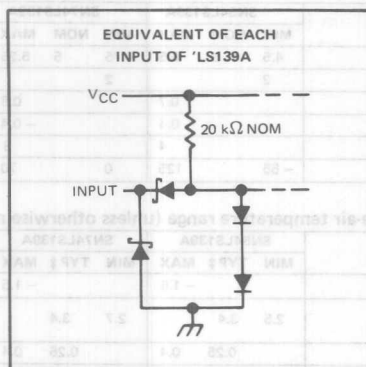
Pin numbers shown on logic notation are for D, J or N packages.

PRODUCTION DATA

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TYPES SN54LS139A, SN54S139A, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS139A, 'LS139	7 V
'S139A	5.5 V
Operating free-air temperature range: SN54LS139A, SN54S139A	-55°C to 125°C
SN74LS139A, SN54S139A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS139A, SN74LS139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54LS139A			SN74LS139A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS139A			SN74LS139A			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
	V _{IL} = MAX, I _{OL} = 8 mA				0.35	0.5		
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20		µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
I _{OS} §	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, Outputs enabled and open	6.8	11		6.8	11		mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS139A SN74LS139A		UNIT	
					MIN	TYP MAX		
tPLH	Binary Select	Any	2	RL = 2 kΩ, CL = 15 pF	13	20	ns	
tPHL					22	33	ns	
tPLH			3		18	29	ns	
tPHL					25	38	ns	
tPLH	Enable	Any	2		16	24	ns	
tPHL					21	32	ns	

† t_{PLH} = propagation delay time, low to high level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

recommended operating conditions

		SN54S139A			SN74S139A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-1			-1	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	-55	125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S139A SN74S139A			UNIT
		MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = 18 mA			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	SN54S†	2.5	3.4	V
		SN74S†	2.7	3.4	V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			50	µA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V			-2	mA
I _{OS} §	V _{CC} = MAX		-40	-100	mA
I _{CC}	V _{CC} = MAX, Outputs enabled and open	SN54S†	60	90	mA
		SN74S†	60	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S139A SN74S139A			UNIT	
					MIN	TYP	MAX		
t _{PLH}	Binary Select	Any	2	R _L = 280 Ω, C _L = 15 pF		5	7.5	ns	
t _{PHL}						6.5	10	ns	
t _{PLH}			3			7	12	ns	
t _{PHL}						8	12	ns	
t _{PLH}	Enable	Any	2			5	8	ns	
t _{PHL}						6.5	10	ns	

†t_{PLH} = propagation delay time, low to high-level output

t_{PHL} = propagation delay time, high to low-level output

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S140, SN74S140

DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 4-input positive-NAND 50-ohm line drivers. They perform the Boolean function $Y = \overline{ABCD}$.

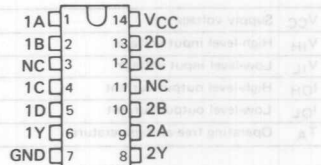
The SN54S140 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74S140 is characterized for operation from 0°C to 70°C .

logic diagram (each driver)



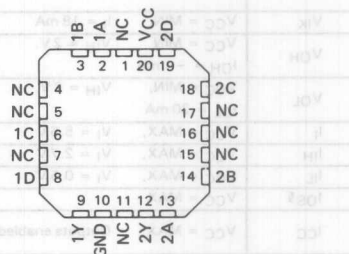
SN54S140 ... J OR W PACKAGE
SN74S140 ... D, J OR N PACKAGE

(TOP VIEW)



SN54S140 ... FK PACKAGE
SN74S140

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

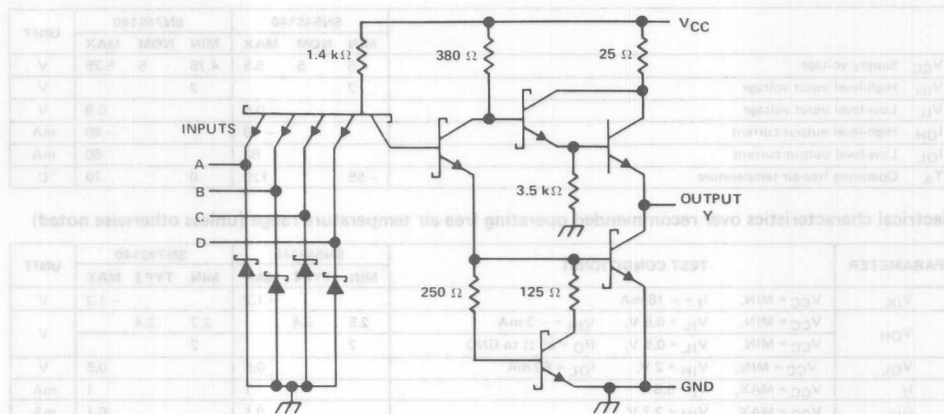
PARAMETER	TO (INPUT)	FROM (OUTPUT)	LEVEL	TEST CONDITIONS	UNIT
t _{PH}	B	S	S	R _L = 50 Ω, C _L = 15 pF	ns
					ns
					ns
					ns
t _{PL}	B	S	S	R _L = 50 Ω, C _L = 15 pF	ns
					ns
					ns
					ns

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TEXAS
INSTRUMENTS

TYPES SN54S140, SN74S140 DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PARAMETER	FROM (INPUT)	TO (OUTPUT)
t_{PLH}	Any	Y
t_{PLH}	Any	Y
t_{PLH}	Any	Y
t_{PLH}	Any	Y

NOTE 2: See General Information Section for load circuit and voltage waveform.

3

TTL DEVICES

TYPES SN54S140, SN74S140 DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

recommended operating conditions

	SN54S140			SN74S140			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-40			-40	mA
I_{OL} Low-level output current			60			60	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S140			SN74S140			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -3 \text{ mA}$	2.5	3.4		2.7	3.4		V
	$V_{CC} = \text{MIN}, V_{IL} = 0.5 \text{ V}, R_O = 50 \Omega \text{ to GND}$	2			2			
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 60 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.7 \text{ V}$			0.1			0.1	mA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.5 \text{ V}$			-4			-4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	-50		-225	-50		-225	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		10	18		10	18	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		25	44		25	44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 100 milliseconds.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 93\ \Omega,$	$C_L = 50\text{ pF}$		4	6.5	ns
t_{PHL}						4	6.5	ns
t_{PLH}			$R_L = 93\ \Omega,$	$C_L = 150\text{ pF}$		6		ns
t_{PHL}						6		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPE SN74141 BCD-TO-DECIMAL DECODER/DRIVER

DECEMBER 1972—REVISED DECEMBER 1983

- Drives Gas-filled Cold-cathode Indicator Tubes Directly
- Fully Decoded Inputs Ensure all Outputs are Off for Invalid Codes
- Input Clamping Diodes Minimize Transmission-line Effects

description

The SN74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 80 milliwatts. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

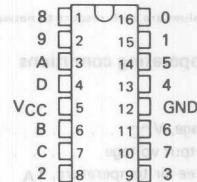
FUNCTION TABLE

INPUT	OUTPUT
D C B A	ON†
L L L L	0
L L L H	1
L L H L	2
L L H H	3
L H L L	4
L H L H	5
L H H L	6
L H H H	7
H L L L	8
H L L H	9
H L H L	NONE
H L H H	NONE
H H L L	NONE
H H L H	NONE
H H H L	NONE
H H H H	NONE

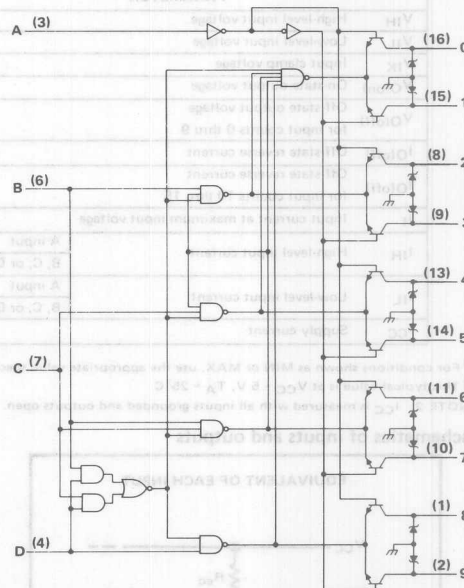
H - high level, L - low level

† All other outputs are off

J OR N PACKAGE
(TOP VIEW)



logic diagram



3

TTL DEVICES

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TEXAS
INSTRUMENTS

TYPE SN74141 BCD-TO-DECIMAL DECODER/DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current into any output (off-state)	2 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Off-state output voltage			60	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

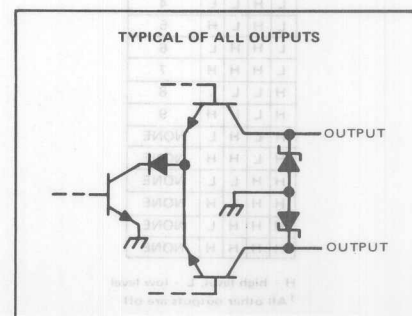
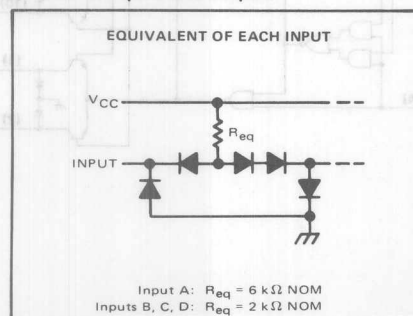
PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -5 \text{ mA}$			-1.5	V
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}$, $I_O = 7 \text{ mA}$			2.5	V
$V_{O(off)}$ Off-state output voltage for input counts 0 thru 9	$V_{CC} = \text{MAX}$, $I_O = 0.5 \text{ mA}$	60			V
$I_{O(off)}$ Off-state reverse current	$V_{CC} = \text{MAX}$, $V_O = 55 \text{ V}$			50	μA
$I_{O(off)}$ Off-state reverse current for input counts 10 thru 15	$V_{CC} = \text{MAX}$, $T_A = 55^\circ\text{C}$			5	μA
	$V_O = 30 \text{ V}$, $T_A = 70^\circ\text{C}$			15	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	A input			40	μA
	B, C, or D input			80	μA
I_{IL} Low-level input current	A input			-1.6	mA
	B, C, or D input			-3.2	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		16	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ This typical value is at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54143, SN54144, SN74143, SN74144 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

NOVEMBER 1971—REVISED DECEMBER 1983

Choice of Driver Outputs:

SN54143 and SN74143 have 15 mA Constant-Current Outputs for Driving Common-Anode LED's such as TIL302 or TIL303 without Series Resistors

SN54144 and SN74144 Drive High-Current Lamps, Numitrons[†], or LED's from Saturated Open-Collector Outputs

Universal Logic Capabilities

Ripple Blanking of Extraneous Zeros
Latch Outputs Can Drive Logic Processors
Simultaneously

Decimal Point Driver Is Included

Synchronous BCD Counter Capability

Includes:

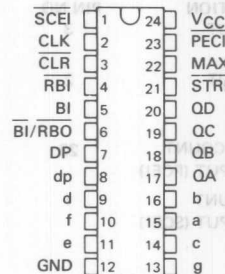
Cascadable to N-Bits

Look-Ahead-Enable Techniques Minimize Speed Degradation When Cascaded for Large-Word Display

Direct Clear Input

SN54143, SN54144 ... J OR W PACKAGE
SN74143, SN74144 ... J OR N PACKAGE

(TOP VIEW)



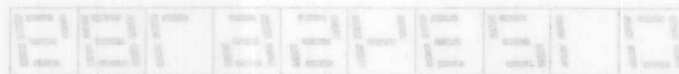
description

These TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-count-enable, actually two internal emitters, is rated as one standard Series 54/74 load. The logic outputs, except RBO, have active pull-ups.

The SN54143 and SN74143 driver outputs are designed specifically to maintain a relatively constant on-level sink current of approximately 15 milliamperes from output "a" through "g" and seven milliamperes from output "dp" over a voltage range from one to five volts. Any number of LED's in series may be driven as long as the output voltage rating is not exceeded.

The SN54144 and SN74144 have high-sink-current saturated outputs for driving indicators having voltage ratings up to 15 volts or requiring up to 25 milliamperes drive. The SN54144 sinks 20 milliamperes and the SN74144 sinks 25 milliamperes at an on-level voltage of 0.6 volts across their respective operating temperature ranges.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 280 milliwatts. The SN54143 and SN54144 are characterized for operation over the full military temperature range of -55°C to 125°C; the SN74143 and SN74144 are characterized for operation from 0°C to 70°C.



[†] Trademark of RCA

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TEXAS
INSTRUMENTS

3-431

3
TTL DEVICES

TYPES SN54143, SN54144, SN74143, SN74144

4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

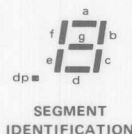
description (continued)

Functions of the inputs and outputs of these devices are as follows:

FUNCTION	PIN NO.	DESCRIPTION
CLEAR INPUT	3	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	2	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	23	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	1	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	22	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	21	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q _A , Q _B , Q _C , Q _D)	17, 18, 19, 20	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: Q _A = 1, Q _B = 2, Q _C = 4, Q _D = 8.
DECIMAL POINT INPUT	7	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	5	When high, will blank (turn off) the entire display and force \overline{RBO} low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (\overline{RBI})	4	When the data in the latches is BCD 0, a low input will blank the entire display and force the \overline{RBO} low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (\overline{RBO})	6	Supplies ripple blanking information for the ripple blanking input of the next decade. Provides a low if BI is high, or if \overline{RBI} is low and the data in the latches is BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.
LED/LAMP DRIVER OUTPUTS (a, b, c, d, e, f, g, dp)	15, 16, 14, 9 11, 10, 13, 8	Outputs for driving seven-segment LED's or lamps and their decimal points. See segment identification and resultant displays on following page.

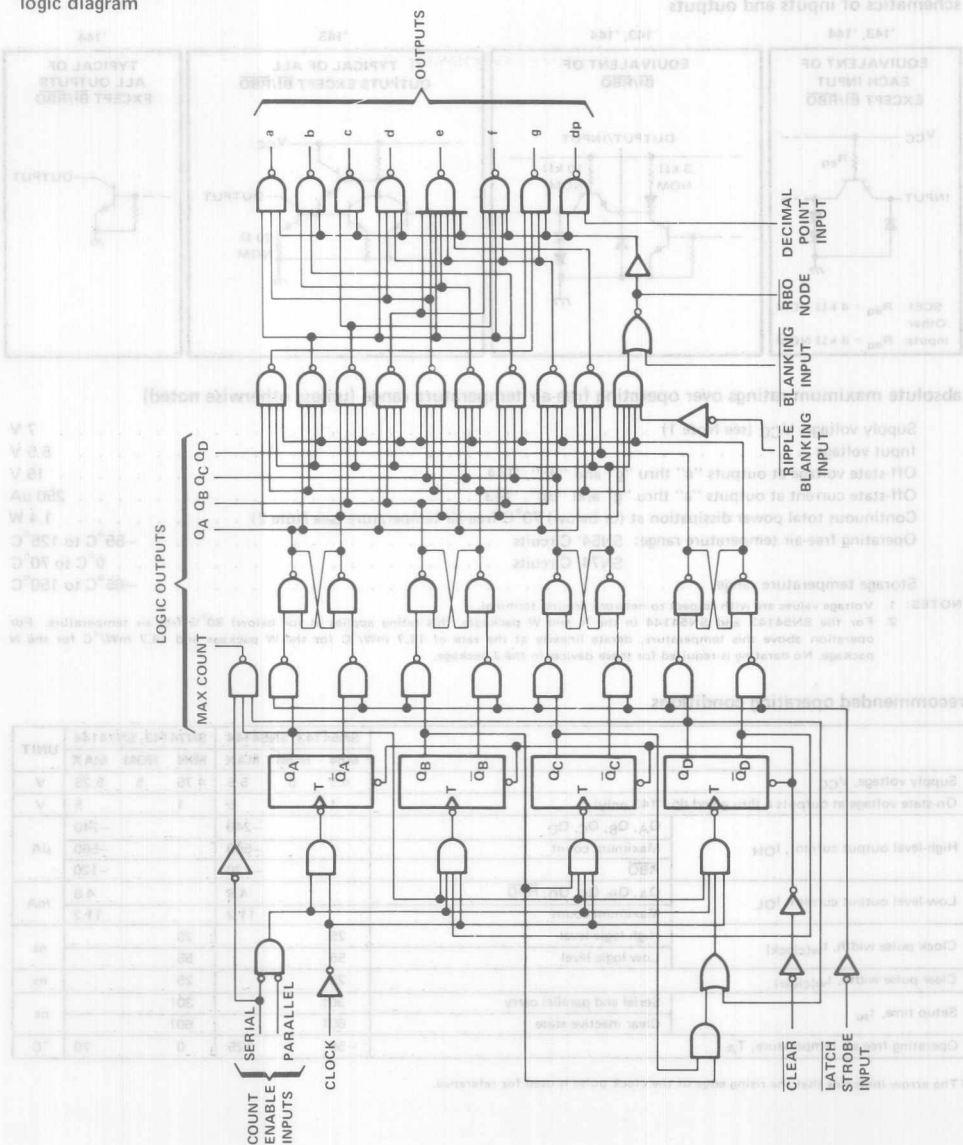
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TTL DEVICES



TYPES SN54143, SN54144, SN74143, SN74144 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

logic diagram

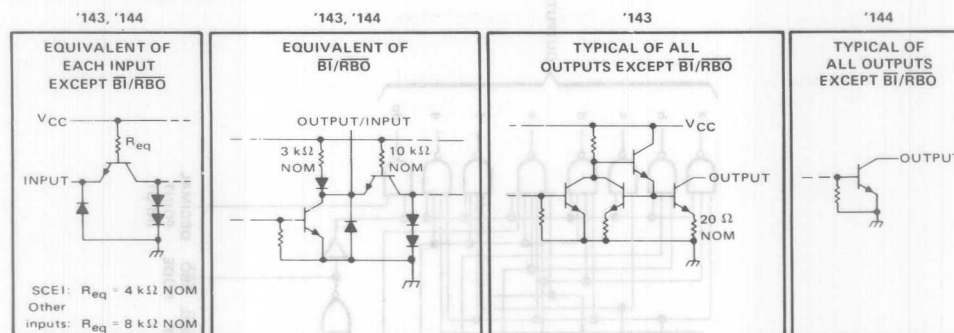


3

TTL DEVICES

TYPES SN54143, SN54144, SN74143, SN74144 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage at outputs "a" thru "g" and "dp", '144	15 V
Off-state current at outputs "a" thru "g" and "dp", '143	250 μ A
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 2)	1.4 W
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For the SN54143 and SN54144 in the N and W packages, this rating applies at (or below) 80°C free-air temperature. For operation above this temperature, derate linearly at the rate of 11.7 mW/°C for the W package and 14.7 mW/°C for the N package. No derating is required for these devices in the J package.

recommended operating conditions

		SN54143, SN54144			SN74143, SN74144			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
On-state voltage at outputs a thru g and dp ('143 only)		1		5	1		5	V
High-level output current, I_{OH}	Q_A, Q_B, Q_C, Q_D			-240			-240	μ A
	Maximum count			-560			-560	
	RBO			-120			-120	
Low-level output current, I_{OL}	Q_A, Q_B, Q_C, Q_D, RBO			4.8			4.8	mA
	Maximum count			11.2			11.2	
Clock pulse width, $t_{w(\text{clock})}$	High logic level	25			25			ns
	Low logic level	55			55			
Clear pulse width, $t_{w(\text{clear})}$		25			25			ns
Setup time, t_{su}	Serial and parallel carry	30†			30†			ns
	Clear inactive state	60†			60†			
Operating free-air temperature, T_A		-55		125	0		70	°C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

3

TTL DEVICES

TYPES SN54143, SN54144, SN74143, SN74144 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54143, SN74143			SN54144, SN74144			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = 12 mA			1.5			1.5	V
V _{OH}	High-level output voltage	R _{B0}							
		Q _A , Q _B , Q _C , Q _D							
		Maximum count	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	2.4		2.4			V
V _{OL}	Low-level output voltage	Q _A , Q _B , Q _C , Q _D , R _{B0}							
		Maximum count	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX		0.4			0.4	V
V _{O(off)}	Off-state output voltage	Outputs a thru g, dp	V _{CC} = MAX, I _{OH} = 250 µA	7		15			V
V _{O(on)}	On-State output voltage	Outputs a thru g, dp	V _{CC} = MIN, See Note 3					0.6	V
I _{O(on)}	On-state output current	Outputs a thru g	V _{CC} = MIN, V _O = 1 V	9	15				mA
			V _{CC} = 5 V, V _O = 2 V		15				
			V _{CC} = MAX, V _O = 5 V		15	22			
		Output dp	V _{CC} = MIN, V _O = 1 V	4.5	7				
			V _{CC} = 5 V, V _O = 2 V		7				
			V _{CC} = MAX, V _O = 5 V		7	12			
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 5.5 V		1			1	mA
I _{IH}	High-level input current	Serial carry			40			40	µA
		R _{B0} node	V _{CC} = MAX, V _I = 2.4 V	-0.12	-0.5	0.12	0.5		mA
		Other inputs			20			20	µA
I _{IL}	Low-level input current	Serial carry			1.6			1.6	mA
		R _{B0} node	V _{CC} = MAX, V _I = 0.4 V, See Note 4	-1.5	-2.4	1.5	2.4		mA
		Other inputs			-0.8			0.8	mA
I _{OS}	Short-circuit output current	Q _A , Q _B , Q _C , Q _D	V _{CC} = MAX	-9	27.5	9	27.5		mA
		Maximum count		15	55	15	55		mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 5	56	93	56	93		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. For SN54144, I_{OL} = 20 mA; for SN74144, I_{OL} = 25 mA.

4. I_{IL} at R_{B0} node is tested with \overline{BT} grounded and RBI at 4.5 V.

5. I_{CC} is measured after the following conditions are established:

- Strobe = R_{B0} = DP = 4.5 V
- Parallel count enable = serial count enable = \overline{BT} = GND
- Clear (\overline{CLR}) then clock until all outputs are on (\overline{Q})
- For '143, outputs "a" through "g" and "dp" = 2.5 V, all other outputs open. For '144, all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER §	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{max}				12	18		MHz
t _{PLH}	Serial look-ahead	Maximum count	C _L = 15 pF, R _L = 560 Ω, See Note 6	12	20		ns
t _{PHL}				23	35		
t _{PLH}	Clock	Maximum count	C _L = 15 pF, R _L = 1.2 kΩ, See Note 6	26	40		ns
t _{PHL}				29	45		
t _{PLH}	Clock	Q _A , Q _B , Q _C , Q _D	C _L = 15 pF, R _L = 1.2 kΩ, See Note 6	28	45		ns
t _{PHL}				38	60		
t _{PHL}	Clear	Q _A , Q _B , Q _C , Q _D		57	90		ns

§ t_{max} = Maximum clock frequency, t_{PLH} = Propagation delay time, low to high level output.

t_{PHL} = Propagation delay time, high to low level output

NOTE 6: See General Information Section for load circuits and voltage waveforms.

TYPES SN54143, SN54144, SN74143, SN74144
4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

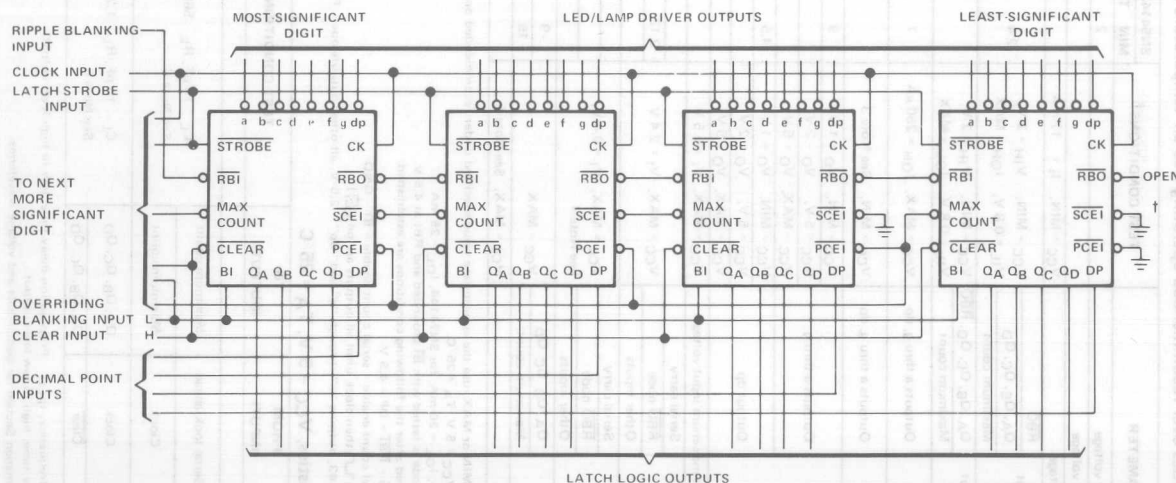
TTL DEVICES

3

TYPICAL APPLICATION DATA

This application demonstrates how the drivers may be cascaded for N-bit display applications. It features:

- Synchronous, look-ahead counting
- Ripple blanking of leading zeros; blanking of trailing zeros (not illustrated) can also be implemented
- Overriding blanking for total suppression or intensity modulation of display
- Direct parallel clear
- Latch strobe permits counter to acquire next display while viewing current display



† The serial count-enable input of the least-significant digit is normally grounded; however, it may be used as a count-enable control for the entire counter (high to disable, low to count) provided the logic level on this pin is not changed while the clock line is low or false counting may result.

FUNCTION TABLE

FUNCTION	CLOCK PULSE	INPUTS							RBI/RBO	MAXIMUM COUNT OUTPUT	OUTPUTS													TYPICAL DISPLAY	NOTES
		CLEAR	LATCH STROBE	RBI	BI	DECIMAL INPUT	SERIAL CARRY	PARALLEL CARRY			LATCH				LED/LAMP DRIVERS										
Clear, Ripple Blank		L	L	L	X	X	X	X	L	H	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	None	A, E		
Blank		H	L	X	H	X	X	X	L	H	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	None	A, D		
Decimal	0	H	L	H	L	H	L	L	H	H	L	L	L	L	ON	ON	ON	ON	ON	ON	OFF	0	B		
	1	H	L	H	L	L	L	L	H	H	L	L	L	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1	B		
	2	H	L	H	L	L	L	L	H	H	L	L	H	L	ON	ON	OFF	ON	ON	OFF	ON	2	B		
	3	H	L	H	L	L	L	L	H	H	L	L	H	H	ON	ON	ON	ON	OFF	OFF	ON	OFF	3	B	
	4	H	L	H	L	L	L	L	H	H	L	H	L	L	OFF	ON	ON	OFF	OFF	ON	ON	OFF	4	B	
	5	H	L	H	L	L	L	L	H	H	L	H	L	H	ON	OFF	ON	ON	OFF	ON	ON	OFF	5	B	
	6	H	L	H	L	L	L	L	H	H	L	H	H	L	ON	OFF	ON	ON	ON	ON	ON	OFF	6	B	
	7	H	L	H	L	L	L	L	H	H	L	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	7	B	
	8	H	L	H	L	L	L	L	H	H	H	L	L	L	ON	ON	ON	ON	ON	ON	ON	OFF	8	B	
	9	H	L	H	L	L	L	L	H	L	H	L	L	H	ON	ON	ON	ON	OFF	ON	ON	OFF	9	B	
	0	H	L	H	L	L	L	L	H	H	L	L	L	L	ON	ON	ON	ON	ON	ON	OFF	OFF	0	B, C	
	1	H	L	H	L	L	L	L	H	H	L	L	L	H	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	1	B	
	2	H	L	H	L	L	L	L	H	H	L	L	H	L	ON	ON	OFF	ON	ON	OFF	ON	OFF	2	B	
	3	H	L	H	L	L	L	L	H	H	L	L	H	H	ON	ON	ON	ON	OFF	OFF	ON	OFF	3	B	
	4	H	L	H	L	L	L	L	H	H	L	H	L	L	OFF	ON	ON	OFF	OFF	ON	ON	OFF	4	B	
	5	H	H	H	L	L	L	L	H	H	L	H	L	H	ON	OFF	ON	ON	OFF	ON	ON	OFF	5	B	
Latch	6	H	H	H	L	L	L	L	H	H	L	H	L	H	ON	OFF	ON	ON	OFF	ON	ON	OFF	6	B	
Latch	7	H	H	H	L	L	L	L	H	H	L	H	L	H	ON	OFF	ON	ON	OFF	ON	ON	OFF	7	B	
	8	H	L	H	L	L	L	L	H	H	H	L	L	L	ON	ON	ON	ON	ON	ON	ON	OFF	8	B	
	9	H	L	H	L	L	L	L	H	L	H	L	L	H	ON	ON	ON	ON	OFF	ON	ON	OFF	9	B	
Ripple Blank	0	H	L	L	X	L	L	L	L	H	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	None	A, B, E		

- NOTES: A. $\overline{\text{RBI}}/\overline{\text{RBO}}$ is wire-AND logic serving as ripple blanking input ($\overline{\text{RBI}}$) and/or ripple blanking output ($\overline{\text{RBO}}$).
 B. The blanking input ($\overline{\text{BI}}$) must be low when functions DECIMAL/0 through 20/RIPPLE BLANK are desired.
 C. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high to display a zero during the decimal 0 input.
 D. When a high logic level is applied directly to the blanking input ($\overline{\text{BI}}$) all segment outputs are off regardless of any other input condition.
 E. When the ripple-blanking input ($\overline{\text{RBI}}$) and outputs Q_A through Q_D are at a low logic level, all segment outputs are off and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a low logic level (response condition).



SEGMENT IDENTIFICATION

TYPES SN54145, SN54LS145, SN74145, SN74LS145 BCD-TO-DECIMAL DECODERS/DRIVERS

MARCH 1974—REVISED DECEMBER 1983

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Full Decoding of Input Logic
- SN54145, SN74145, and SN74LS145 Have 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145 ... 35 mW Typical

logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

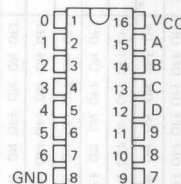
H = high level (off), L = low level (on)

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) of the SN54145, SN74145, or SN74LS145 will sink up to 80 milliamperes of current. Each input is one Series 54/74 or Series 54LS/74LS standard load, respectively. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts for the '145 and 35 milliwatts for the 'LS145.

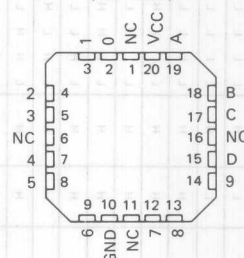
SN54145, SN54LS145 ... J OR W PACKAGE
SN74145 ... J OR N PACKAGE
SN74LS145 ... D, J OR N PACKAGE

(TOP VIEW)



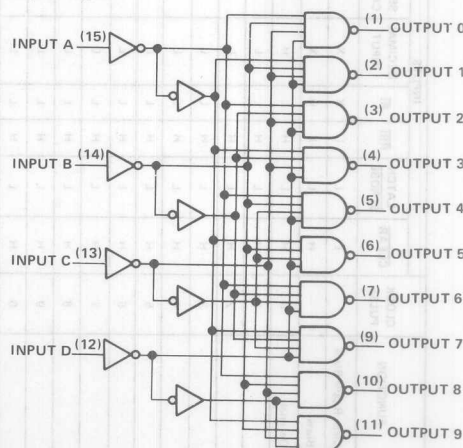
SN54LS145 ... FK PACKAGE
SN74LS145

(TOP VIEW)



NC - No internal connection

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54145, SN74145 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Maximum current into any output (off-state)	1 mA
Operating free-air temperature range: SN54145	-55°C to 125°C
SN74145	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54145			SN74145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
$I_{O(off)}$ Off-state output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{O(off)} = 15 \text{ V}$			250	µA
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$				
	$I_{O(on)} = 80 \text{ mA}$	0.5	0.9		V
	$I_{O(on)} = 20 \text{ mA}$		0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$				mA
		SN54145	43	62	
		SN74145	43	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

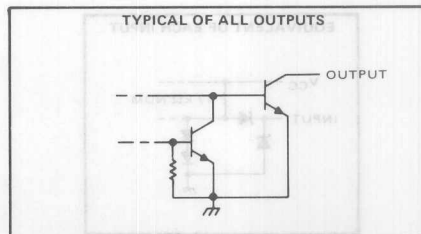
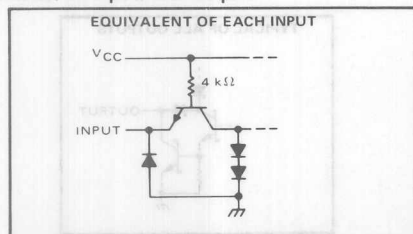
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 100 \Omega, \text{ See Note 3}$		50	ns
t_{PHL} Propagation delay time, high-to-low-level output			50	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



TYPES SN54LS145, SN74LS145 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS145	-55°C to 125°C
SN74LS145	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS145			SN74LS145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS145			SN74LS145			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$		-1.5			-1.5		V
$I_{O(off)}$ Off-state output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 15 \text{ V}$		250			250		μA
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{IH} = 2 \text{ V}$, $I_{OL} = 24 \text{ mA}$				0.35	0.5		V
	$V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 80 \text{ mA}$				2.3	3		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		20			20		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	7	13		7	13		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

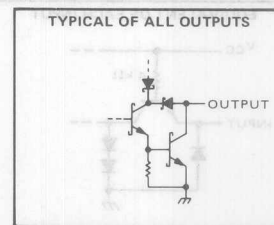
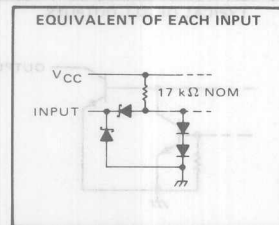
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}$, $R_L = 665 \Omega$, See Note 3		50	ns
t_{PHL} Propagation delay time, high-to-low-level output			50	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

schematic of inputs and outputs



3

TTL DEVICES

TYPES SN54147, SN54148, SN54LS147, SN54LS148, SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

OCTOBER 1976—REVISED DECEMBER 1983

'147, 'LS147

- Encodes 10-Line Decimal to 4-Line BCD
- Applications Include:

Keyboard Encoding

Range Selection: '148, 'LS148

- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:

N-Bit Encoding

Code Converters and Generators

TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION
'147	10 ns	225 mW
'148	10 ns	190 mW
'LS147	15 ns	60 mW
'LS148	15 ns	60 mW

description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54LS/74LS load, respectively.

'147, 'LS147

FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

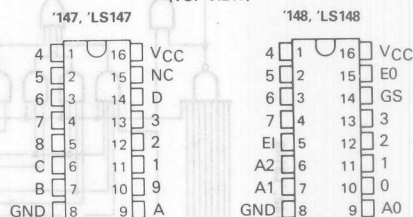
SN54147, SN54LS147,

SN54148, SN54LS148 ... J OR W PACKAGE

SN74147, SN74148 ... J OR N PACKAGE

SN74LS147, SN74LS148 ... D, J OR N PACKAGE

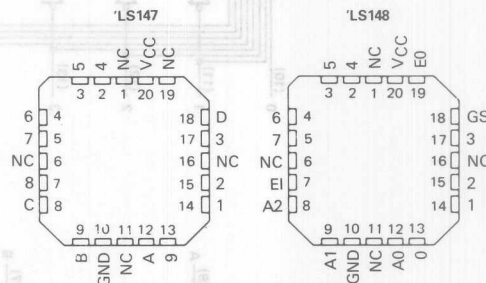
(TOP VIEW)



SN54LS147, SN54LS148 ... FK PACKAGE

SN74LS147, SN74LS148

(TOP VIEW)



NC - No internal connection

'148, 'LS148

FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS
H	X	X	X	X	X	X	X	X	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	H
L	X	X	L	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	L	H

PRODUCTION DATA

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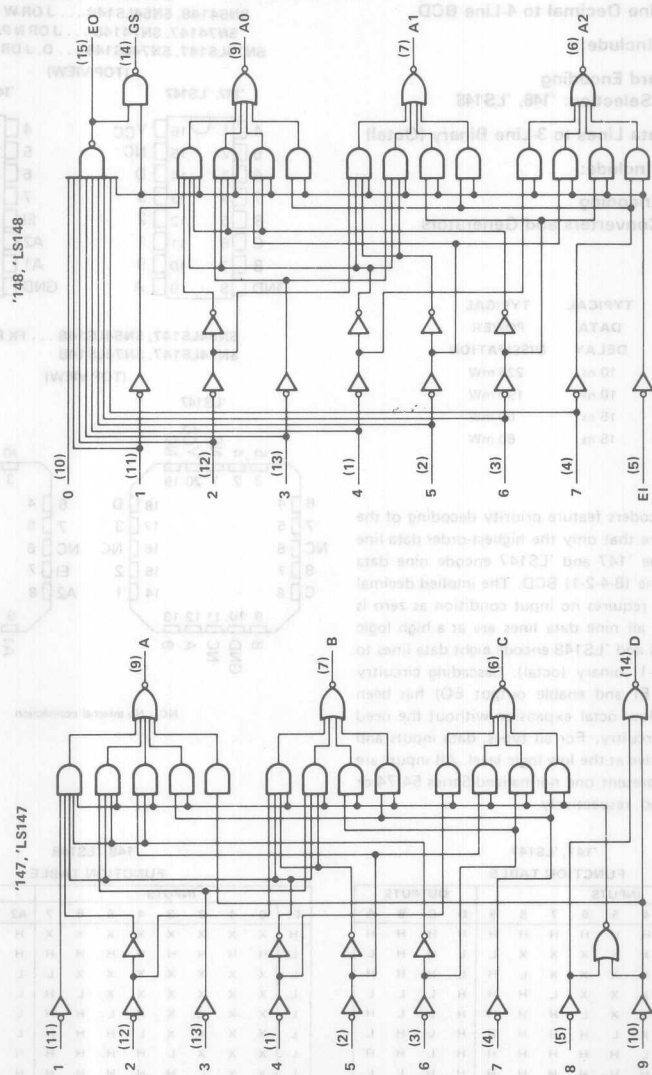
TEXAS
INSTRUMENTS

**TYPES SN54147, SN54148, SN54LS147, SN54LS148,
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

logic diagram

3

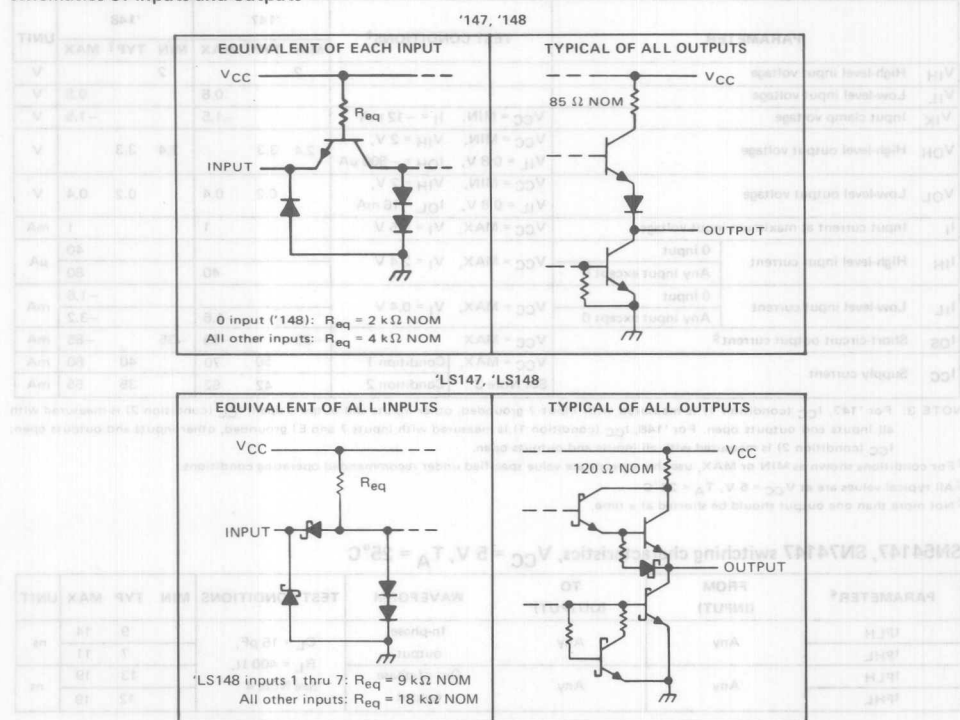
TTL DEVICES



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54147, SN54148, SN54LS147, SN54LS148,
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '147, '148	5.5 V
'LS147, 'LS148	7 V
Interemitter voltage: '148 only (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54LS Circuits	-55°C to 125°C
SN74', SN74LS Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.

recommended operating conditions

	SN54'			SN74'			SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800			-400			-400	μA
Low-level output current, I_{OL}			16			16			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	-55		125	0		70	°C

TYPES SN54147, SN54148, SN74147, SN74148 (TIM9907) 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'147			'148			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage			0.8			0.8		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA		-1.5			-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.3		2.4	3.3		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2	0.4		0.2	0.4		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	0 input					40		µA
	Any input except 0		40			80		µA
I _{IL} Low-level input current	0 input					-1.6		mA
	Any input except 0		-1.6			-3.2		mA
I _{OS} Short-circuit output current‡	V _{CC} = MAX	-35	-85		-35	-85		mA
I _{CC} Supply current	V _{CC} = MAX, Condition 1	50	70		40	60		mA
	See Note 3, Condition 2	42	62		35	55		mA

NOTE 3: For '147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For '148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

SN54147, SN74147 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Any	In-phase output	C _L = 15 pF, R _L = 400 Ω, See Note 4	9	14		ns
t _{PHL}			Out-of-phase output		7	11		ns
t _{PLH}	Any	Any	Out-of-phase output		13	19		ns
t _{PHL}			In-phase output		12	19		ns

SN54148, SN74148 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C _L = 15 pF, R _L = 400 Ω, See Note 4	10	15		ns
t _{PHL}			Out-of-phase output		9	14		ns
t _{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output		13	19		ns
t _{PHL}			In-phase output		12	19		ns
t _{PLH}	0 thru 7	EO	Out-of-phase output		6	10		ns
t _{PHL}			In-phase output		14	25		ns
t _{PLH}	0 thru 7	GS	In-phase output		18	30		ns
t _{PHL}			Out-of-phase output		14	25		ns
t _{PLH}	EI	A0, A1, or A2	In-phase output		10	15		ns
t _{PHL}			Out-of-phase output		10	15		ns
t _{PLH}	EI	GS	In-phase output		8	12		ns
t _{PHL}			Out-of-phase output		10	15		ns
t _{PLH}	EI	EO	In-phase output		10	15		ns
t _{PHL}			Out-of-phase output		17	30		ns

¶t_{PLH} = propagation delay time, low to high level output

t_{PHL} = propagation delay time, high to low level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS147, SN54LS148, SN74LS147, SN74LS148 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
		MIN	TYP‡	MAX	MIN TYP‡ MAX	
V _{IH} High-level input voltage		2			2	V
V _{IL} Low-level input voltage				0.7		0.8 V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5 V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 µA	2.5	3.4		2.7 3.4	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25 0.4		0.25 0.4	V
	V _{IL} = V _{ILmax} , I _{OL} = 8 mA				0.35 0.5	
I _I Input current at maximum input voltage	'LS148 inputs 1 thru 7			0.2		mA
	All other inputs			0.1		
I _{IH} High-level input current	'LS148 inputs 1 thru 7			40		µA
	All other inputs			20		
I _{IL} Low-level input current	'LS148 inputs 1 thru 7			-0.8		mA
	All other inputs			-0.4		
I _{OS} Short-circuit output current§	V _{CC} = MAX	-20	-100		-20 -100	mA
I _{CC} Supply current	V _{CC} = MAX, Condition 1	12	20		12 20	mA
	See Note 5, Condition 2	10	17		10 17	

NOTE 5: For 'LS147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For 'LS148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open, I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

SN54LS147, SN74LS147 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Any	In-phase output	C _L = 15 pF, R _L = 2 kΩ, See Note 4	12	18		ns
t _{PHL}					12	18		
t _{PLH}	Any	Any	Out-of-phase output		21	33		ns
t _{PHL}					15	23		

SN54LS148, SN74LS148 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C _L = 15 pF, R _L = 2 kΩ, See Note 4	14	18		ns
t _{PHL}			output		15	25		
t _{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output		20	36		ns
t _{PHL}			output		16	29		
t _{PLH}	0 thru 7	EO	Out-of-phase output		7	18		ns
t _{PHL}			output		25	40		
t _{PLH}	0 thru 7	GS	In-phase output		35	55		ns
t _{PHL}			output		9	21		
t _{PLH}	EI	A0, A1, or A2	In-phase output		16	25		ns
t _{PHL}			output		12	25		
t _{PLH}	EI	GS	In-phase output		12	17		ns
t _{PHL}			output		14	36		
t _{PLH}	EI	EO	In-phase output		12	21		ns
t _{PHL}			output		23	35		

†t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

3 TTL DEVICES

The diagram illustrates a 16-to-4 priority encoder circuit. It consists of two 74148/LS148 8-to-3 priority encoders and one 7408/LS08 4-to-1 multiplexer.

- 16-LINE DATA (ACTIVE LOW):** A 16-bit bus at the top, labeled 0 through 15. Pins 8 through 15 are connected to the inputs of the two 74148 chips.
- ENABLE (ACTIVE LOW):** Pin 15 is connected to the \overline{EI} pin of the right 74148 chip. Pin 8 is connected to the \overline{EI} pin of the left 74148 chip.
- 74148/LS148 Chips:**
 - Left Chip:** Inputs 0-7 are connected to data lines 0-7. Its \overline{EO} output is connected to data line 0, and its \overline{GS} output is connected to data line 1.
 - Right Chip:** Inputs 8-15 are connected to data lines 8-15. Its \overline{EO} output is connected to data line 2, and its \overline{GS} output is connected to data line 3.
- 7408/LS08 Multiplexer:** A dashed box containing four 2-input AND gates.
 - Inputs 0, 1, and 2 are connected to the $\overline{A0}$, $\overline{A1}$, and $\overline{A2}$ pins of the left 74148 chip.
 - Inputs 1, 2, and 3 are connected to the $\overline{A0}$, $\overline{A1}$, and $\overline{A2}$ pins of the right 74148 chip.
 - The output of the AND gate with inputs 0, 1, and 2 is connected to data line 0.
 - The output of the AND gate with inputs 1, 2, and 3 is connected to data line 1.
 - The output of the AND gate with inputs 2 and 3 is connected to data line 2.
 - The output of the AND gate with inputs 1, 2, and 3 (the fourth gate) is connected to data line 3.
- ENCODED DATA (ACTIVE LOW):** A 4-bit bus at the bottom, labeled 0 through 3, representing the final 4-bit output of the encoder.
- PRIORITY FLAG (ACTIVE LOW):** A single output line at the bottom right, which is the \overline{GS} output of the right 74148 chip.

The diagram illustrates a 4-bit priority encoder circuit. It consists of two 74LS148 chips and one 74LS00 chip.

- 74LS148 Chip 1 (Left):**
 - Inputs: 0, 1, 2, 3, 4, 5, 6, 7, 8.
 - Outputs: EO, A0, A1, A2, GS.
- 74LS148 Chip 2 (Right):**
 - Inputs: 8, 9, 10, 11, 12, 13, 14, 15.
 - Outputs: EO, A0, A1, A2, GS.
- 74LS00 Chip (Bottom):**
 - Inputs: 0, 1, 2, 3.
 - Output: Priority Flag (Active High).

Connections:

- The **ENABLE (ACTIVE LOW)** pin of both 74LS148 chips is connected to a common ground.
- The **EO** (End of Output) pin of the first 74LS148 chip is connected to the **GS** (Group Select) pin of the second 74LS148 chip.
- The **A0**, **A1**, and **A2** outputs of the first 74LS148 chip are connected to the inputs 0, 1, and 2 of the 74LS00 chip.
- The **A0**, **A1**, and **A2** outputs of the second 74LS148 chip are connected to the inputs 1, 2, and 3 of the 74LS00 chip.
- The **EO** output of the second 74LS148 chip is connected to the input 3 of the 74LS00 chip.
- The output of the 74LS00 chip is the **PRIORITY FLAG (ACTIVE HIGH)**.

ENCODED DATA (ACTIVE HIGH) is indicated by the outputs A0, A1, and A2 of the first 74LS148 chip.

TEXAS
INSTRUMENTS

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151 DATA SELECTORS/MULTIPLEXERS

DECEMBER 1972—REVISED DECEMBER 1983

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

TYPE	TYPICAL AVERAGE		TYPICAL POWER DISSIPATION
	PROPAGATION DELAY TIME	DATA INPUT TO W OUTPUT	
'150	13 ns		200 mW
'151A	8 ns		145 mW
'152A	8 ns		130 mW
'LS151	13 ns		30 mW
'LS152	13 ns		28 mW
'S151	4.5 ns		225 mW

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

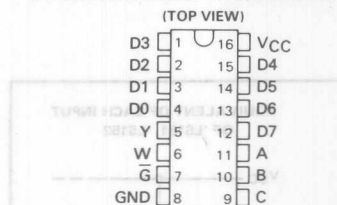
The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

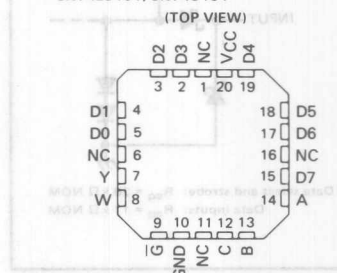
SN54150 ... J OR W PACKAGE
SN74150 ... J OR N PACKAGE



SN54151A, SN54LS151, SN54S151 ... J OR W PACKAGE
SN74151A ... J OR N PACKAGE
SN74LS151, SN74S151 ... D, J OR N PACKAGE

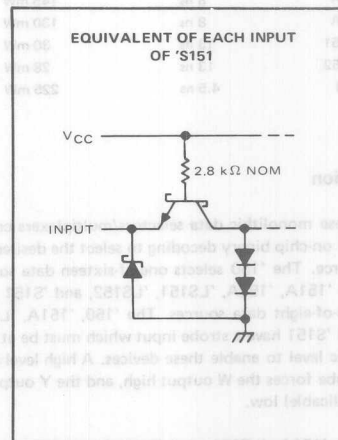
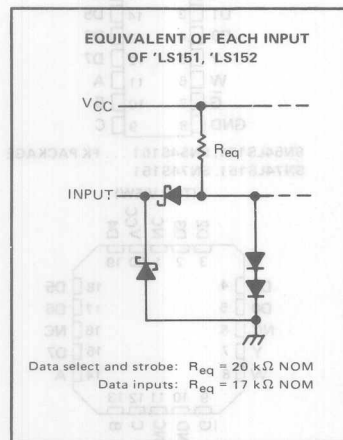
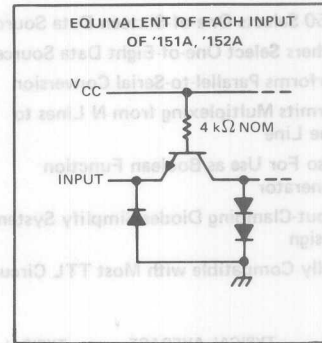
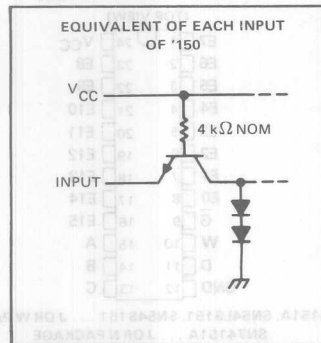


SN54LS151, SN54S151 ... FK PACKAGE
SN74LS151, SN74S151



**TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151,
SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS**

schematics of inputs and outputs

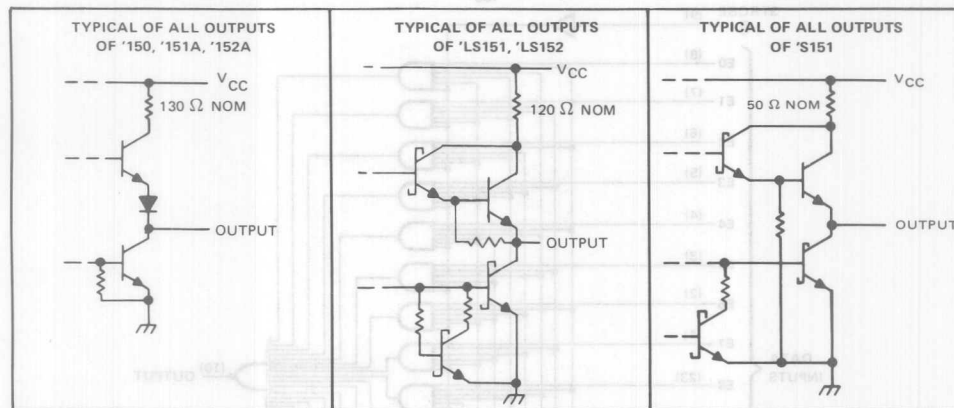


3

TTL DEVICES

**TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151
SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS**

schematics of inputs and outputs



logic

'150
FUNCTION TABLE

INPUTS				STROBE \bar{G}	OUTPUT W
D	C	B	A		
X	X	X	X	H	H
L	L	L	L	L	$\bar{E}0$
L	L	L	H	L	$\bar{E}1$
L	L	H	L	L	$\bar{E}2$
L	L	H	H	L	$\bar{E}3$
L	H	L	L	L	$\bar{E}4$
L	H	L	H	L	$\bar{E}5$
L	H	H	L	L	$\bar{E}6$
L	H	H	H	L	$\bar{E}7$
H	L	L	L	L	$\bar{E}8$
H	L	L	H	L	$\bar{E}9$
H	L	H	L	L	$\bar{E}10$
H	L	H	H	L	$\bar{E}11$
H	H	L	L	L	$\bar{E}12$
H	H	L	H	L	$\bar{E}13$
H	H	H	L	L	$\bar{E}14$
H	H	H	H	L	$\bar{E}15$

'151A, 'LS151, 'S151
FUNCTION TABLE

INPUTS			STROBE \bar{G}	OUTPUTS	
C	B	A		Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\bar{D}0$
L	L	H	L	D1	$\bar{D}1$
L	H	L	L	D2	$\bar{D}2$
L	H	H	L	D3	$\bar{D}3$
H	L	L	L	D4	$\bar{D}4$
H	L	H	L	D5	$\bar{D}5$
H	H	L	L	D6	$\bar{D}6$
H	H	H	L	D7	$\bar{D}7$

'152A, 'LS152
FUNCTION TABLE

SELECT INPUTS			OUTPUT W
C	B	A	
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

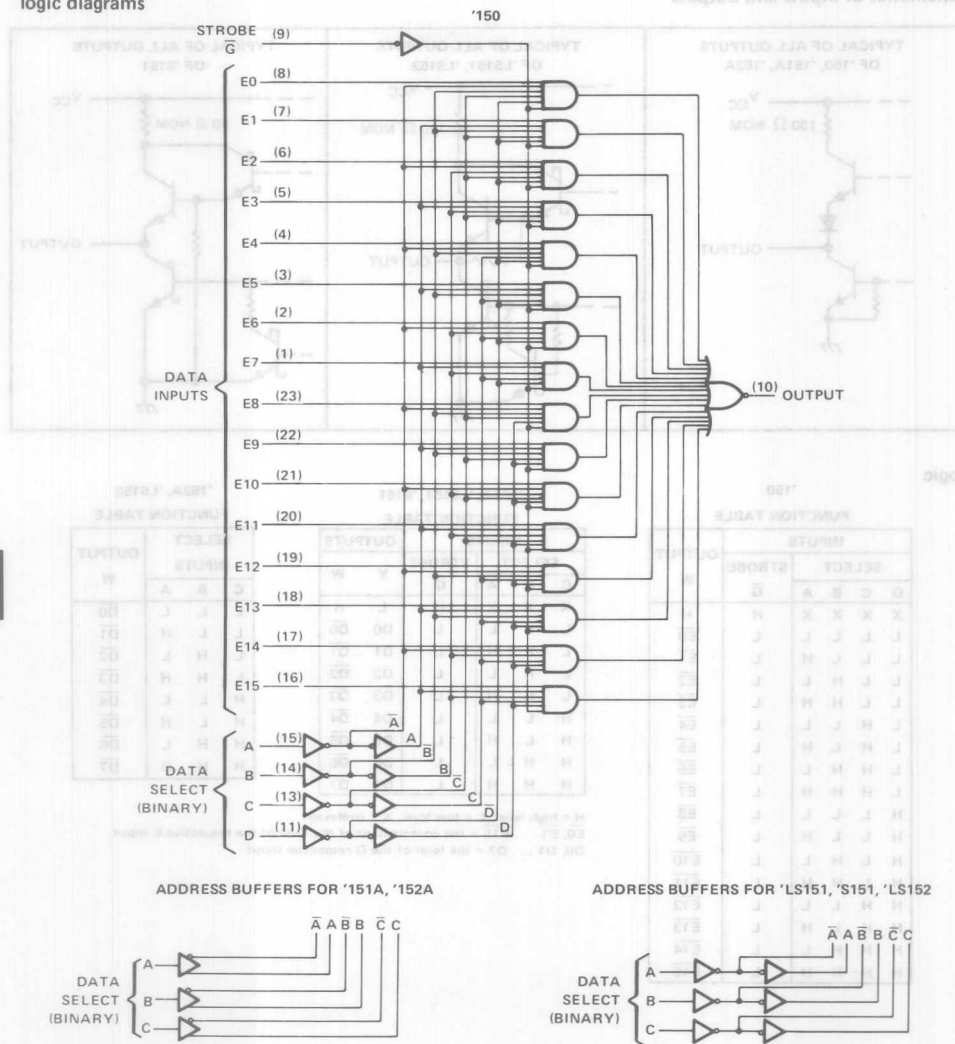
H = high level, L = low level, X = irrelevant
 $\bar{E}0, \bar{E}1 \dots \bar{E}15$ = the complement of the level of the respective E input
 D0, D1 ... D7 = the level of the D respective input

3

TTL DEVICES

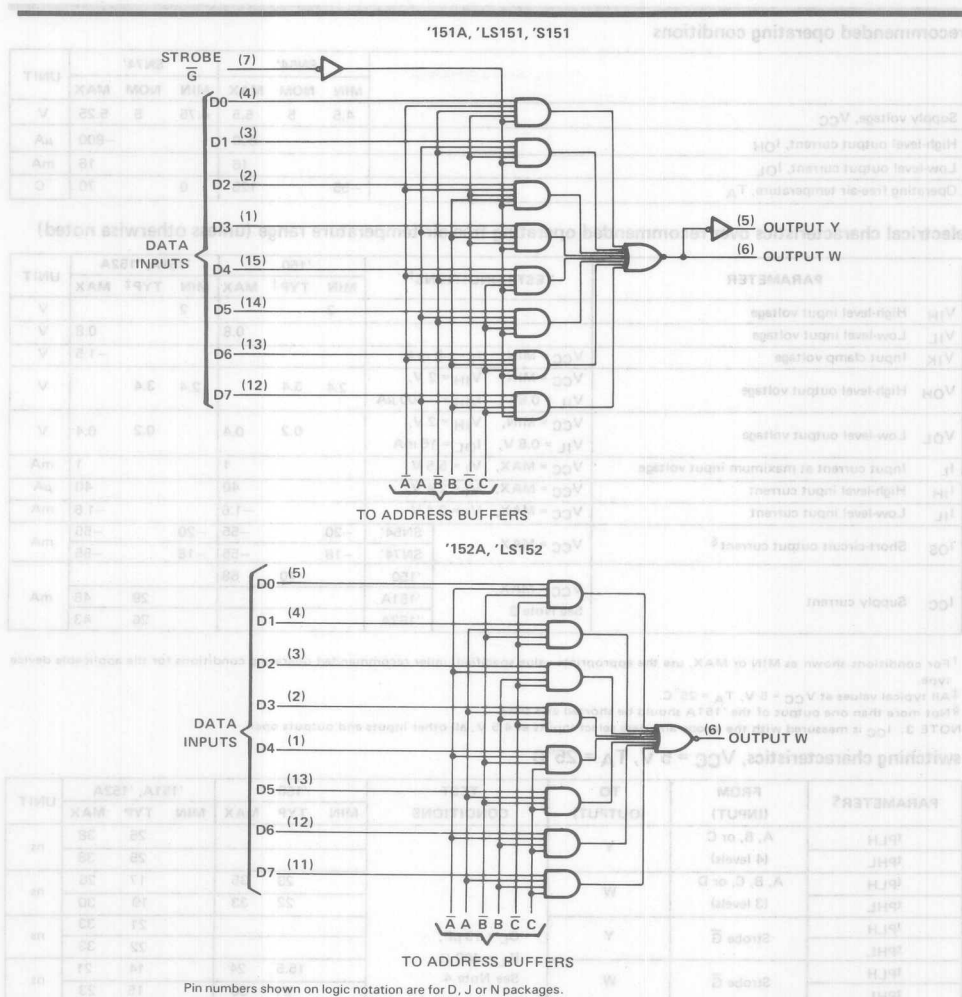
**TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151,
SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS**

logic diagrams



Pin numbers shown on logic notation are for D, J or N packages.

**TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151,
SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS**



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2): '150, '151A, 'S151, '152A	5.5 V
'LS151, 'LS152	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For the '150, input voltages must be zero or positive with respect to network ground terminal.

TYPES SN54150, SN54151A, SN54152A, SN74150, SN74151A DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'150			'151A, '152A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$						-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54'	-20	-55	-20	-55		mA
		SN74'	-18	-55	-18	-55		
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3	'150		40	68			mA
		'151A			29	48		
		'152A			26	43		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output of the '151A should be shorted at a time.

NOTE 3: I_{CC} is measured with the strobe and data select inputs at 4.5 V, all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'150			'151A, '152A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	A, B, or C (4 levels)	Y	CL = 15 pF, RL = 400 Ω, See Note 4				25	38		ns
tPHL							25	38		
tPLH	A, B, C, or D (3 levels)	W		23	35		17	26	ns	
tPHL				22	33		19	30		
tPLH	Strobe G̅	Y					21	33	ns	
tPHL							22	33		
tPLH	Strobe G̅	W		15.5	24		14	21	ns	
tPHL				21	30		15	23		
tPLH	D0 thru D7	Y					13	20	ns	
tPHL							18	27		
tPLH	E0 thru E15, or D0 thru D7	W		8.5	14		8	14	ns	
tPHL				13	20		8	14		

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS151, SN54LS152, SN74LS151 DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	"C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}$		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25 0.4		0.25 0.35	0.4 0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{Outputs open, All inputs at } 4.5 \text{ V}$	'LS151 'LS152	6.0 5.6	10 9	6.0	10		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS*, SN74LS*			UNIT
				MIN	TYP	MAX	
tPLH	A, B, or C (4 levels)	Y	CL = 15 pF, RL = 2 kΩ, See Note 4		27	43	ns
tPHL					18	30	
tPLH	A, B, or C (3 levels)	W			14	23	ns
tPHL					20	32	
tPLH	Strobe G̅	Y			26	42	ns
tPHL					20	32	
tPLH	Strobe G̅	W			15	24	ns
tPHL					18	30	
tPLH	Any D	Y			20	32	ns
tPHL					16	26	
tPLH	Any D	W			13	21	ns
tPHL					12	20	

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S151, SN74S151 DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S151			SN74S151			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S'	2.5	3.4	V
		SN74S'	2.7	3.4	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			-1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ All inputs at } 4.5 \text{ V},$ All outputs open		45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S151, SN74S151			UNIT
				MIN	TYP	MAX	
tPLH	A, B, or C (4 levels)	Y	CL = 15 pF, RL = 280 Ω, See Note 4	12	12	18	ns
tPHL				12	12	18	
tPLH	A, B, or C (3 levels)	W		10	10	15	ns
tPHL				9	9	13.5	
tPLH	Any D	Y		8	8	12	ns
tPHL				8	8	12	
tPLH	Any D	W		4.5	4.5	7	ns
tPHL				4.5	4.5	7	
tPLH	Strobe G̅	Y		11	11	16.5	ns
tPHL				12	12	18	
tPLH	Strobe G̅	W		9	9	13	ns
tPHL				8.5	8.5	12	

¶ t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

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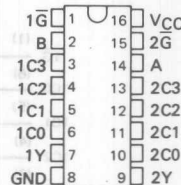
TTL DEVICES

**TYPES SN54153, SN54LS153, SN54S153
SN74153, SN74LS153, SN74S153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

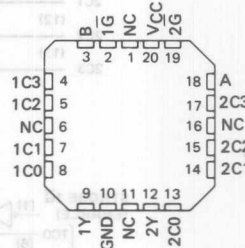
DECEMBER 1972—REVISED DECEMBER 1983

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL Circuits

SN54153, SN54LS153, SN54S153 ... J OR W PACKAGE
SN74153 ... J OR N PACKAGE
SN74LS153, SN74S153 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS153, SN54S153 ... FK PACKAGE
SN74LS153, SN74S153
(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES			TYPICAL POWER DISSIPATION
	FROM DATA	FROM STROBE	FROM SELECT	
'153	14 ns	17 ns	22 ns	180 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT	
B	A	C0	C1	C2	C3	\bar{G}	\bar{Y}	Y
X	X	X	X	X	X	H	L	L
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '153, 'S153	5.5 V
'LS153	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

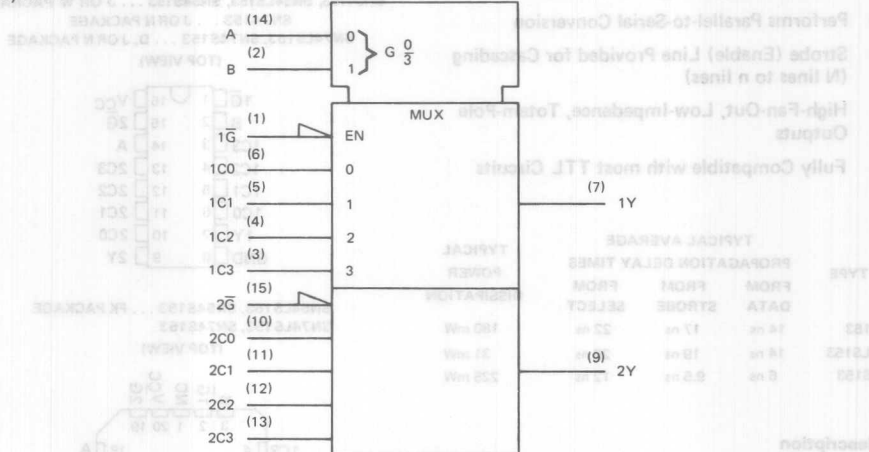
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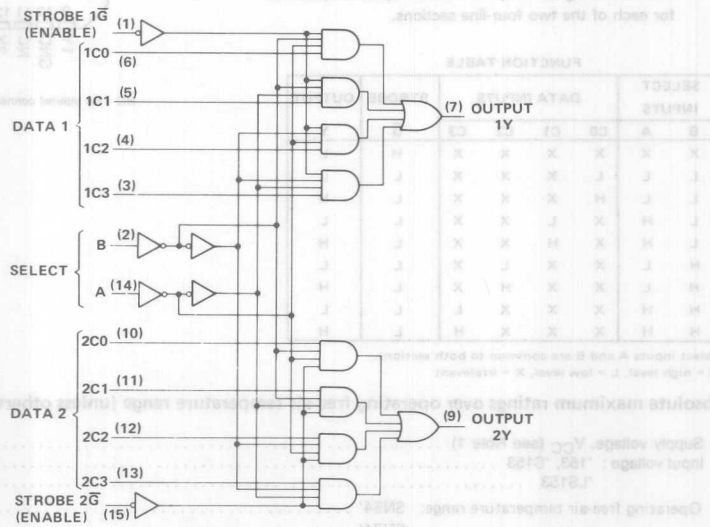
TTL DEVICES

**TYPES SN54153, SN54LS153, SN54S153
SN74153, SN74LS153, SN74S153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

logic symbol



logic diagram



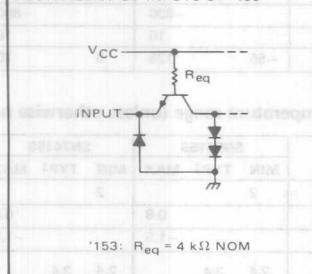
Pin numbers shown on logic notation are for D, J or N packages.

3 TTL DEVICES

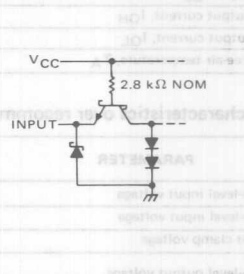
**TYPES SN54153, SN54LS153, SN54S153
SN74153, SN74LS153, SN74S153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

schematics of inputs and outputs

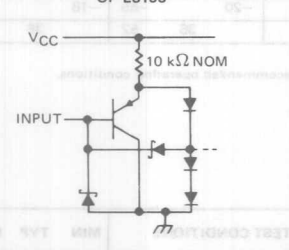
EQUIVALENT OF INPUTS OF '153



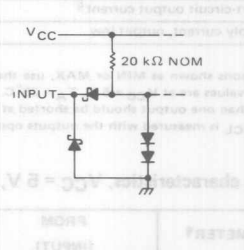
EQUIVALENT OF INPUTS OF 'S153



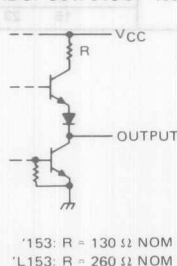
**EQUIVALENT OF 1G, 2G INPUTS
OF LS153**



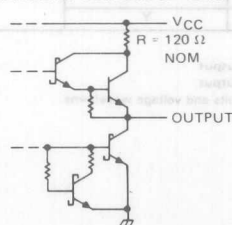
**EQUIVALENT OF ALL OTHER INPUTS
OF 'LS153**



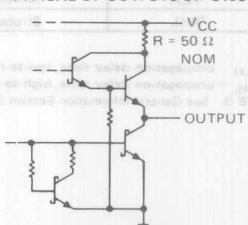
TYPICAL OF OUTPUTS OF '153



TYPICAL OF OUTPUTS OF 'LS153



TYPICAL OF OUTPUTS OF 'S153



**3
TTL DEVICES**

TYPES SN54153, SN74153

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54153			SN74153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54153			SN74153			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-55	-18		-57	mA
I_{CCL} Supply current, output low	$V_{CC} = \text{MAX}, \text{ See Note 2}$		36	52		36	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	$C_L = 30 \text{ pF}, R_L = 400 \Omega,$ See Note 3	12	18		ns
t_{PHL}	Data	Y		15	23		ns
t_{PLH}	Select	Y		22	34		ns
t_{PHL}	Select	Y		22	34		ns
t_{PLH}	Strobe \overline{G}	Y		19	30		ns
t_{PHL}	Strobe \overline{G}	Y		15	23		ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS153, SN74LS153 **DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

recommended operating conditions

	SN54LS153			SN74LS153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS153			SN74LS153			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
						0.35	0.5	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
				-0.4			-0.4	
$I_{OS} §$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.2	10		6.2	10		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER ¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 3	10	15		ns
t_{PHL}	Data	Y		17	26		ns
t_{PLH}	Select	Y		19	29		ns
t_{PHL}	Select	Y		25	38		ns
t_{PLH}	Strobe \overline{G}	Y		16	24		ns
t_{PHL}	Strobe \overline{G}	Y		21	32		ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S153, SN74S153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S153			SN74S153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55	125	0	70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$	0.5			V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CCL} Supply current, low-level output	$V_{CC} = \text{MAX}, \text{ See Note 2}$		45	70	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 3		6	9	ns
t_{PHL}	Data	Y			6	9	ns
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}	Select	Y			12	18	ns
t_{PLH}	Strobe \overline{G}	Y			10	15	ns
t_{PHL}	Strobe \overline{G}	Y			9	13.5	ns

[¶] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54154, SN74154

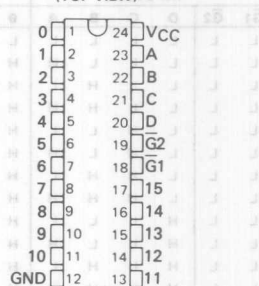
4-LINE TO 16-LINE DECODERS/DEMULPLEXERS

DECEMBER 1972—REVISED DECEMBER 1983

- '154 is Ideal for High-Performance Memory Decoding
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL and MSI Circuits

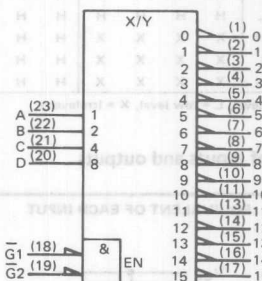
SN54154 ... J OR W PACKAGE
SN74154 ... J OR N PACKAGE

(TOP VIEW)



TYPE	TYPICAL AVERAGE PROPAGATION DELAY		TYPICAL POWER DISSIPATION
	3 LEVELS OF LOGIC	STROBE	
'154	23 ns	19 ns	170 mW

logic symbol

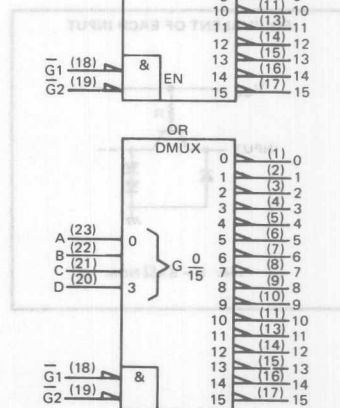


description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

The SN54154 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74154 is characterized for operation from 0°C to 70°C .



Pin numbers shown on logic notation are for J or N packages.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-461

3
TTL DEVICES

TYPES SN54154, SN74154 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1973 • REVISED DECEMBER 1983

FUNCTION TABLE

INPUTS		OUTPUTS															
\bar{G}_1	\bar{G}_2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H

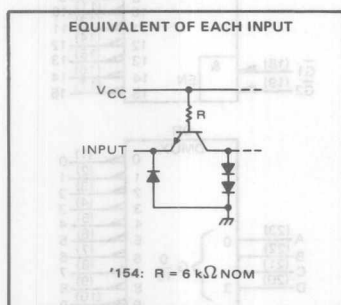
H = high level, L = low level, X = irrelevant

3

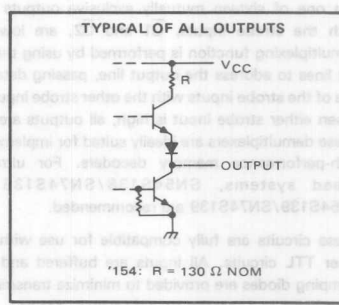
TTL DEVICES

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

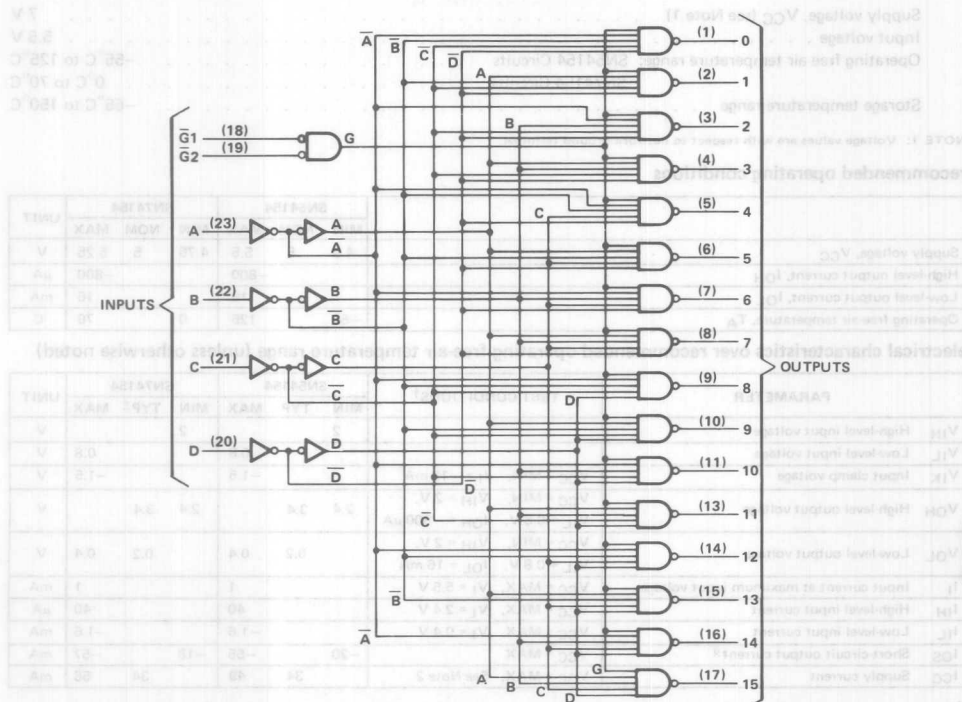


TYPICAL OF ALL OUTPUTS



TYPES SN54154, SN74154 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

logic diagram



Pin numbers shown on logic notation are for J or N packages.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high level output, from A, B, C, or D inputs through 3 levels of logic	$V_{CC} = 5V, T_A = -55^{\circ}C$ See Note 3	34	36	38	ns
Propagation delay time, high-to-low level output, from A, B, C, or D inputs through 3 levels of logic		33	35	37	ns
Propagation delay time, low-to-high level output, from either strobe input		50	58	65	ns
Propagation delay time, high-to-low level output, from either strobe input		48	55	62	ns

NOTE 3: See General Information Section for test inputs and voltage waveforms.

3
TTL DEVICES

TYPES SN54154, SN74154

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54154 Circuits	-55°C to 125°C
SN74154 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54154			SN74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54154			SN74154			UNIT
		MIN	TYP	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-55	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		34	49		34	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 3		24	36	ns
t_{PHL} Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH} Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

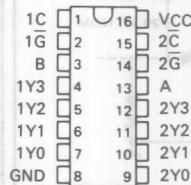
TYPES SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

MARCH 1974—REVISED DECEMBER 1983

- **Applications:**
Dual 2-to-4-Line Decoder
Dual 1-to-4-Line Demultiplexer
3-to-8-Line Decoder
1-to-8-Line Demultiplexer
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
Totem Pole ('155, 'LS155A)
Open-Collector ('156, 'LS156)

SN54155, SN54156, SN54LS155A,
SN54LS156 ... J OR W PACKAGE
SN74155, SN74156 ... J OR N PACKAGE
SN74LS155A, SN74LS156 ... D, J OR N PACKAGE

(TOP VIEW)



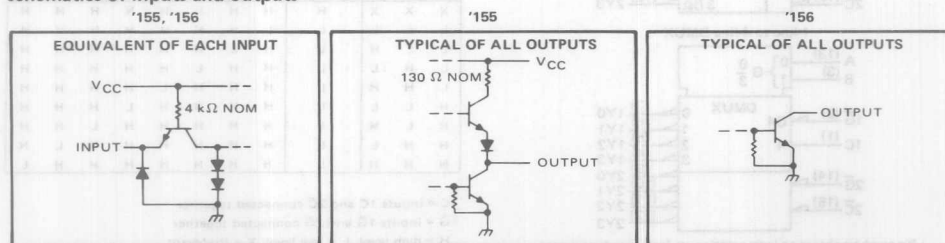
TYPES	TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS	TYPICAL POWER DISSIPATION
'155, '156	21 ns	125 mW
'LS155A	18 ns	31 mW
'LS156	32 ns	31 mW

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

Series 54 and 54LS are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and 74LS are characterized for operation from 0°C to 70°C .

schematics of inputs and outputs



PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-465

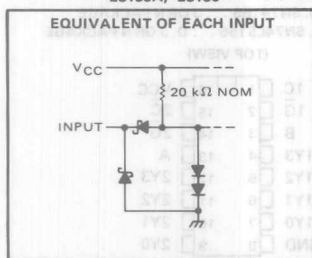
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TTL DEVICES

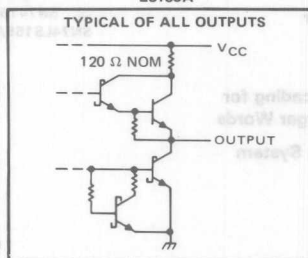
**TYPES SN54155, SN54156, SN54LS155A, SN54LS156,
SN74155, SN74156, SN74LS155A, SN74LS156
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS**

schematics of inputs and outputs (continued)

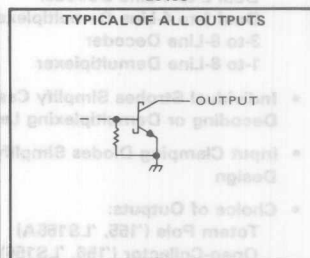
'LS155A, 'LS156



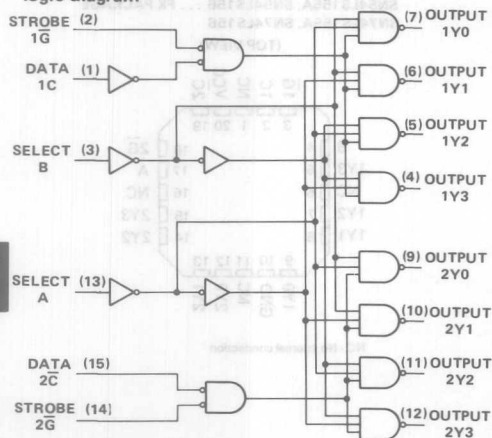
'LS155A



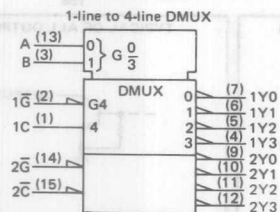
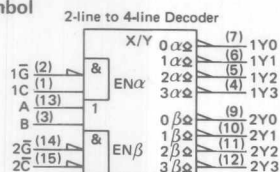
'LS156



logic diagram



logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT	STROBE	DATA		1Y0	1Y1	1Y2	1Y3
B	A	1C					
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT	STROBE	DATA		2Y0	2Y1	2Y2	2Y3
B	A	2C					
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT	STROBE	OR DATA		(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together

‡G = inputs 1G and 2G connected together

H = high level, L = low level, X = irrelevant

3

TTL DEVICES

**TYPES SN54155, SN54156, SN54LS155A, SN54LS156,
SN74155, SN74156, SN74LS155A, SN74LS156
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '155, '156	5.5 V
'LS155A, 'LS156	7 V
Off-state output voltage: '155	5.5 V
'LS156	7 V
Operating free-air temperature range: SN54', SN54LS' Circuits	-55°C to 125°C
SN74', SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54155 SN74155		UNIT	
		MIN	TYP‡		MAX
V _{IH} High-level input voltage		2		V	
V _{IL} Low-level input voltage			0.8	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = −8 mA		−1.5	V	
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = −800 μA	2.4	3.4	V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.4 V			40	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			−1.6	mA
I _{OS} Short-circuit output current §	V _{CC} = MAX	SN54155 SN74155	−20 −18	−55 −57	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	SN54155 SN74155	25 40	35	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3	13		20	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54156, SN74156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54156 SN74156		UNIT	
		MIN	TYP‡ MAX		
V_{IH} High-level input voltage		2		V	
V_{IL} Low-level input voltage			0.8	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$		-1.5	V	
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$		250	μA	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6	mA	
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54156 SN74156	25 25	35 40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNI
tPLH	A, B, 2C, 1G, or 2G	Y	2	CL = 15 pF, RL = 400 Ω, See Note 3	15	23	ns	
tPHL	A, B, 2C, 1G, or 2G	Y	2		20	30	ns	
tPLH	A or B	Y	3		23	34	ns	
tPHL	A or B	Y	3		23	34	ns	
tPLH	1C	Y	3		18	27	ns	
tPHL	1C	Y	3		22	33	ns	

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS155A, SN74LS155A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54LS155A			SN74LS155A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS155A			SN74LS155A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155A SN74LS155A			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 3		10	15	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			19	30	ns
t_{PLH}	A or B	Y	3			17	26	ns
t_{PHL}	A or B	Y	3			19	30	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			18	27	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS156, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

	SN54LS156			SN74LS156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS156			SN74LS156			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage								V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.1		10	6.1		10	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS156 SN74LS156			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C 1G, or 2G	Y	2	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 3		25	40	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			34	51	ns
t_{PLH}	A or B	Y	3			31	46	ns
t_{PHL}	A or B	Y	3			34	51	ns
t_{PLH}	1C	Y	3			32	48	ns
t_{PHL}	1C	Y	3			32	48	ns

[¶] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158 QUADRUPL 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

MARCH 1974—REVISED DECEMBER 1983

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE \bar{G}	SELECT \bar{A}/B	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

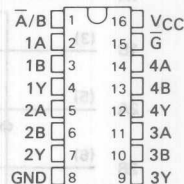
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

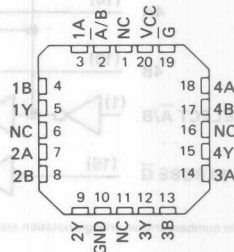
Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '157, 'L157, 'S158	5.5 V
'LS157, 'LS158	7 V
Operating free-air temperature range: SN54'	–55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54157, SN54LS157, SN54S157,
SN54LS158, SN54S158 ... J OR W PACKAGE
SN54L157 ... J PACKAGE
SN74157 ... J OR N PACKAGE
SN74LS157, SN74S157,
SN74LS158, SN74S158 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS157, SN54S157, SN54LS158
SN54S158, SN74LS157, SN74S157,
SN74LS158, SN74S158 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

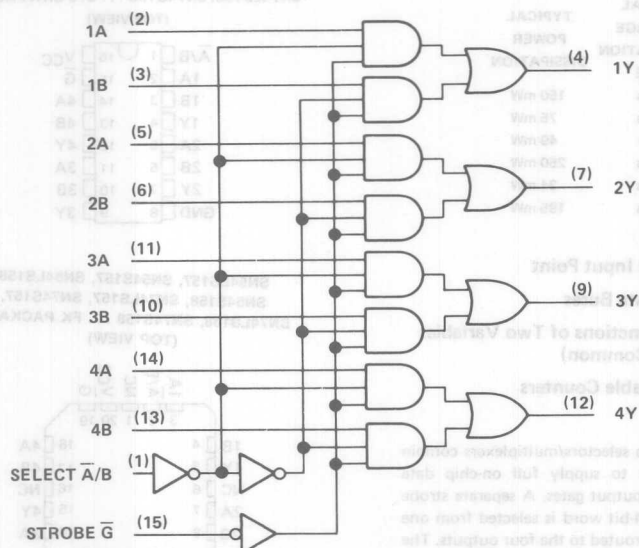
PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54157, SN54L157, SN74157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

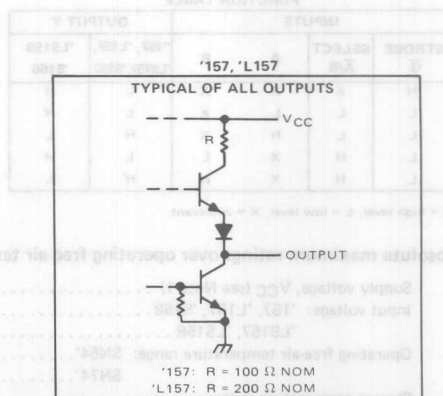
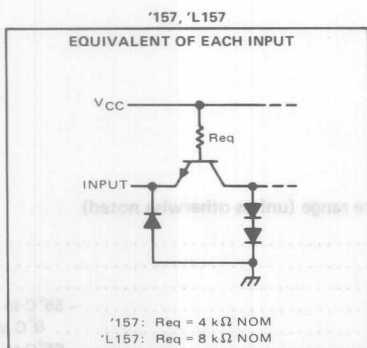
logic diagram

'157, 'L157



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



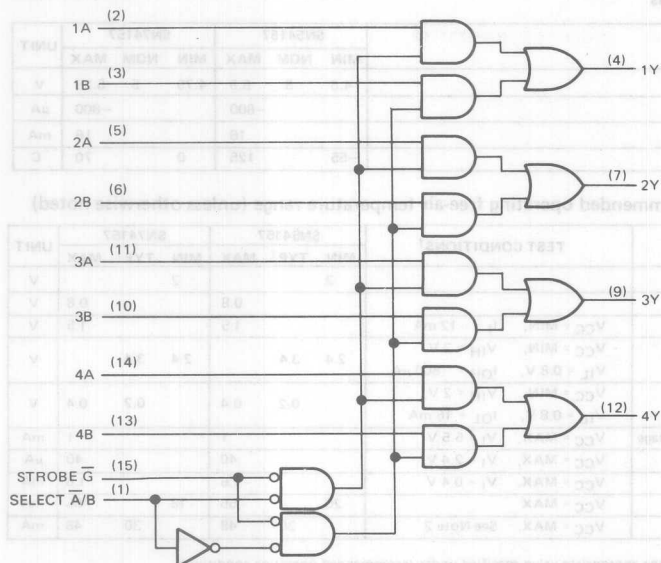
3

TTL DEVICES

**TYPES SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

logic diagrams

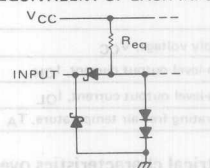
'LS157, 'S157



schematics of inputs and outputs

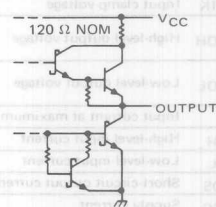
'LS157, 'LS158

EQUIVALENT OF EACH INPUT

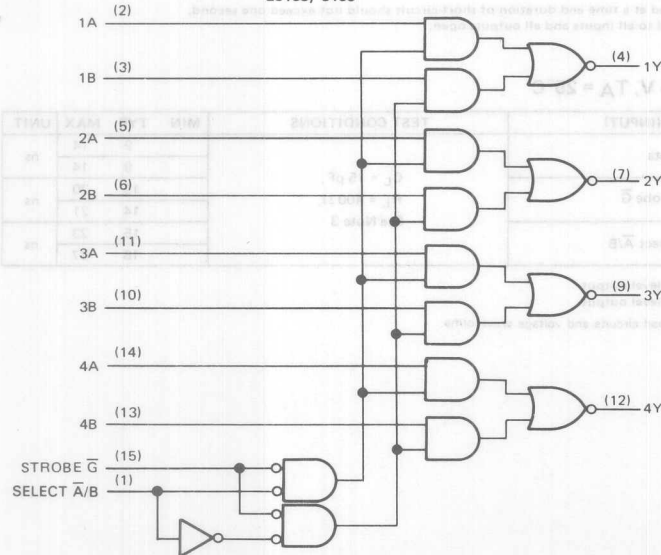


S or G inputs: $R_{eq} = 8.5 \text{ k}\Omega \text{ NOM}$
A or B inputs: $R_{eq} = 17 \text{ k}\Omega \text{ NOM}$

TYPICAL OF ALL OUTPUTS

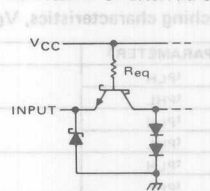


'LS158, 'S158



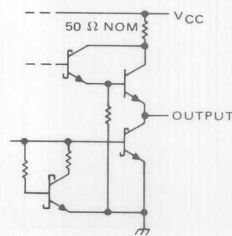
'S157, 'S158

EQUIVALENT OF EACH INPUT



S or G inputs: $R_{eq} = 1.4 \text{ k}\Omega \text{ NOM}$
A or B inputs: $R_{eq} = 2.8 \text{ k}\Omega \text{ NOM}$

TYPICAL OF ALL OUTPUTS



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54157, SN74157

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55	125	0	70			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54157			SN74157			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			1.5			1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	30	48		30	48		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER ¹	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3	9	14	ns	
t_{PHL}			9	14		
t_{PLH}	Strobe \overline{G}		13	20	ns	
t_{PHL}			14	21		
t_{PLH}	Select $\overline{A/B}$		15	23	ns	
t_{PHL}			18	27		

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPE SN54L157 QUADRUPL 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
I_{OH} High-level output current			-400	μ A
I_{OL} Low-level output current			8	mA
T_A Operating free-air temperature	-55		125	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-9		-28	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		15	24	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	$C_L = 15 \text{ pF},$ $R_L = 800 \Omega,$ See Note 3	18	28		ns
t_{PHL}			18	28		
t_{PLH}	Strobe \overline{G}		26	40		ns
t_{PHL}			28	42		
t_{PLH}	Select $\overline{A/B}$		30	46		ns
t_{PHL}			36	54		

[¶] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS157, SN54LS158, SN74LS157, SN74LS158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-400			-400	μA
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage					2			2			V
V _{IL}	Low-level input voltage							0.7			0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA					-1.5			-1.5	V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -400 μA			2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 4 mA, I _{OL} = 8 mA				0.25	0.4		0.25	0.4	V
I _I	Input current at maximum input voltage	A/B or \bar{G} A or B	V _{CC} = MAX, V _I = 7 V					0.2			0.2	mA
I _{IH}	High-level input current	A/B or \bar{G} A or B	V _{CC} = MAX, V _I = 2.7 V					40			40	μA
I _{IL}	Low-level input current	A/B or \bar{G} A or B	V _{CC} = MAX, V _I = 0.4 V					-0.8			-0.8	mA
I _{OS}	Short-circuit output current§		V _{CC} = MAX			-20		-100	-20		-100	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 2	'LS157		9.7	16		9.7	16		mA
				'LS158		4.8	8		4.8	8		
			V _{CC} = MAX, All A inputs at 4.5 V, All other inputs at 0 V	'LS158		6.5	11		6.5	11		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER ¶	FROM (INPUT)	TEST CONDITIONS	'LS157			'LS158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Data	C _L = 15 pF, R _L = 2 kΩ, See Note 3	9	14		7	12		ns
t _{PHL}			9	14		10	15		
t _{PLH}	Strobe \overline{G}		13	20		11	17		ns
t _{PHL}			14	21		18	24		
t _{PLH}	Select $\overline{A/B}$		15	23		13	20		ns
t _{PHL}			18	27		16	24		

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S157, SN54S158, SN74S157, SN74S158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.8			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$		-1.2			-1.2		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -1 \text{ mA}$	Series 54S 2.5	3.4		Series 74S 2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$		0.5			0.5		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		1			1		mA
I_{IH} High-level input current	\bar{A}/B or \bar{G}		100			100		μA
	A or B		50			50		
I_{IL} Low-level input current	\bar{A}/B or \bar{G}		-4			-4		mA
	A or B		-2			-2		
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40	-100		-40	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, All inputs at 4.5 V, See Note 2	50	78		39	61		mA
	$V_{CC} = \text{MAX}$, A inputs at 4.5 V, B,G,S, inputs at 0 V, See Note 2					81		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Note 2: I_{CC} is measured with all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	Data	CL = 15 pF, RL = 280 Ω, See Note 3	5 7.5			4 6			ns
tPHL			4.5 6.5			4 6			
tPLH	8.5 12.5			6.5 11.5			ns		
tPHL	7.5 12			7 12					
tPLH	Select A/B		9.5 15			8 12			ns
tPHL			9.5 15			8 12			

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

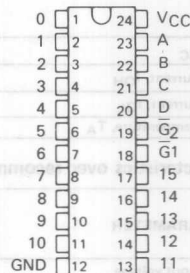
NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54159, SN74159 4-LINE TO 16-LINE DECODERS/DEMULPLEXERS WITH OPEN-COLLECTOR OUTPUTS DECEMBER 1972—REVISED DECEMBER 1983

- Open-Collector Outputs for Interfacing with MOS or Memory Decoders/Drivers
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data from One Input Line to Any One of 16 Outputs
- Typical Average Propagation Delay Times:
24 ns through 3 levels of Logic
19 ns from Strobe Input
- Output Off-State Current is Less Than 50 μ A
- Fully Compatible with Most TTL, and MSI Circuits

SN54159 J OR W PACKAGE
SN74159 J OR N PACKAGE

(TOP VIEW)



description

Each of these monolithic, 4-line-to-16 line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive open-collector outputs when both the strobe inputs, \bar{G}_1 and \bar{G}_2 , are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing MOS memory decoding or for interfacing with discrete memory address drivers. For ultra-high-speed applications, the SN54S138/SN74S138 or SN54S139/SN74S139 is recommended.

These circuits are fully compatible for use with most other TTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54159 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74159 is characterized for operation from 0°C to 70°C .

function table

Same as SN54154, SN74154.

logic diagram

Same as SN54154, SN74154.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54159 Circuits	-55°C to 125°C
SN74159 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54159, SN74159 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54159			SN74159			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 5.5 \text{ V}$			50	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, All inputs grounded		34	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

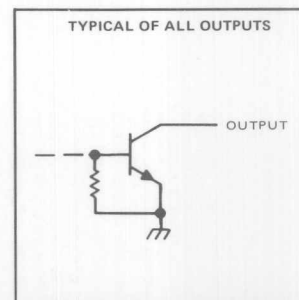
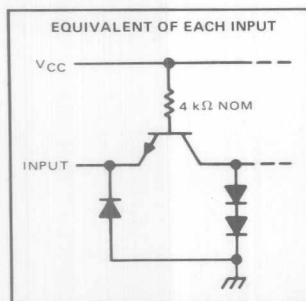
‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	$C_L = 15 \text{ pF}, \quad R_L = 400 \, \Omega, \quad \text{See Note 2}$		23	36	ns	
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			24	36	ns	
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			15	25	ns	
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			22	36	ns	

NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



4-LINE TO 16-LINE DECODER/MULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS TYPES SN54156, SN74156

recommended operating conditions

PARAMETER	SN54156		SN74156	
	MIN	MAX	MIN	MAX
Supply voltage, V_{CC}	4.5	5.5	4.5	5.5
Low-level input current, I_{IL}	10	10	10	10
Operating free-air temperature, T_A	0	70	0	70

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹		UNIT
	MIN	MAX	
V_{IH} High-level input voltage	2	5	V
V_{IL} Low-level input voltage	0.5	1	V
V_{IC} Input clamp voltage	1.5	1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2.5$ $V_{CC} = \text{MIN}$, $V_{IH} = 2.5$	10	mA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 10$ mA $V_{CC} = \text{MAX}$, $I_{OL} = 10$ mA	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5$ V	10	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.5$ V	10	mA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5$ V	10	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, No inputs switched	20	mA

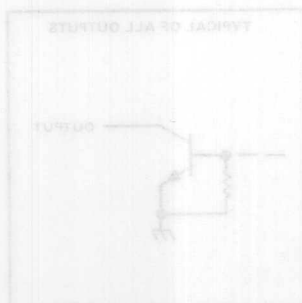
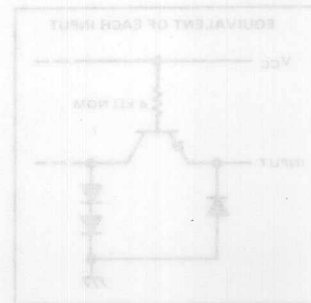
¹Test conditions shown as MIN or MAX; use the appropriate value specified unless otherwise noted. For the SN54156, $V_{CC} = 5.5$ V, $T_A = 25^\circ\text{C}$. For the SN74156, $V_{CC} = 5.5$ V, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		UNIT
	MIN	MAX	
t_{PLH} Propagation delay time, low-to-high level output from A, B, C, or D inputs through 3 levels of logic	20	30	ns
t_{PHL} Propagation delay time, high-to-low level output from A, B, C, or D inputs through 3 levels of logic	20	30	ns
t_{PLH} Propagation delay time, low-to-high level output from either strobe input	15	20	ns
t_{PHL} Propagation delay time, high-to-low level output from either strobe input	20	25	ns

NOTE 2: See Detailed Information Section for load circuit and voltage waveform.

schematic of inputs and outputs



3 TTL DEVICES

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

OCTOBER 1976—REVISED DECEMBER 1983

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

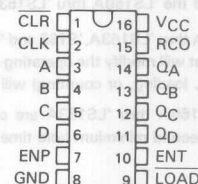
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE

SERIES 74' . . . J OR N PACKAGE

SERIES 74LS', 74S' . . . D, J OR N PACKAGE

(TOP VIEW)

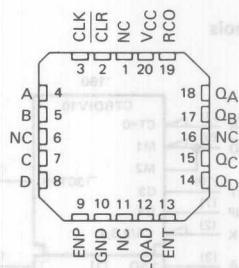


NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE

SERIES 74LS', 74S' . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

TYPE	TYPICAL TIME, CLOCK TO Q OUTPUT	MAXIMUM FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-481

3

TTL DEVICES

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

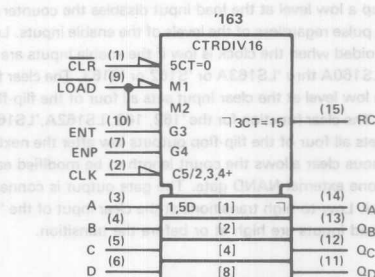
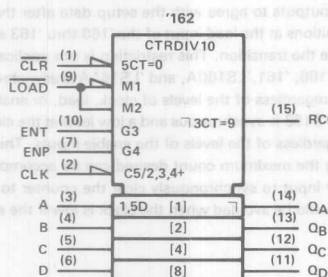
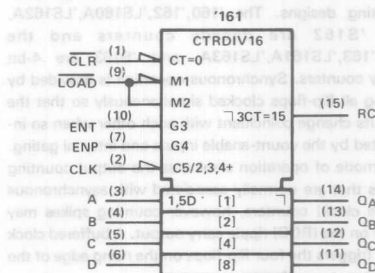
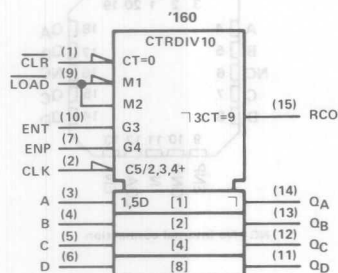
'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL}.

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A or 'S163 will count in binary. Virtually any count mode (modulo-N, N₁-to-N₂, N₁-to-maximum) can be used with this fast look-ahead circuit.

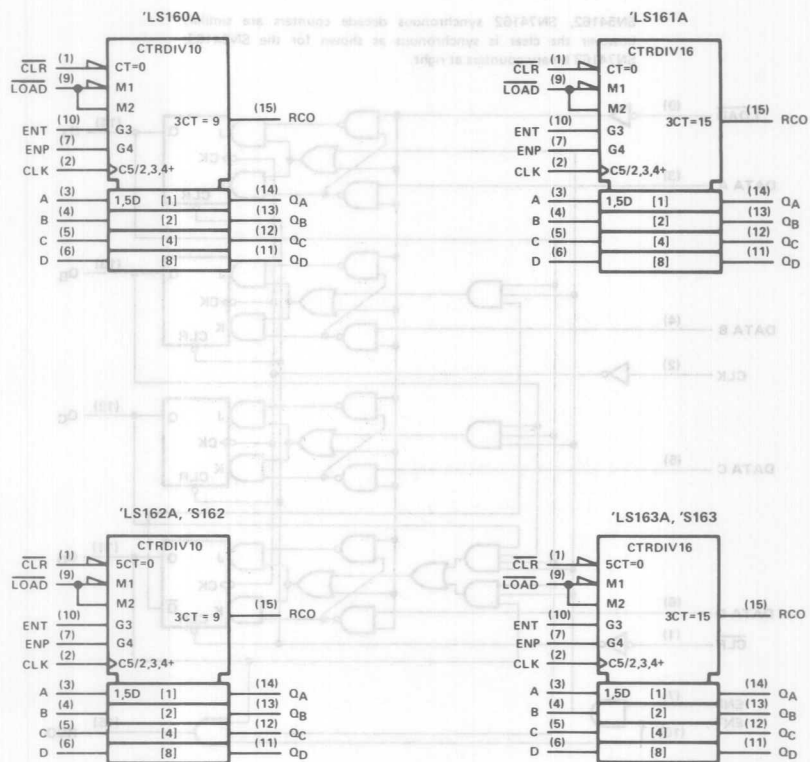
logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54LS160A THRU SN54LS163A, SN54S162, SN54S163,
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS

logic symbols (continued)



Pin numbers shown on logic notation are for D, J or N packages.

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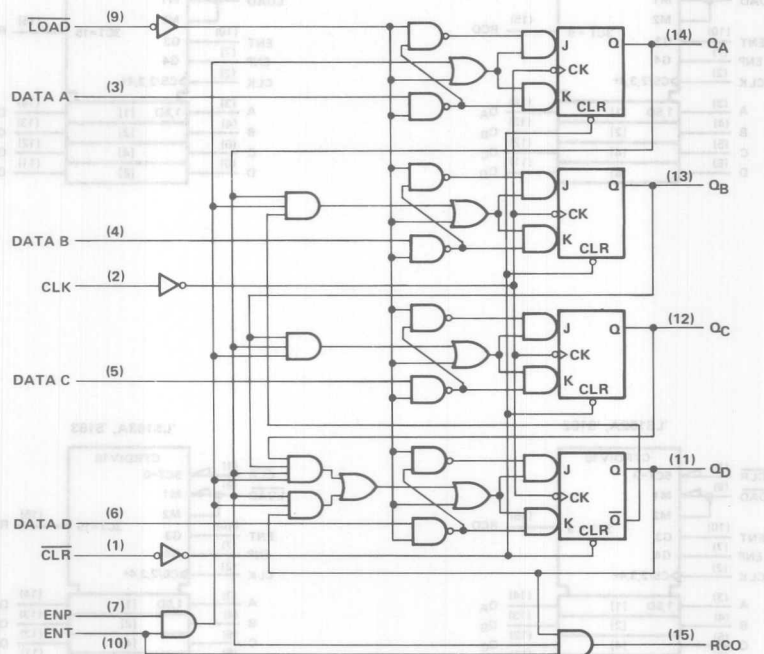
TTL DEVICES

SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS 4-BIT COUNTERS

logic diagram

SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



Pin numbers shown on logic notation are for D, J or N packages.

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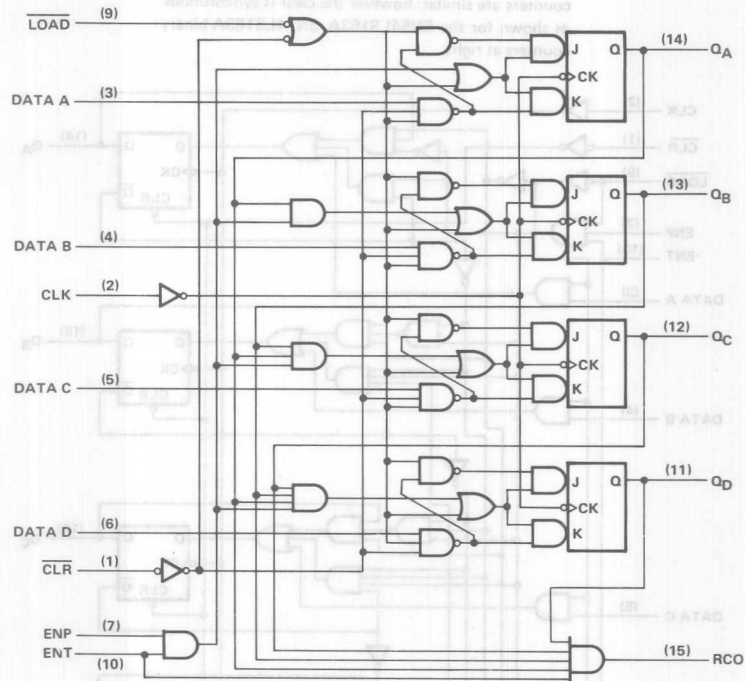
TTL DEVICES

SN54161, SN54163, SN74161, SN74163 SYNCHRONOUS 4-BIT COUNTERS

logic diagram

SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



Pin numbers shown on logic notation are for D, J or N packages.

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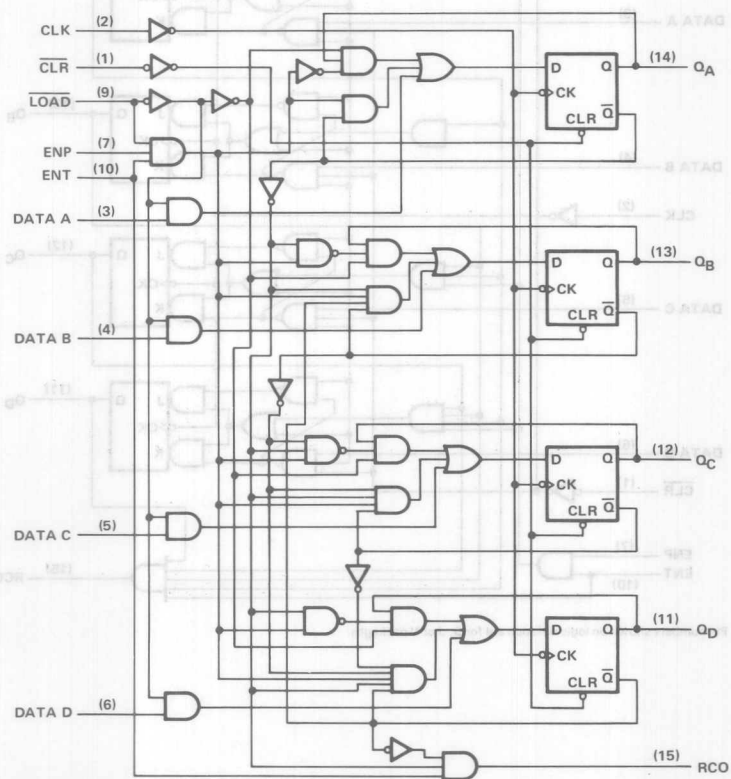
TTL DEVICES

SN54LS160A, SN54LS162A, SN74LS160A, SN74LS162A SYNCHRONOUS 4-BIT COUNTERS

logic diagram

SN54LS160A, SN74LS160A SYNCHRONOUS DECADE COUNTERS

SN54LS162A, SN74LS162A synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163A, SN74LS163A binary counters at right.



Pin numbers shown on logic notation are for D, J or N packages.

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TTL DEVICES

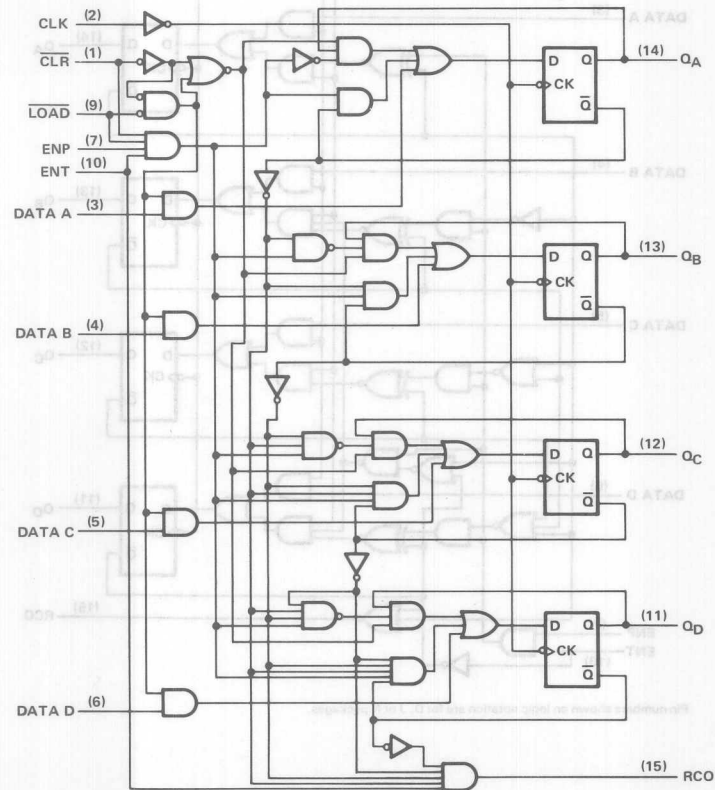
SN54LS161A, SN54LS163A, SN74LS161A, SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

logic diagram

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SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



Pin numbers shown on logic notation are for D, J or N packages.

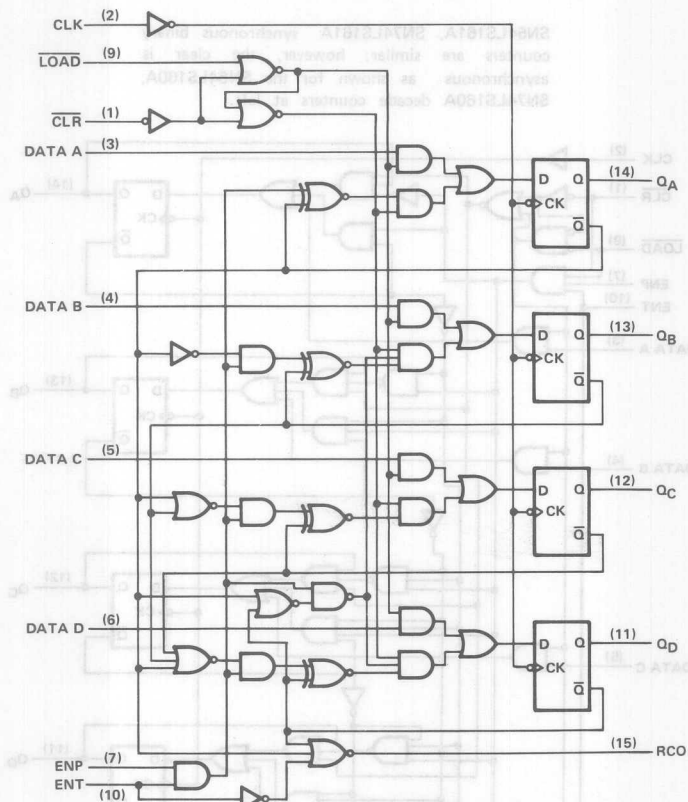
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TTL DEVICES

SN54S162, SN74S162 SYNCHRONOUS 4-BIT COUNTERS

logic diagram

SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTER



Pin numbers shown on logic notation are for D, J or N packages.

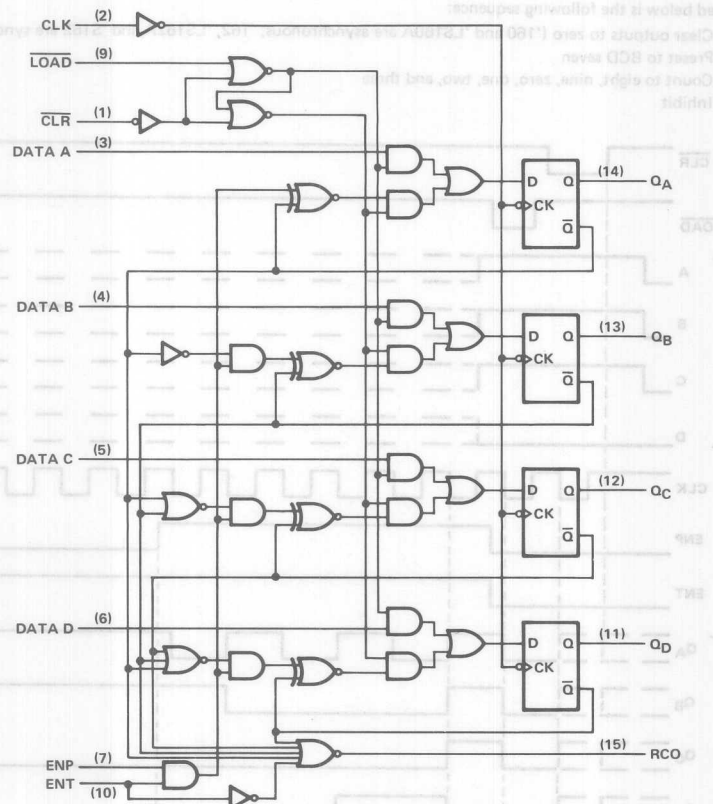
3

TTL DEVICES

SN54S163, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

logic diagram

SN54S163, SN74S163 SYNCHRONOUS DECADE COUNTER



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

**TYPES SN54160, SN54162, SN54LS160A, SN54LS162A, SN54S162,
SN74160, SN74162, SN74LS160A, SN74LS162A, SN74S162
SYNCHRONOUS 4-BIT COUNTERS**

'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

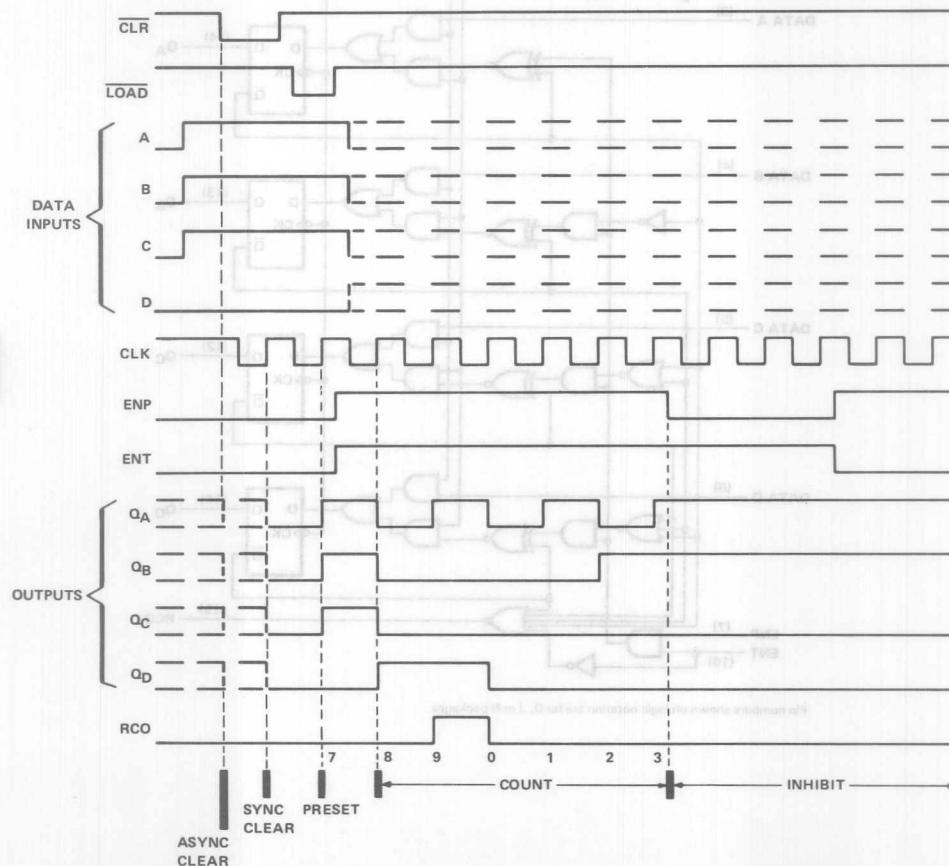
typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A, and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

3

TTL DEVICES



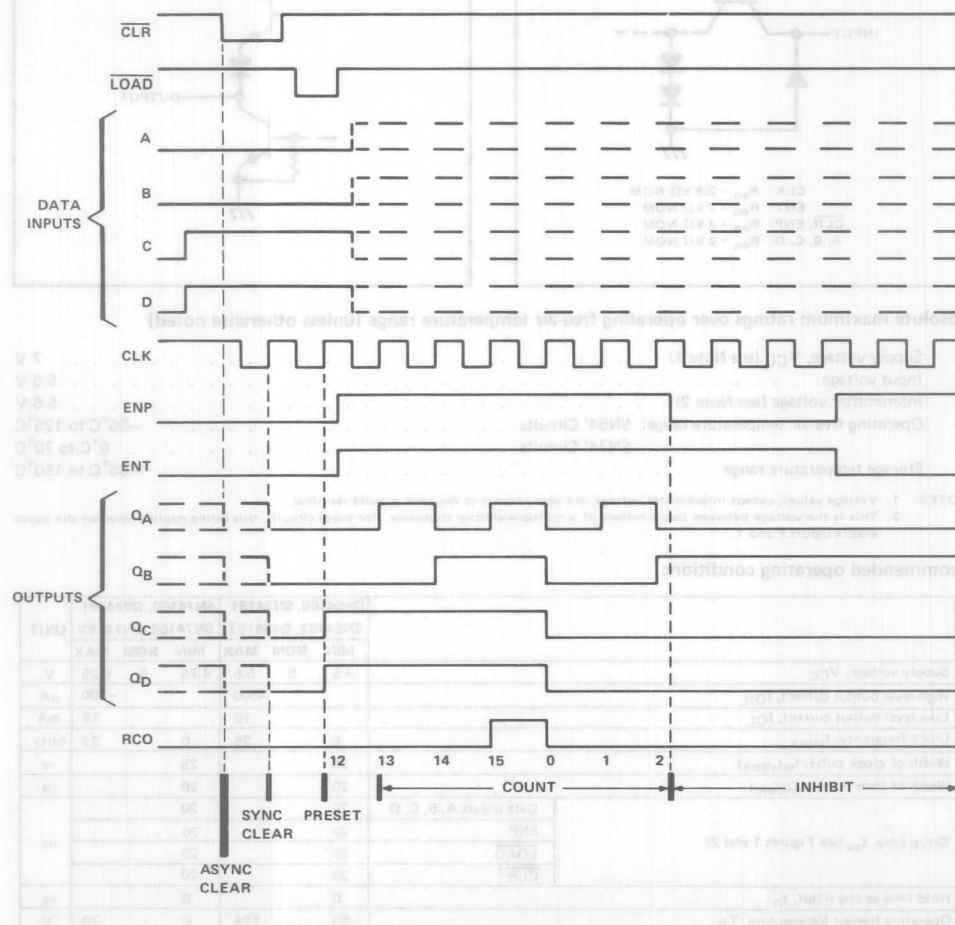
TYPES SN54161, SN54163, SN54LS161A, SN54LS163A, SN54S163,
SN74161, SN74163, SN74LS161A, SN74LS163A, SN74S163
SYNCHRONOUS 4-BIT COUNTERS

'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit

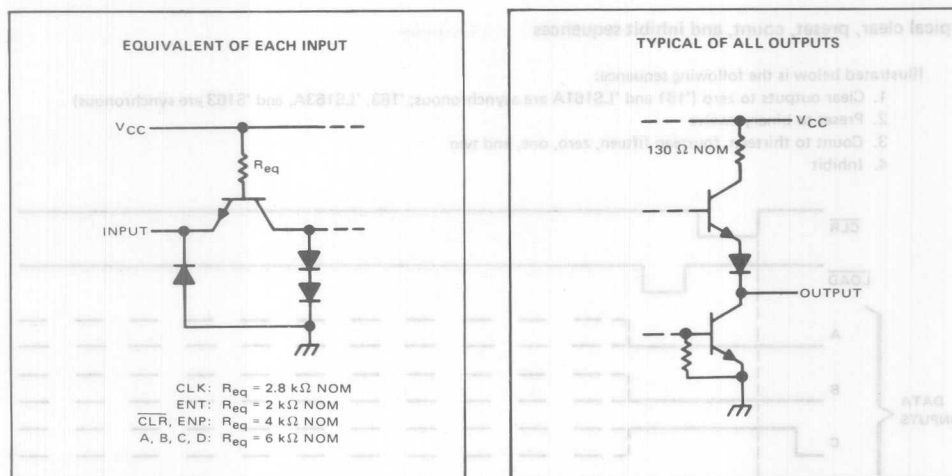


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TTL DEVICES

SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

			SN54160, SN54161			SN74160, SN74161			UNIT
			SN54162, SN54163			SN74162, SN74163			
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					-800			-800	μ A
Low-level output current, I_{OL}					16			16	mA
Clock frequency, f_{clock}			0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$			25			25			ns
Width of clear pulse, $t_{w(clear)}$			20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D		20			20			ns
	ENP		20			20			
	LOAD		25			25			
	CLR ¹		20			20			
Hold time at any input, t_h			0			0			ns
Operating free-air temperature, T_A			-55		125	0		70	°C

† This applies only for '162 and '163, which have synchronous clear inputs.

SN54160 THRU SN54163, SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	CLK or ENT		80			80		µA
	Other inputs		40			40		µA
I _{IL} Low-level input current	CLK or ENT		-3.2			-3.2		mA
	Other inputs		-1.6			-1.6		mA
I _{OS} Short-circuit output current §	V _{CC} = MAX	-20	-57		-18	-57		mA
I _{CCH} Supply current, all outputs high	V _{CC} = MAX, See Note 3		59	85		59	94	mA
I _{CCL} Supply current, all outputs low	V _{CC} = MAX, See Note 4		63	91		63	101	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
t _{PLH}	CLK	RCO	C _L = 15 pF, R _L = 400 Ω, See Figures 1 and 2 and Note 5		23	35	ns
t _{PHL}		Q			23	35	ns
t _{PLH}	CLK (LOAD input high)	Any			13	20	ns
t _{PHL}		Q			15	23	ns
t _{PLH}	CLK (LOAD input low)	Any			17	25	ns
t _{PHL}		Q			19	29	ns
t _{PLH}	ENT	RCO			11	16	ns
t _{PHL}		Q			11	16	ns
t _{PHL}	CLR	Any Q			26	38	ns

¶f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

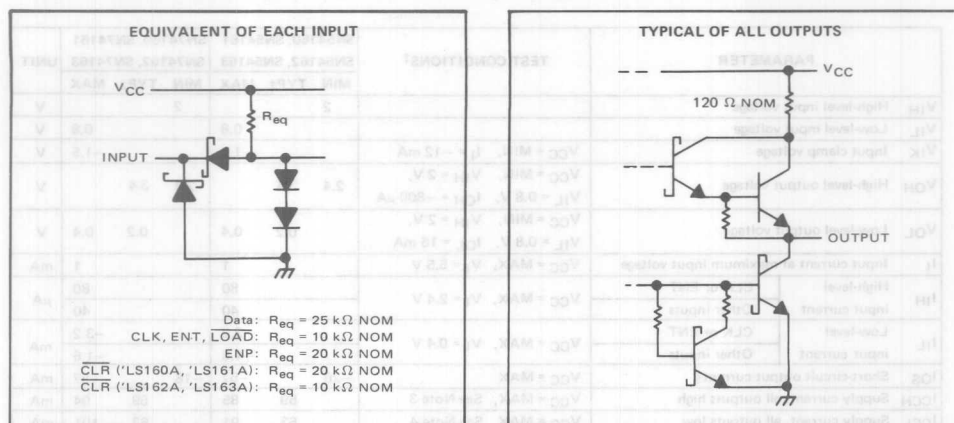
NOTE 5: Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

3

TTL DEVICES

SN54LS160A THRU SN54LS163A, SN74LS160A THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7)	7 V
Input voltage	7 V
Operating free-air temperature: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS*			SN74LS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			− 400			− 400	μA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		25	0		25	MHz
t _{w(clock)}	Width of clock pulse	25			25			ns
t _{w(clear)}	Width of clear pulse	20			20			ns
t _{su}	Setup time, (see Figures 1 and 2)	Data inputs A, B, C, D	20		20			ns
		ENP or ENT	20		20			
		LOAD	20		20			
		LOAD inactive state	20		20			
		CLR†	20		20			
	CLR inactive state	25		25				
t _h	Hold time at any input	9			3			ns
T _A	Operating free-air temperature	− 55		125	0		70	°C

[†] This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

3

TTL DEVICES

SN54LS160A THRU SN54LS163A, SN74LS160A THRU SN74LS163A SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 4 mA, I _{OL} = 8 mA		0.25	0.4		0.25	0.4	V
I _I	Input current at maximum input voltage	Data or ENP			0.1			0.1	mA
		LOAD, CLK, or ENT			0.2			0.2	
		CLR ('LS160A, 'LS161A)			0.1			0.1	
		CLR ('LS162A, 'LS163A)			0.2			0.2	
I _{IH}	High-level input current	Data or ENP			20			20	µA
		LOAD, CLK, or ENT			40			40	
		CLR ('LS160A, 'LS161A)			20			20	
		CLR ('LS162A, 'LS163A)			40			40	
I _{IL}	Low-level input current	Data or ENP			-0.4			-0.4	mA
		LOAD, CLK, or ENT			-0.8			-0.8	
		CLR ('LS160A, 'LS161A)			-0.4			-0.4	
		CLR ('LS162A, 'LS163A)			-0.8			-0.8	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CCCH}	Supply current, all outputs high	V _{CC} = MAX, See Note 3	18	31		18	31		mA
I _{CCCL}	Supply current, all outputs low	V _{CC} = MAX, See Note 4	19	32		19	32		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
t _{PLH}	CLK	RCO	C _L = 15 pF, R _L = 2 kΩ, See figures 1 and 2 and Note 8		20	35	ns
t _{PHL}					18	35	
t _{PLH}	CLK	Any			13	24	ns
t _{PHL}	(LOAD input high)	Q			18	27	
t _{PLH}	CLK	Any			13	24	ns
t _{PHL}	(LOAD input low)	Q			18	27	
t _{PLH}	ENT	RCO			9	14	ns
t _{PHL}					9	14	
t _{PHL}	CLR	Any Q			20	28	ns

‡ f_{max} = Maximum clock frequency

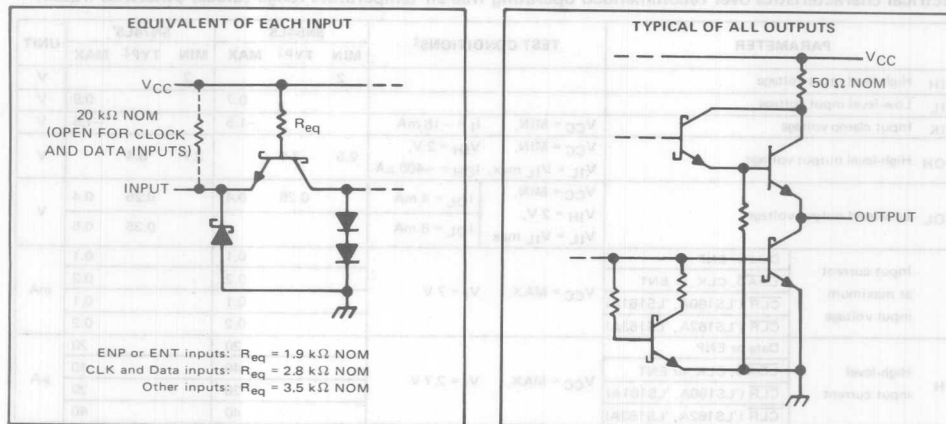
t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 8: Propagation delay for clearing is measured from the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.

SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10)	-55°C to 125°C
SN74S162, SN74S163	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54S162, SN54S163			SN74S162, SN74S163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low)		10			10			ns
Width of clear pulse, $t_{w(clear)}$		10			10			ns
Setup time, t_{su} (see Figure 4)	Data inputs, A, B, C, D	4			4			ns
	ENP or ENT	12			12			
	LOAD	14			14			
	CLR	14			14			
	LOAD inactive-state	12			12			
Release time, $t_{release}$ (see Figure 4)	ENP or ENT			4			4	ns
	Data inputs A, B, C, D	3			3			
Hold time, t_h (see Figure 4)	LOAD	0			0			ns
	CLR	0			0			
Operating free-air temperature, T_A (see Note 10)		-55		125	0		70	°C

- NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
10. An SN54S162 or SN54S163 in the W package operating at free air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S162 SN54S163			SN74S162 SN74S163			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage			0.8			0.8		V
V _{IF} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.2			-1.2		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA		0.5			0.5		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	CLK and data inputs		50			50		μA
	Other inputs	-10	-200		-10	-200		
I _{IL} Low-level input current	ENT		-4			4		mA
	Other inputs		2			2		
I _{OS} Short-circuit output current §	V _{CC} = MAX	-40	-100		-40	100		mA
I _{CC} Supply current	V _{CC} = MAX	95	160		95	160		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				40	70		MHz
t _{PLH}	CLK	RCO	C _L = 15 pF, R _L = 280 Ω, See Figures 1, 3, and 4		14	25	ns
t _{PHL}		RCO			17	25	
t _{PLH}	CLK	Any Q			8	15	ns
t _{PHL}		Any Q			10	15	
t _{PLH}	ENT	RCO			10	15	ns
t _{PHL}		RCO			10	15	

¶f_{max} ≡ maximum clock frequency

t_{PLH} ≡ propagation delay time, low to high-level output

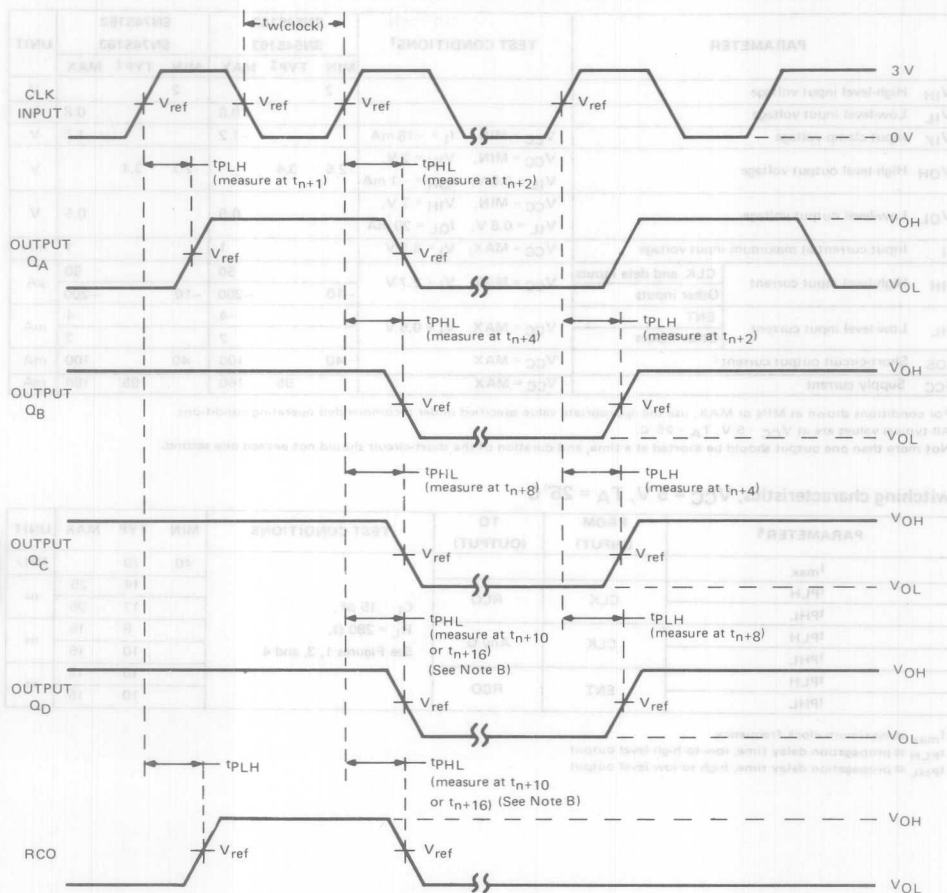
t_{PHL} ≡ propagation delay time, high to low-level output

3

TTL DEVICES

**SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS**

PARAMETER MEASUREMENT INFORMATION

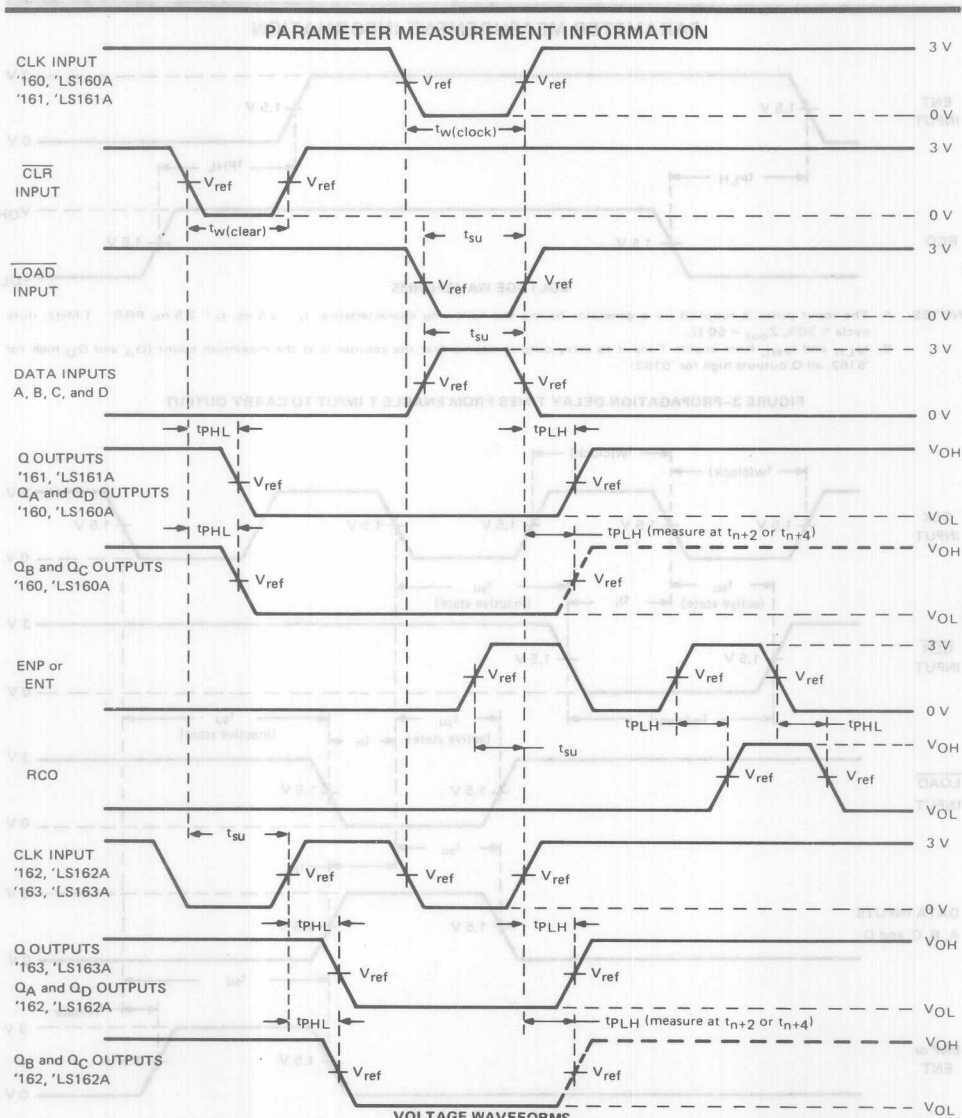


VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$; for 'LS160A thru 'LS163A, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$; and for 'S162, 'S163, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$. Vary PRR to measure t_{max} .
- B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.
- C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5 \text{ V}$; for 'LS160A thru 'LS163A, $V_{ref} = 1.3 \text{ V}$.

FIGURE 1—SWITCHING TIMES

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN74160 THRU SN74163, SN74LS160A, THRU SN74LS163A
SYNCHRONOUS 4-BIT COUNTERS

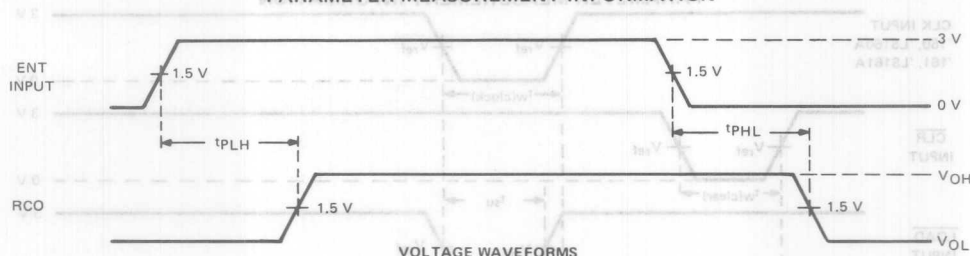


NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle $\sim 50\%$, $Z_{out} \approx 50 \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. Enable P and enable T setup times are measured at t_{n+0} .
C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 2—SWITCHING TIMES

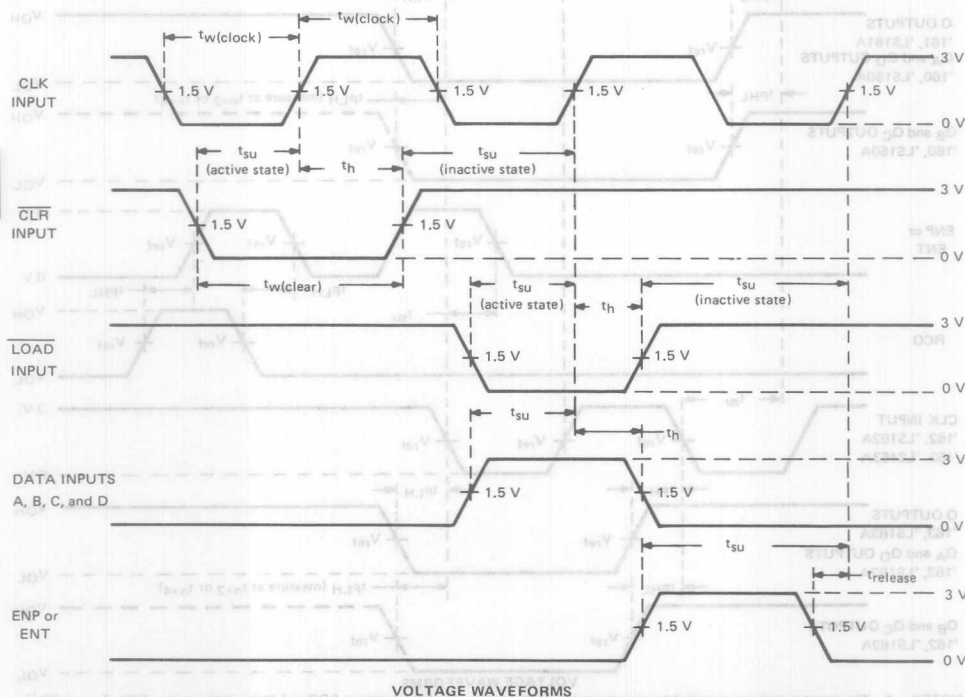
TYPES SN54S162, SN54S163, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$.
B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3—PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$.

FIGURE 4—PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS



$$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH}) (N-2) + (\text{ENT } t_{SU})$$

**TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS**

TYPICAL APPLICATION DATA

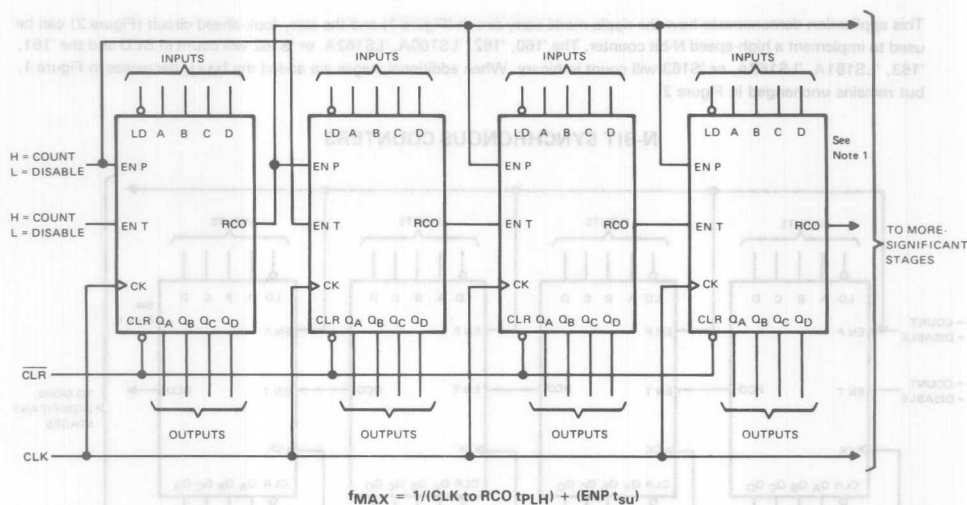


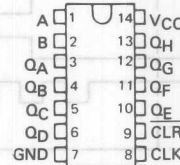
FIGURE 2

TYPES SN54164, SN74LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

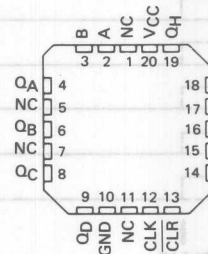
MARCH 1974—REVISED DECEMBER 1983

- Gated Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

SN54164, SN54LS164 ... J OR W PACKAGE
SN74164 ... J OR N PACKAGE
SN74LS164 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS164 ... FK PACKAGE
SN74LS164
(TOP VIEW)



NC — No internal connection

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74164 and SN74LS164 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS				OUTPUTS			
CLR	CLOCK	A	B	QA	QB	...	QH
L	X	X	X	L	L	...	L
H	L	X	X	QA0	QB0	...	QH0
H	↑	H	H	HA	HB	...	Hn
H	↑	L	X	LA	LB	...	Ln
H	↑	X	L	LA	LB	...	Ln

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

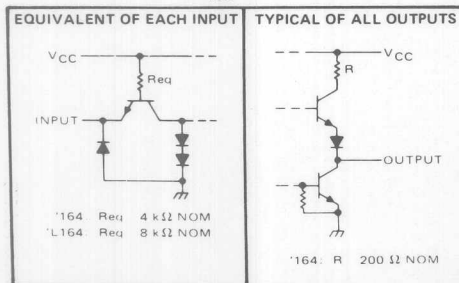
↑ = transition from low to high level.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

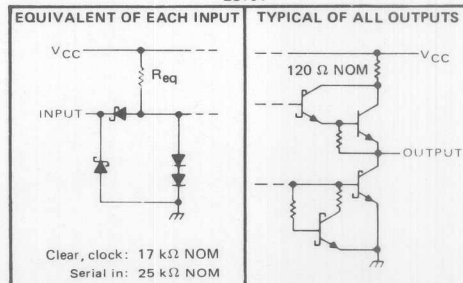
HA, HB, Hn = the level of QA or QB before the most-recent ↑ transition of the clock; indicates a one-bit shift.

schematics of inputs and outputs

'164



'LS164



PRODUCTION DATA

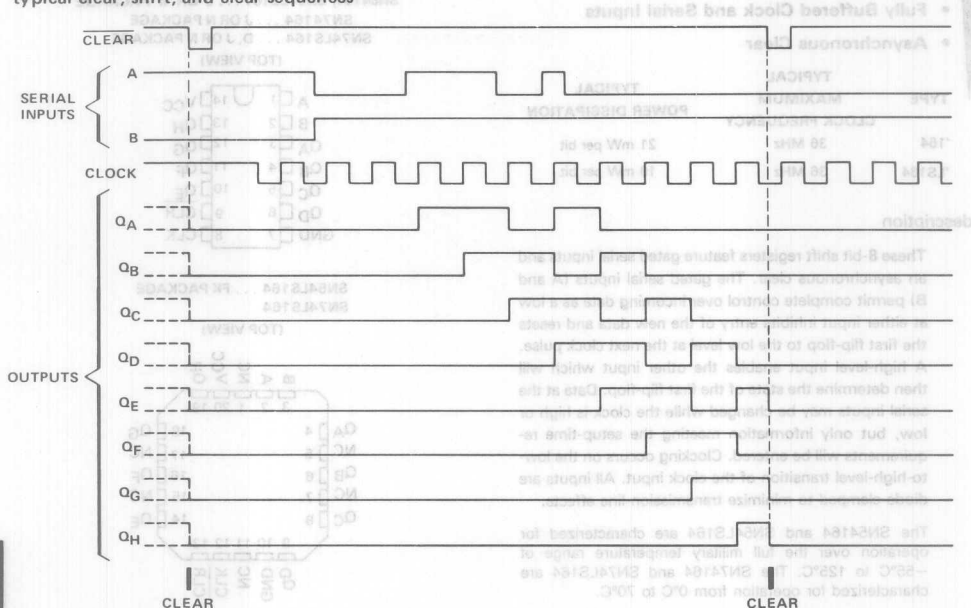
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54164, SN54LS164, SN74164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

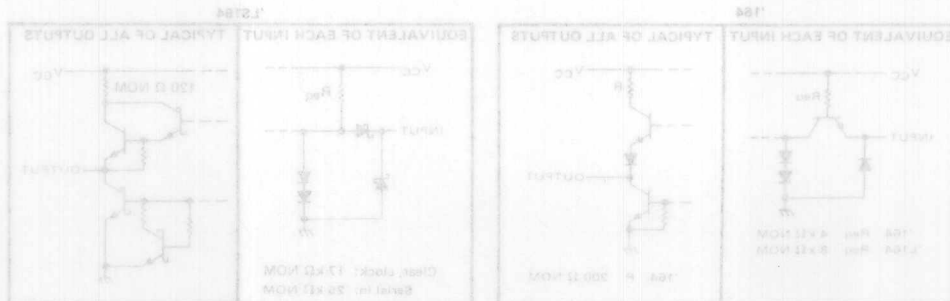
typical clear, shift, and clear sequences



FUNCTION TABLE

INPUTS		OUTPUTS	
CLEAR	CLOCK	A	B
L	X	X	L
H	X	X	X
H	L	X	X
H	H	X	X
H	L	X	X
H	H	X	X
H	L	X	X
H	H	X	X

schematics of inputs and outputs



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TTL DEVICES

logic diagram



TYPES SN54164, SN74164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54164	−55°C to 125°C
SN74164	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164			SN74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_W	20			20			ns
Data setup time, t_{SU} (see Figure 1)	15			15			ns
Data hold time, t_H (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54164			SN74164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			−1.5			−1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.2		2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			−1.6			−1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	−10		−27.5	−9		−27.5	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, V_{I(\text{clock})} = 0.4 \text{ V}$		30			30		mA
	See Note 2, $V_{I(\text{clock})} = 2.4 \text{ V}$		37	54		37	54	

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than two outputs should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$	25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input	$C_L = 15 \text{ pF}$		24	36	ns
	$C_L = 50 \text{ pF}$		28	42	
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	$C_L = 15 \text{ pF}$	8	17	27	ns
	$C_L = 50 \text{ pF}$	10	20	30	
t_{PHL} Propagation delay time, high-to-low-level Q outputs from the clock input	$C_L = 15 \text{ pF}$	10	21	32	ns
	$C_L = 50 \text{ pF}$	10	25	37	

3

TTL DEVICES

TYPES SN54LS164, SN74LS164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS164	-55°C to 125°C
SN74LS164	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS164			SN74LS164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Width of clock or clear input pulse	20			20			ns
t_{su}	Data setup time (See Figure 1)	15			15			ns
t_{su}	Clear inactive setup time (See Figure 1)	15			15			ns
t_h	Data hold time (See Figure 1)	5			5			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS164			SN74LS164			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$ $I_{OH} = -0.4 \text{ mA}$	2.5	3.5		2.7	3.5		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25			0.25 0.35	0.4 0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS}	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ See Note 3}$		16	27		16	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

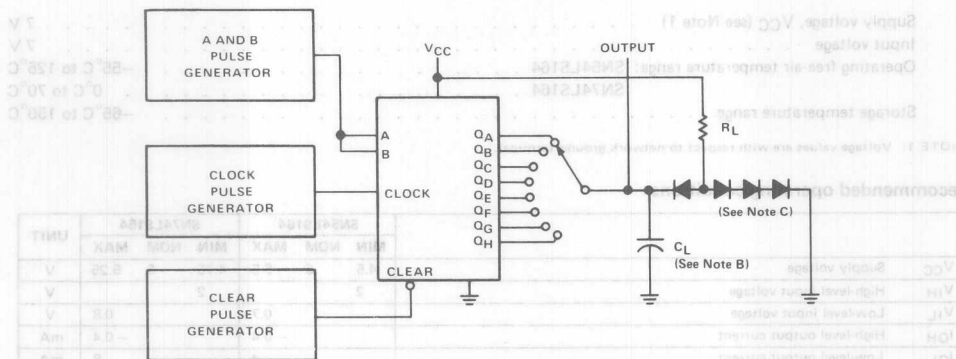
NOTE 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

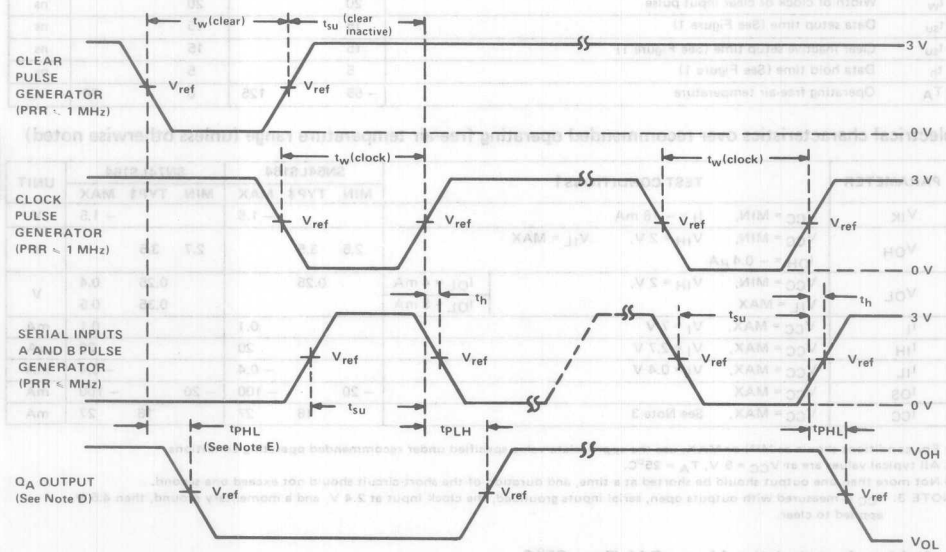
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		24	36	ns
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input	See Figure 1		17	27	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

TYPES SN54164, SN54LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '164, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS164, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
F. For '164, $V_{ref} = 1.5$ V; for 'LS164, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

TYPES SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

OCTOBER 1976 - REVISED APRIL 1985

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165A	35 MHz	90 mW

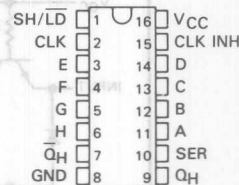
description

The '165 and 'LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register while the shift/load input is low independently of the levels of the clock, clock inhibit, or serial inputs.

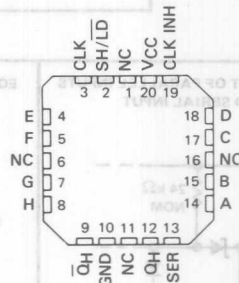
SN54165, SN54LS165A ... J OR W PACKAGE
SN74165 ... J OR N PACKAGE
SN74LS165A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS165A ... FK PACKAGE
SN74LS165A

(TOP VIEW)



FUNCTION TABLE

SHIFT/ LOAD	CLOCK INHIBIT	INPUTS			INTERNAL OUTPUTS		OUTPUT Q_H
		CLOCK	SERIAL	PARALLEL A ... H	Q_A	Q_B	
L	X	X	X	a ... h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

PRODUCTION DATA

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TEXAS
INSTRUMENTS

3-509

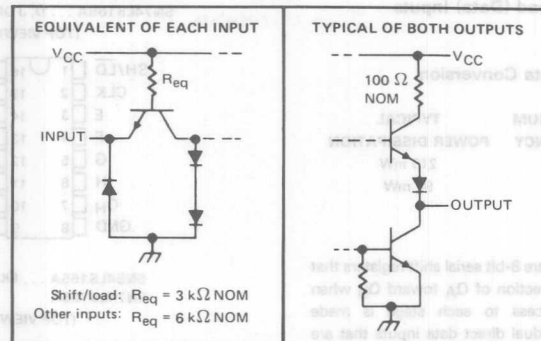
3

TTL DEVICES

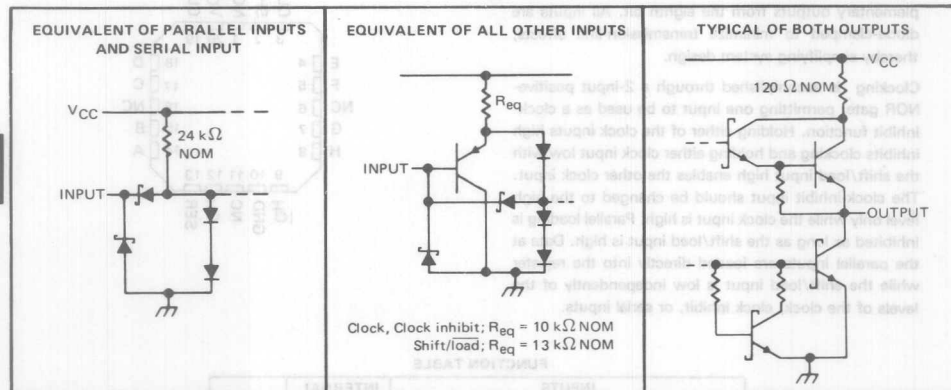
TYPES SN54165, SN54LS165A, SN74165, SN74S165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

schematics of inputs and outputs

'165



'LS165A



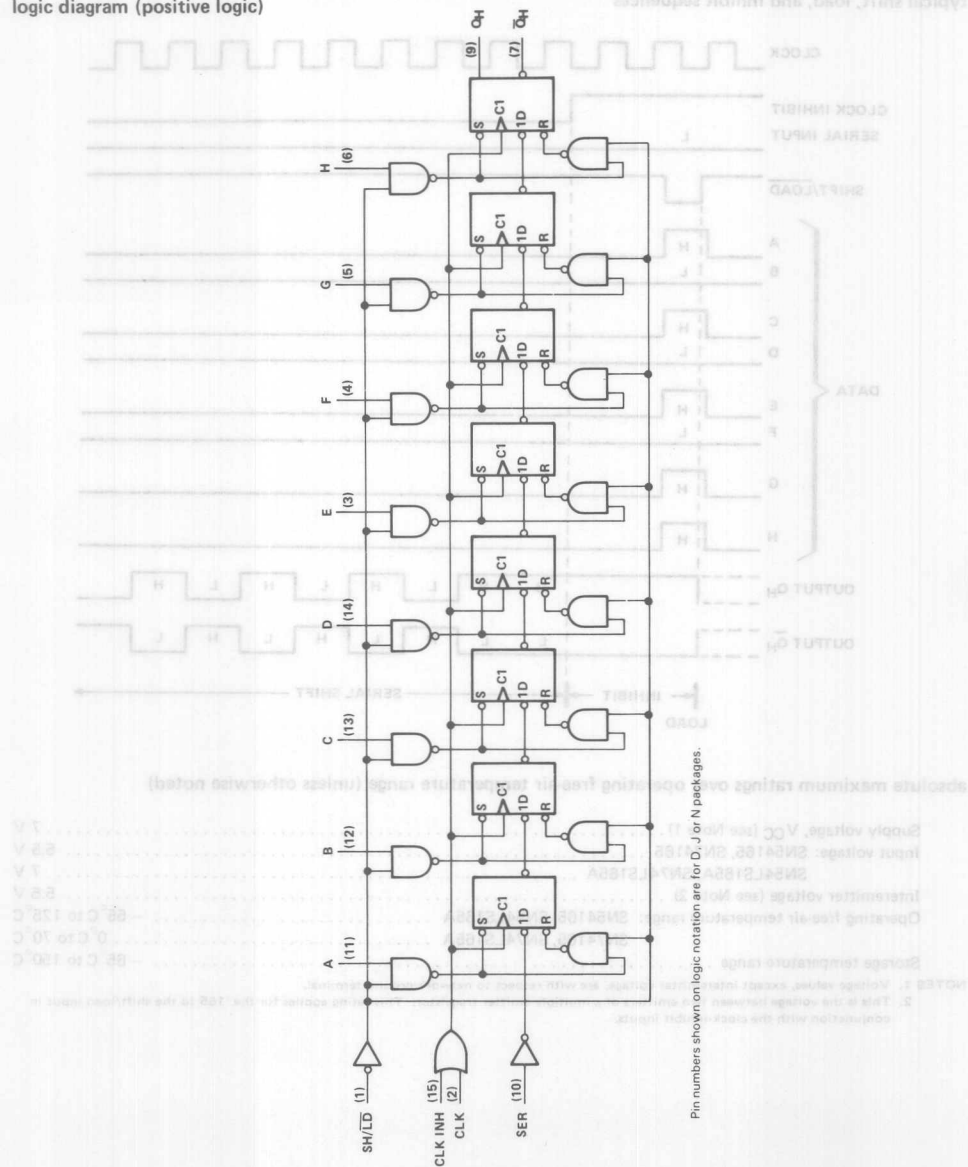
LOAD INHIBIT	SHIFT CLOCK INHIBIT	CLOCK SERIAL	PARALLEL A...H	OUTPUTS	
				QA	QB
H	H	X	X	Q	Q
H	L	X	X	Q	Q
H	L	L	X	Q	Q
H	L	L	X	Q	Q
H	H	X	X	Q	Q

3

TTL DEVICES

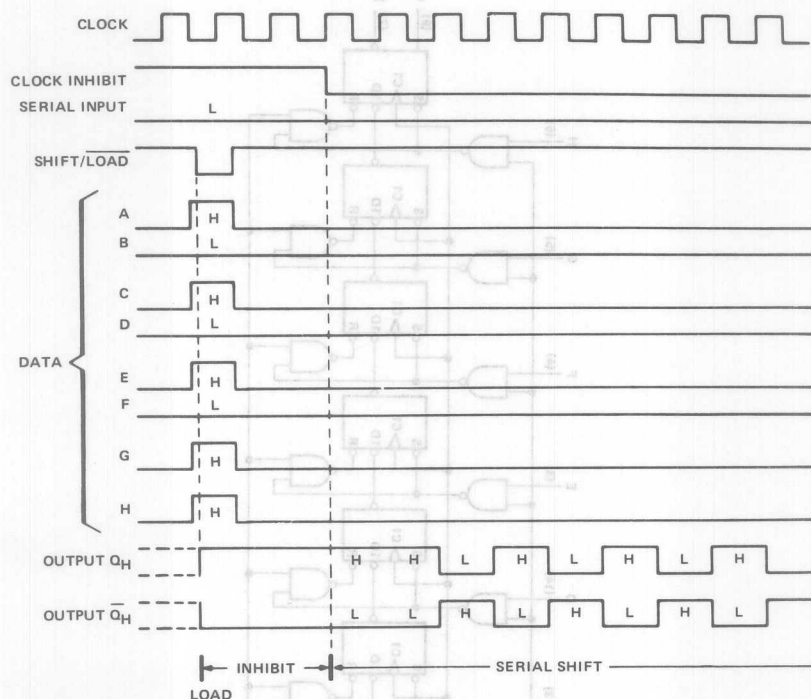
TYPES SN54165, SN54LS165A, SN74165, SN74LS165A
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

logic diagram (positive logic)



TYPES SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SN54165, SN74165	5.5 V
SN54LS165A, SN74LS165A	7 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54165, SN54LS165A	-55°C to 125°C
SN74165, SN74LS165A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the shift/load input in conjunction with the clock-inhibit inputs.

3

TTL DEVICES

PARALLEL-LOAD 8-BIT SHIFT REGISTERS

recommended operating conditions

	SN54165			SN74165			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	-800			-800			μ A
Low-level output current, I_{OL}	16			16			mA
Clock frequency, f_{clock}	0	20	0	20			MHz
Width of clock input pulse, $t_{W(clock)}$	25		25				ns
Width of load input pulse, $t_{W(load)}$	15		15				ns
Clock-enable setup time, t_{SU} (see Figure 1)	30		30				ns
Parallel input setup time, t_{SU} (see Figure 1)	10		10				ns
Serial input setup time, t_{SU} (see Figure 2)	20		20				ns
Shift setup time, t_{SU} (see Figure 2)	45		45				ns
Hold time at any input, t_H	0		0				ns
Operating free-air temperature, T_A	-55	125	0	70			C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54165			SN74165			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	Shift/load			80			80	μ A
	Other inputs			40			40	μ A
I_{IL} Low-level input current	Shift/load			3.2			3.2	mA
	Other inputs			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		55	18		55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3	42	63		42	63		mA

NOTE 3: With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift/load input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15 \text{ pF}, R_L = 400 \Omega$, See figures 1 thru 3	20	26		MHz
t_{PLH}	$\overline{\text{Load}}$	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	\overline{O}_H			18	27	ns
t_{PHL}					18	27	

¶ f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

TYPES SN54LS165A, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS165A			SN74LS165A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		25	0		25	MHz
t _{w(clock)}	Width of clock input pulse (See Figure 1)		15			15		ns
			25			25		
t _{w(load)}	Width of load input pulse		25			25		ns
			17			17		
t _{su}	Clock-enable setup time (See Figure 1)		30			30		ns
t _{su}	Parallel input setup time (See Figure 1)		10			10		ns
t _{su}	Serial input setup time (See Figure 2)		20			20		ns
t _{su}	Shift setup time (See Figure 2)		45			45		ns
t _h	Hold time at any input		0			0		ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LS165A			SN74LS165A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -0.4 mA, V _{IL} = MAX.	2.5	3.5		2.7	3.5		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX.		0.25	0.4		0.25	0.4	V
						0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS‡}	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, See Note 3		18	30		18	30	mA

NOTE 3: With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift/load input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	35		MHz
t _{PLH}	Load	Any	R _L = 2 kΩ, See Figures 1 thru 3	21	35		ns
t _{PHL}				26	35		
t _{PLH}	Clock	Any		14	25		ns
t _{PHL}				16	25		
t _{PLH}	H	Q _H		13	25		ns
t _{PHL}				24	30		
t _{PLH}	H	\overline{Q}_H		19	30		ns
t _{PHL}				17	25		

† f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

3

TTL DEVICES

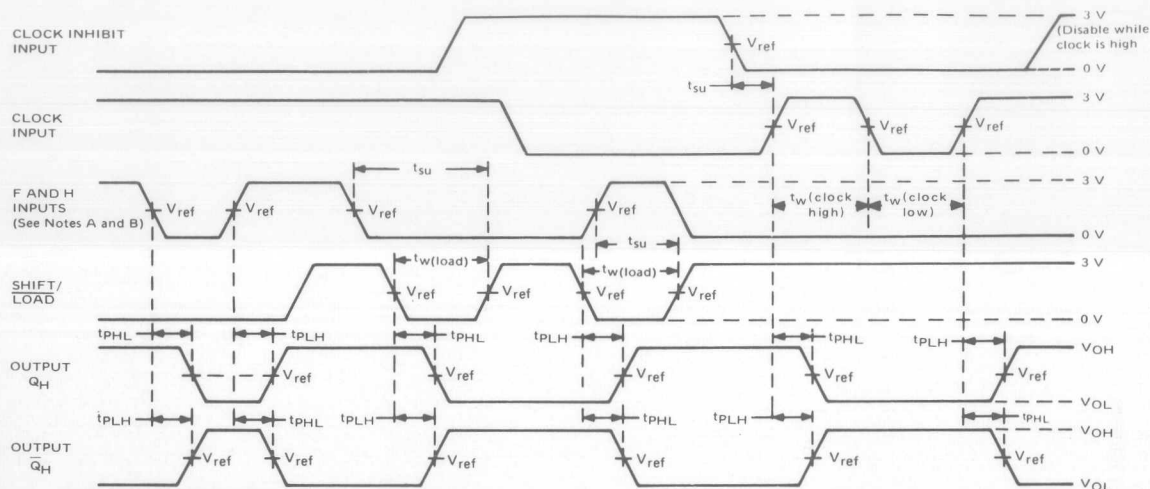
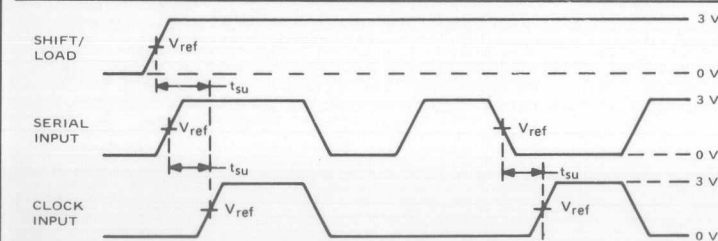
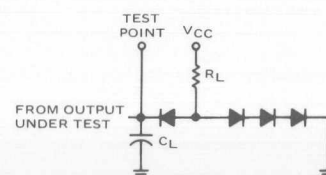


FIGURE 1—VOLTAGE WAVEFORMS



- NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at $t_n + 7$.
B. The input pulse generators have the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for '165, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$; for 'LS165A, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
C. For '165, $V_{ref} = 1.5 \text{ V}$; for 'LS165A, $V_{ref} = 1.3 \text{ V}$.

FIGURE 2—VOLTAGE WAVEFORMS



- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.

FIGURE 3—LOAD CIRCUIT FOR SWITCHING TESTS

TYPES SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

OCTOBER 1976—REVISED DECEMBER 1983

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'166	35 MHz	360 mW
'LS166A	35 MHz	100 mW

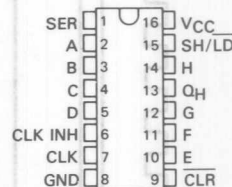
description

The '166 and 'LS166A 8-bit shift registers are compatible with most other TTL logic families. All '166 and 'LS166A inputs are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

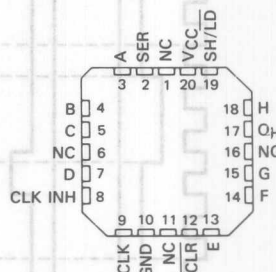
SN54166, SN54LS166A ... J OR W PACKAGE
SN74166 ... J OR N PACKAGE
SN74LS166A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS166A ... FK PACKAGE
SN74LS166A

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	QA _n	QH _n
H	H	L	↑	L	X	L	QA _n	QH _n
H	X	H	↑	X	X	QA0	QB0	QH0

PRODUCTION DATA

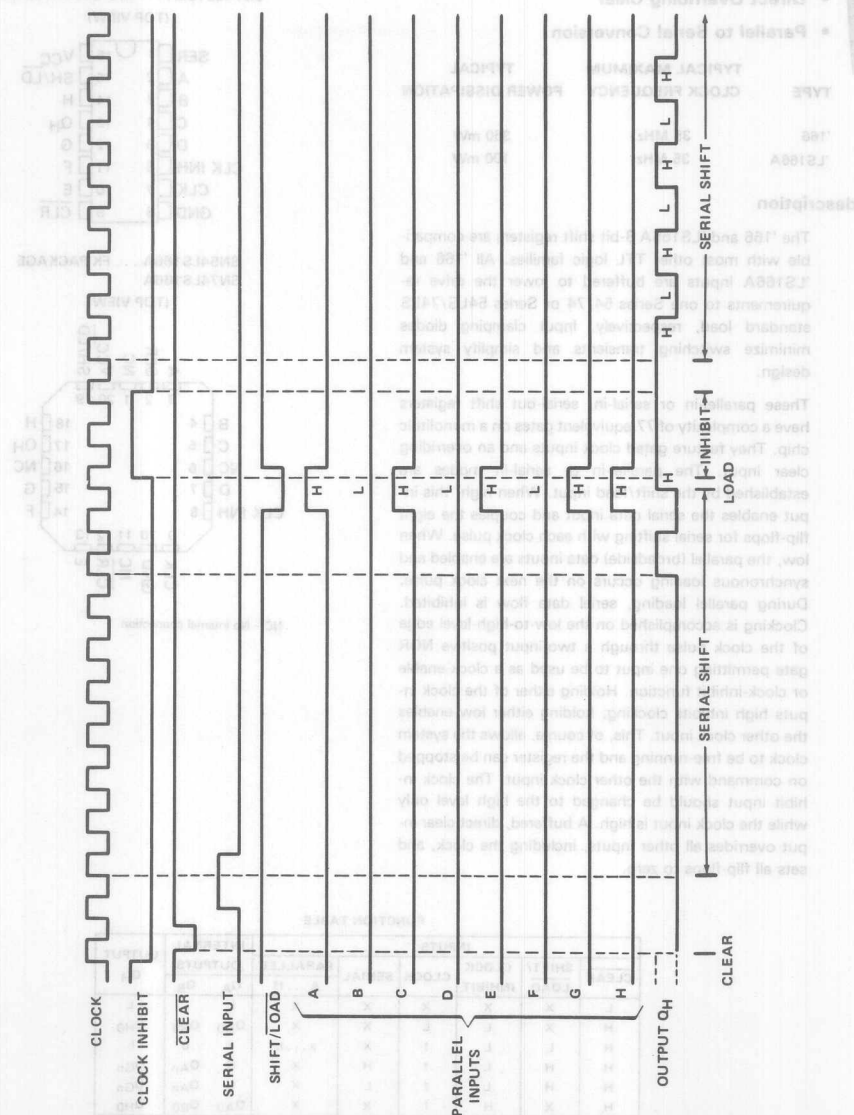
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TEXAS
INSTRUMENTS

3-517

TYPES SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

typical clear, shift, load, inhibit, and shift sequences



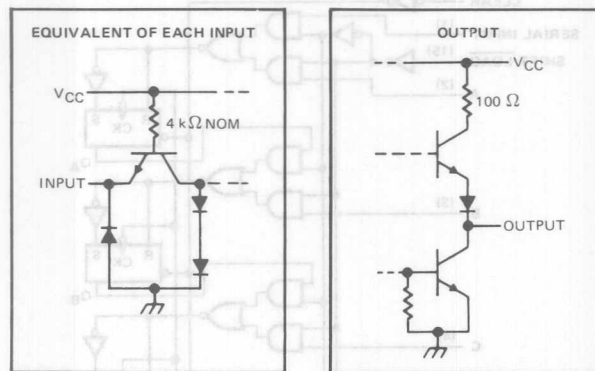
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TTL DEVICES

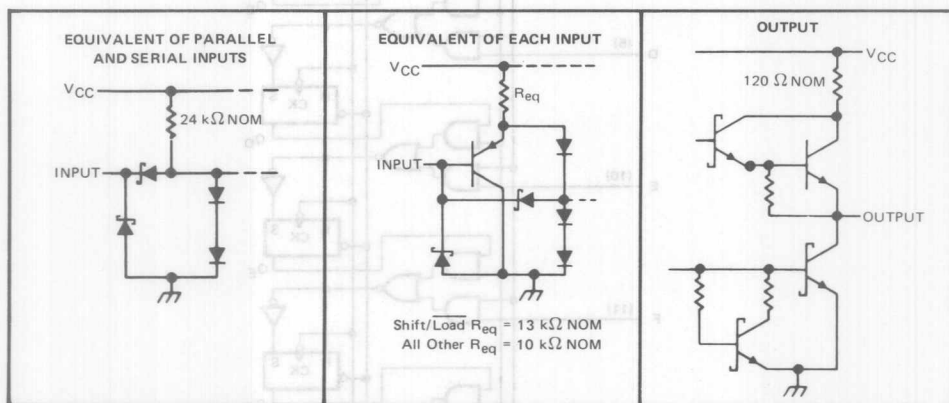
TYPES SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

schematics of inputs and outputs

'166



'LS166A

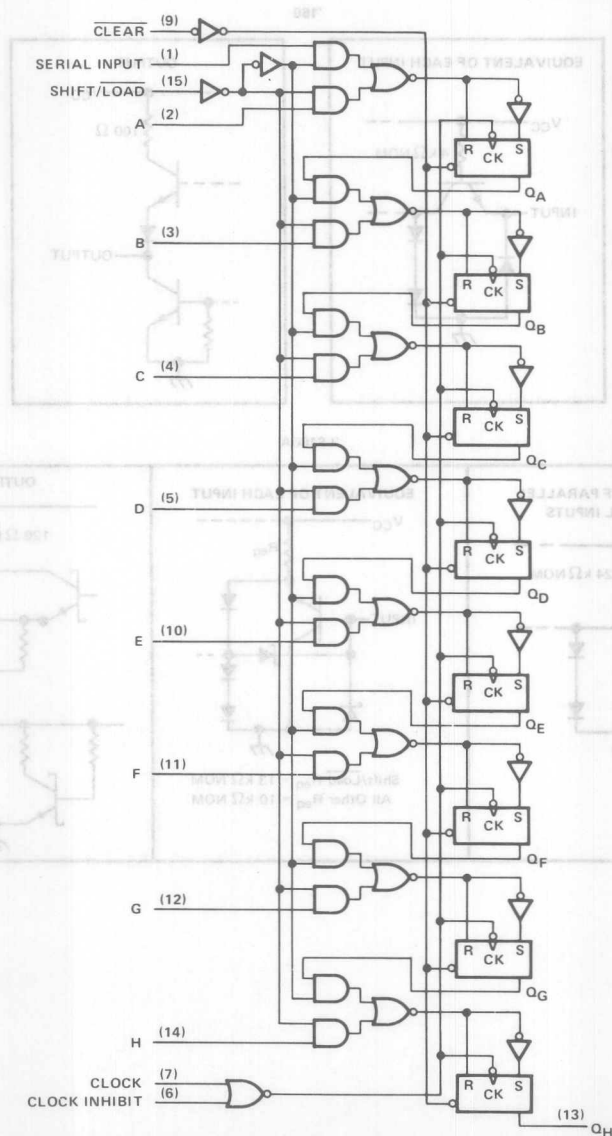


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TTL DEVICES

TYPES SN54166, SN54LS166A, SN74166, SN74LS166A
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

AB812J TYPES SN54166, SN74166 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54166 (see Note 2)	-55°C to 125°C
SN74166	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54166			SN74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W (see Figure 1)	20			20			ns
Mode-control setup time, t_{SU}	30			30			ns
Data setup time, t_{SU} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A (see Note 2)	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54166			SN74166			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3	90	127		90	127		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54166 in the W package operating at free-air temperatures above 113°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.
3. With all outputs open, 4.5 V applied to the serial input, all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to the clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	35		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}, R_L = 400 \Omega$, See Figure 1		23	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			20	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			17	26	ns

TYPES SN54LS166A, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS166A	–55°C to 125°C
SN74LS166A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS166A			SN74LS166A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Width of clear pulse (See Figure 1)	20			20			ns
t_w	Width of clock pulse (See Figure 1)	High	15		15			ns
		Low	25		25			ns
t_{su}	Mode-control setup time	30			30			ns
t_{su}	Data setup time (See Figure 1)	20			20			ns
t_h	Hold time at any input (See Figure 1 and Note 4)	0			0			ns
T_A	Operating free air temperature	–55		125	0		70	°C

NOTE 4: The hold time limit of 0 ns applies only if the rise time is less than or equal to 10 ns.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS166A			SN74LS166A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		–0.4			–0.4		mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	–20	–100		–20	–100		mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ See Note 5}$	20	32		20	32		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration for short-circuit should not exceed one second.

NOTE 5: With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, than 4.5 V, is applied to clock.

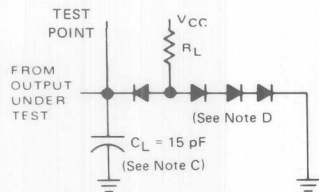
switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency			25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear	$C_L = 15\text{ pF}, R_L = 2\text{ k}\Omega$, See Figure 1			19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	14	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			5	11	20	ns

$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$,
See Figure 1

TYPES SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

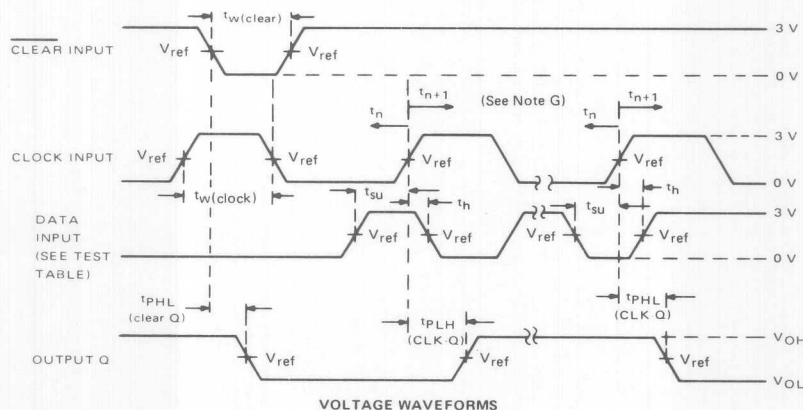
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE F)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}



- NOTE: A. All pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$; for '166, $t_r \leq 7$ ns and $t_f \leq 7$ ns; for 'LS166A, $t_r \leq 15$ ns and $t_f \leq 6$ ns.
- B. The clock pulse has the following characteristics: $t_w(\text{clock}) \leq 20$ ns and $\text{PRR} = 1$ MHz. The clear pulse has the following characteristics: $t_w(\text{clear}) \leq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max} , vary the clock PRR.
- C. C_L includes probe and jig capacitance.
- D. All diodes are 1N3064, 1N916, or equivalent.
- E. A clear pulse is applied prior to each test.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+8} with a functional test.
- G. t_n = bit time before clocking transition
 t_{n+1} = bit time after one clocking transition
 t_{n+8} = bit time after eight clocking transitions
- H. For '166 $V_{ref} = 1.5$ V; for 'LS166A $V_{ref} = 1.3$ V.

FIGURE 1

3

TYPES SN54167, SN74167 SYNCHRONOUS DECADE RATE MULTIPLIERS

DECEMBER 1972—REVISED DECEMBER 1983

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 MHz

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These decade counters feature buffered clock, clear, enable and set-to-nine inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe set-to-nine, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 10, ie:

$$f_{out} = \frac{M \cdot f_{in}}{10}$$

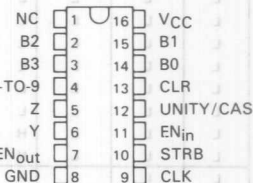
where: $M = B_3 \cdot 2^3 + B_2 \cdot 2^2 + B_1 \cdot 2^1 + B_0 \cdot 2^0$ for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform two-decade rate multiplication (0.99), the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output. For longer words, see typical application data, Figure 1.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the output. These devices are completely compatible with most TTL and DTL families. Typical dissipation is 270 milliwatts. The SN54167 is characterized for operation over the full military temperature range of -55°C to 125°C , and the SN74167 is characterized for operation from 0°C to 70°C .

SN54167 . . . J OR W PACKAGE
SN74167 . . . J OR N PACKAGE
(TOP VIEW)



NC—No internal connection

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TTL DEVICES

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-525

TYPES SN54167, SN74167 SYNCHRONOUS DECADE RATE MULTIPLIERS

STATE AND/OR RATE FUNCTION TABLE (See Note A)

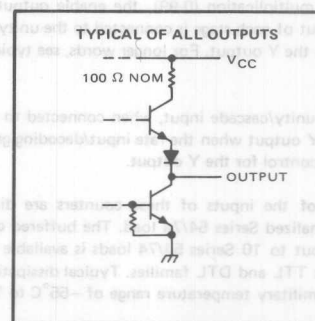
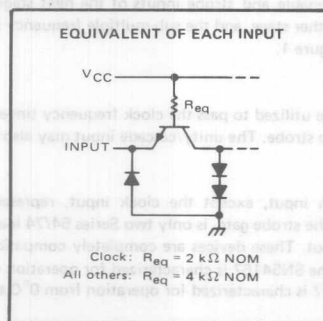
INPUTS										OUTPUTS			
CLEAR	ENABLE	STROBE	BCD RATE				NUMBER OF CLOCK PULSES	UNITY/ CASCADE	LOGIC LEVEL OR NUMBER OF PULSES	LOGIC LEVEL OR NUMBER OF PULSES			NOTES
			B3	B2	B1	B0				Y	Z	ENABLE	
H	X	H	X	X	X	X	X	H	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	1	C
L	L	L	L	L	L	H	10	H	1	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	1	C
L	L	L	L	L	H	H	10	H	3	3	1	1	C
L	L	L	L	H	L	L	10	H	4	4	1	1	C
L	L	L	L	H	L	H	10	H	5	5	1	1	C
L	L	L	L	H	H	L	10	H	6	6	1	1	C
L	L	L	L	H	H	H	10	H	7	7	1	1	C
L	L	L	H	L	L	L	10	H	8	8	1	1	C
L	L	L	H	L	L	H	10	H	9	9	1	1	C
L	L	L	H	L	H	L	10	H	8	8	1	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	1	E

- NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
 B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
 C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
 D. These input conditions exceed the range of the decimal rate inputs.
 E. Unity/cascade can be used to inhibit output Y.

3

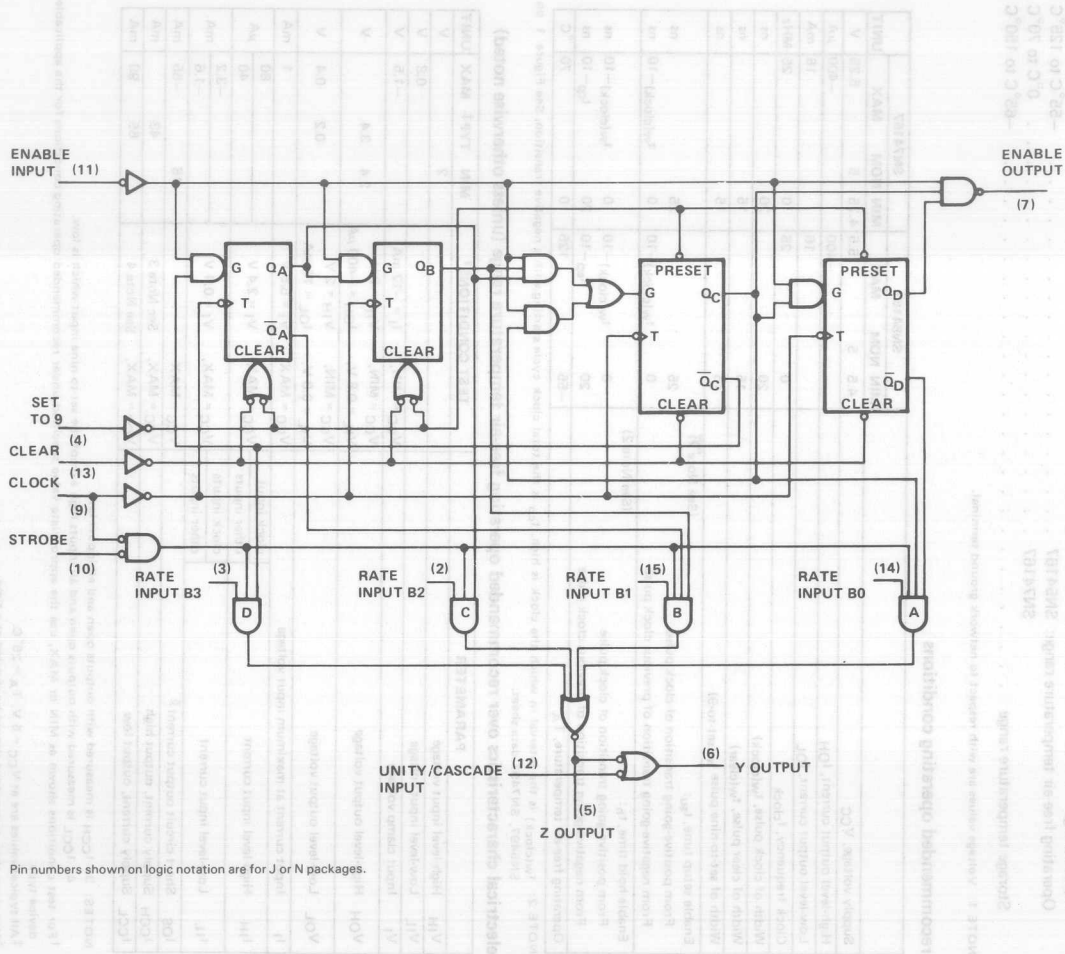
TTL DEVICES

schematics of inputs and outputs



TYPES SN64167, SN74167 SYNCHRONOUS DECADE RATE MULTIPLIERS

logic diagram



TTL DEVICES

3

TYPES SN54167, SN74167

SYNCHRONOUS DECADE RATE MULTIPLIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54167	−55°C to 125°C
SN74167	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54167			SN74167			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Width of set-to-nine pulse $t_{w(set-to-9)}$	15			15			ns
Enable setup time, t_{SU} : From positive-going transition of clock pulse	25			25			ns
From negative-going transition of previous clock pulse	0	$t_{w(clock)} - 10$		0	$t_{w(clock)} - 10$		ns
Enable hold time, t_H : From positive-going transition of clock pulse	0	$t_{w(clock)} - 10$		0	$t_{w(clock)} - 10$		ns
From negative-going transition of previous clock pulse	20	$t_{cp} - 10$		20	$t_{cp} - 10$		ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 2: $t_{w(clock)}$ is the interval in which the clock is high. t_{cp} is the total clock cycle starting with a negative transition. See Figure 1 on SN5497, SN7497 data sheet.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			−1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	clock input $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ other inputs			80 40	μ A
I_{IL} Low-level input current	clock inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ other inputs			−3.2 −1.6	mA
I_{OS} Short circuit output current [§]	$V_{CC} = \text{MAX}$			−18	mA
I_{CCH} Supply current, output high	$V_{CC} = \text{MAX},$ See Note 3			43	mA
I_{CCL} Supply current, output low	$V_{CC} = \text{MAX},$ See Note 4			65 99	mA

NOTES: 3. I_{CCH} is measured with outputs open and all inputs low.

4. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input which is low.

[†] For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

TYPES SN54167, SN74167
SYNCHRONOUS DECADE RATE MULTIPLIERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETERS*	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{max}				25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z	$C_L = 15 \text{ pF}$ $R_L = 400 \, \Omega$, See Note 5		9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PHL}	Set-to-9	Enable			18	27	ns
t_{PLH}					15	23	
t_{PHL}	Any Rate Input	Y			15	23	ns

f_{\max} is maximum clock frequency.

t_{pLH} is propagation delay time, low-to-high-level output.

t_{PHL} is propagation delay time, high-to-low-level output.

NOTE 5: Load circuit, voltage waveforms, and input conditions for measuring switching characteristics are the same as those for the SN5497 and SN7497.

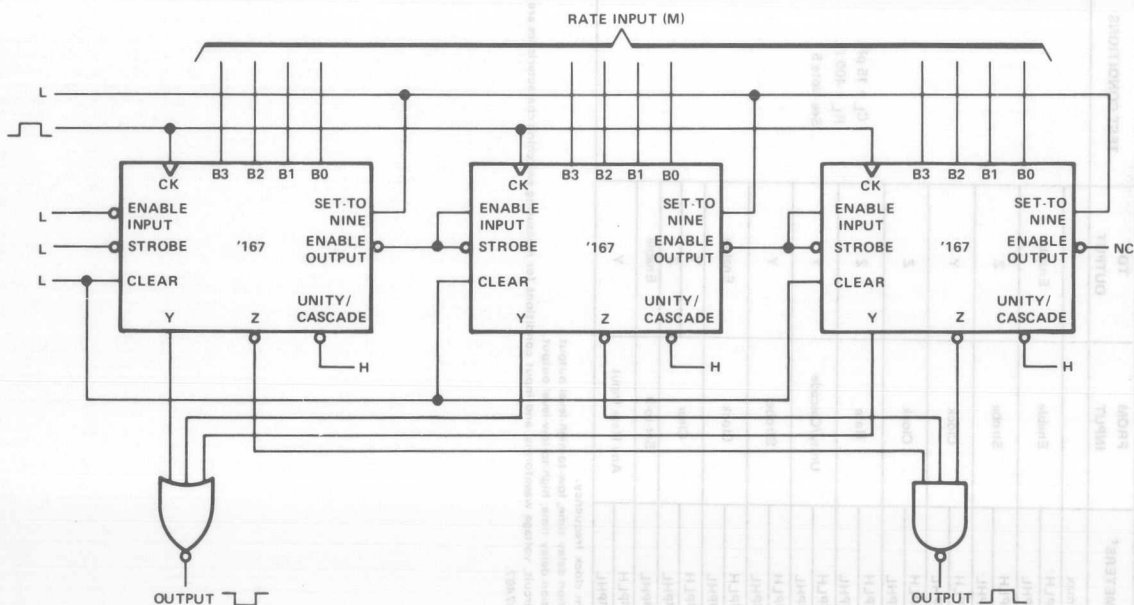
3

TTL DEVICES

TYPES SN54167, SN74167 SYNCHRONOUS DECADE RATE MULTIPLIERS

TYPICAL APPLICATION DATA

V_{CC} = 5.0V, J_W = 25°C, J_W = 25°C



This application demonstrates how the decimal-rate multipliers may be cascaded for longer words. Three decades are illustrated (0.999 to 999) although longer words can be implemented by using the pattern shown. The output is decoded either from output Y with a NOR gate or from output Z with a NAND gate. Either method of decoding produces the complement of the output used.

TTL DEVICES

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TYPES SN54LS169B, SN54S168, SN54S169, SN74LS169B, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

OCTOBER 1976—REVISED MAY 1983

'S168 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS 'LS169B, 'S169 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

- Programmable Look-Ahead Up/Down Binary/Decade Counters
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high speed counting applications. The 'S168 is a decade counter and the 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

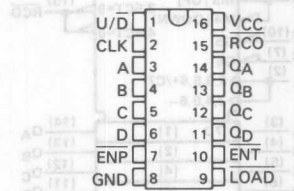
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (ENP, ENT) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input ENT is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, $\overline{\text{LOAD}}$, U/D) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

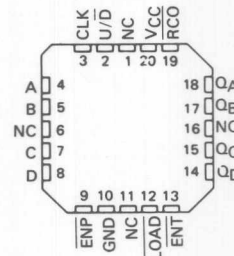
SN54S168, SN54LS169B, SN54S169 . . . J OR W PACKAGE
SN74S168, SN74LS169B, SN74S169 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54S168, SN54LS169B, SN54S169 . . . FK PACKAGE
SN74S168, SN74LS169B, SN74S169

(TOP VIEW)



NC—No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169B	35MHz	35MHz	100mW
'S168, 'S169	70MHz	55MHz	500mW

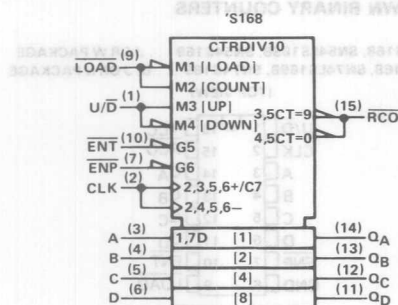
PRODUCTION DATA
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TEXAS
INSTRUMENTS

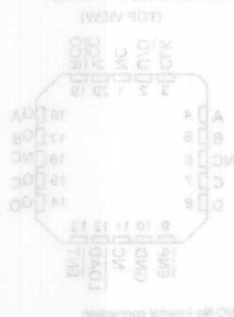
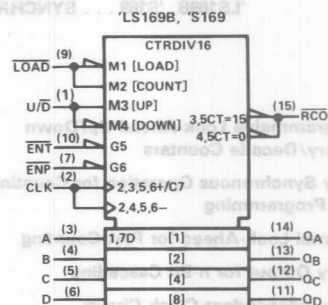
3-531

TYPES SN54LS169B, SN54S168, SN54S169, SN74LS169B, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.



TYPICAL POWER DISSIPATION	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPE
	COUNTING UP	COUNTING DOWN	
100mW	25MHz	25MHz	LS169B
200mW	20MHz	20MHz	LS168

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumentation in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (ENP, ENT) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input ENT is tied forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level output can be used to enable associated cascaded stages. Transitions at the ENP or ENT inputs are allowed regardless of the level of the clock input. All inputs are edge-triggered to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock input. Changes to control inputs (ENP, ENT, U/D) that will modify the counting mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, holding, or counting) will be dictated solely by the conditions meeting the setup and hold times.

These counters are fully programmable; that is, the outputs may be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

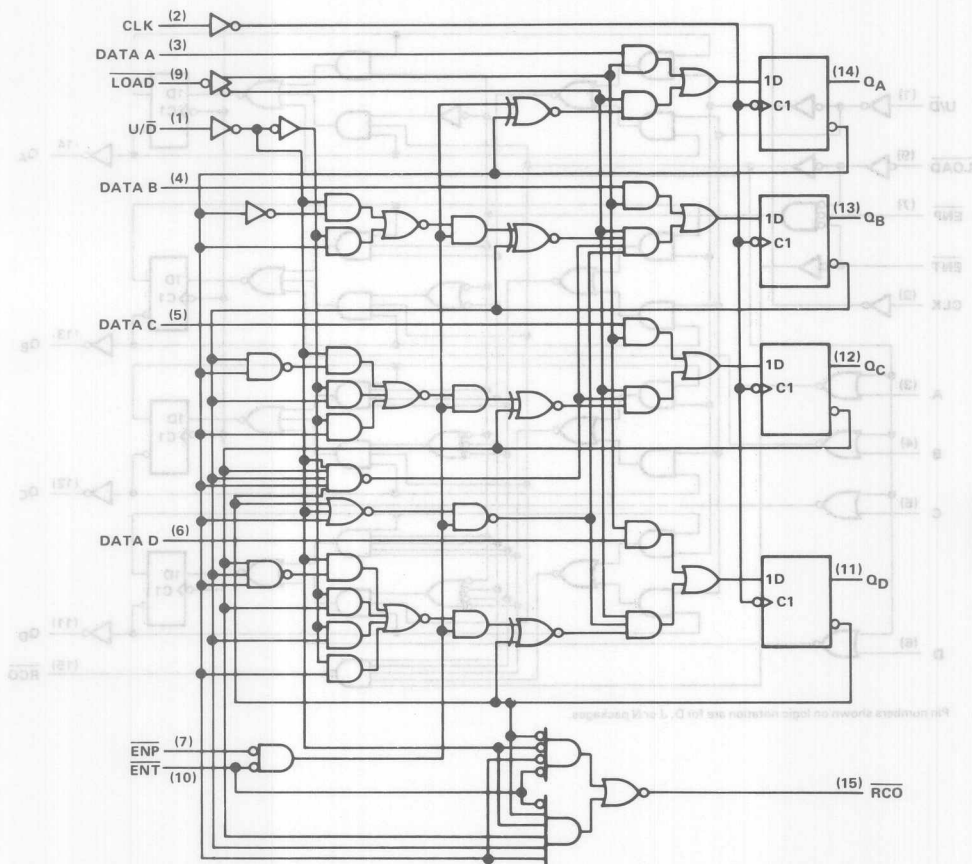
These counters are fully programmable; that is, the outputs may be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

3
TTL DEVICES

TYPES SN54S168, SN74S168 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

logic diagram

SN54S168, SN74S168 DECADE COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

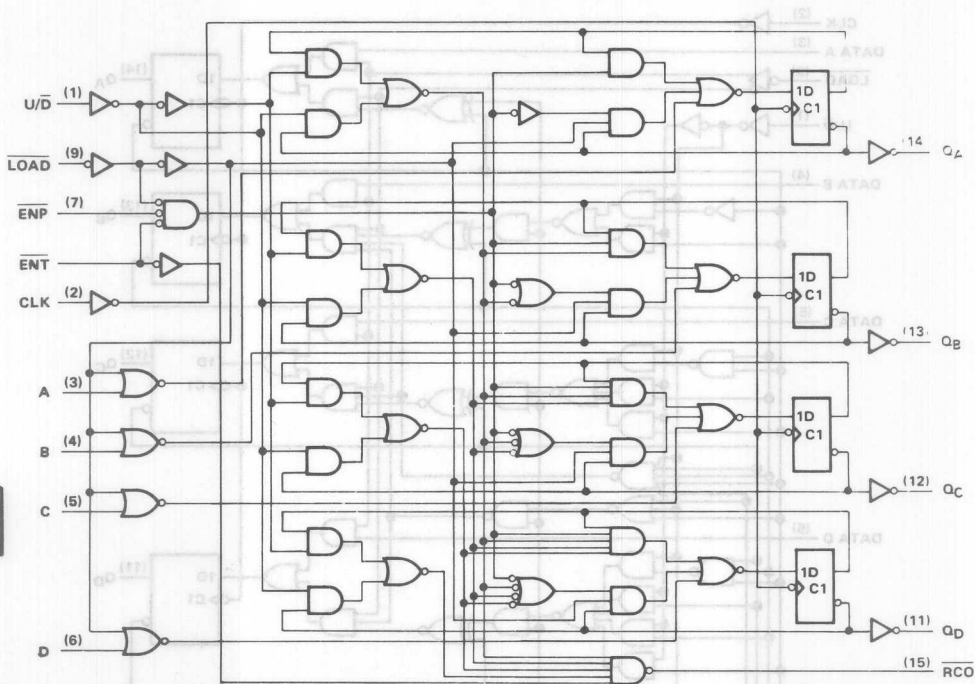
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TTL DEVICES

TYPES SN54LS169B, SN74LS169B SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

logic diagram

SN54LS169B, SN74LS169B BINARY COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

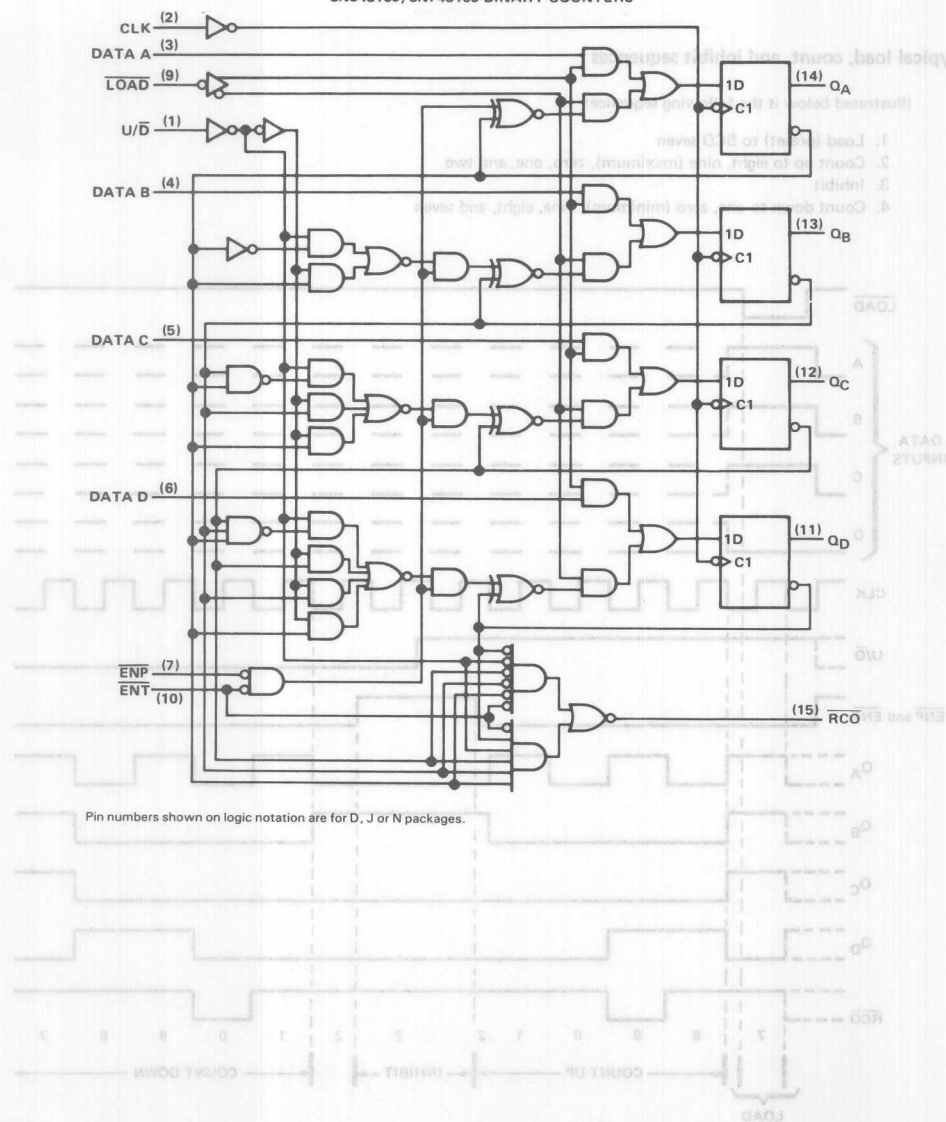
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TTL DEVICES

TYPES SN54S169, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

logic diagram

SN54S169, SN74S169 BINARY COUNTERS



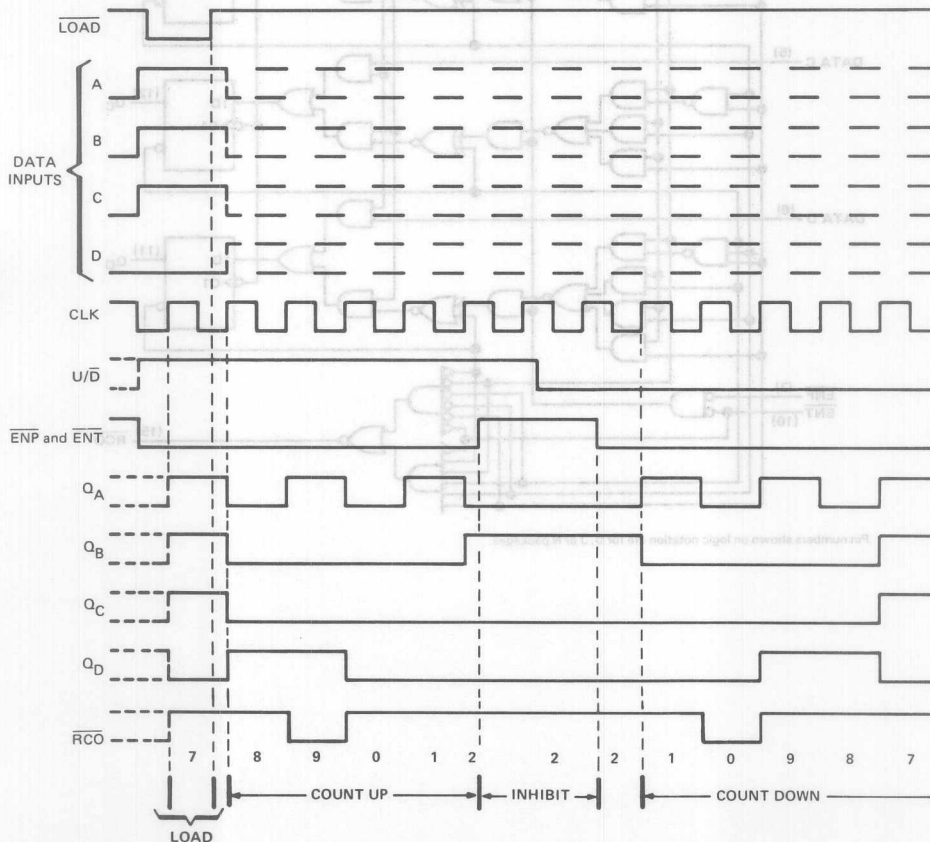
3

TTL DEVICES

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



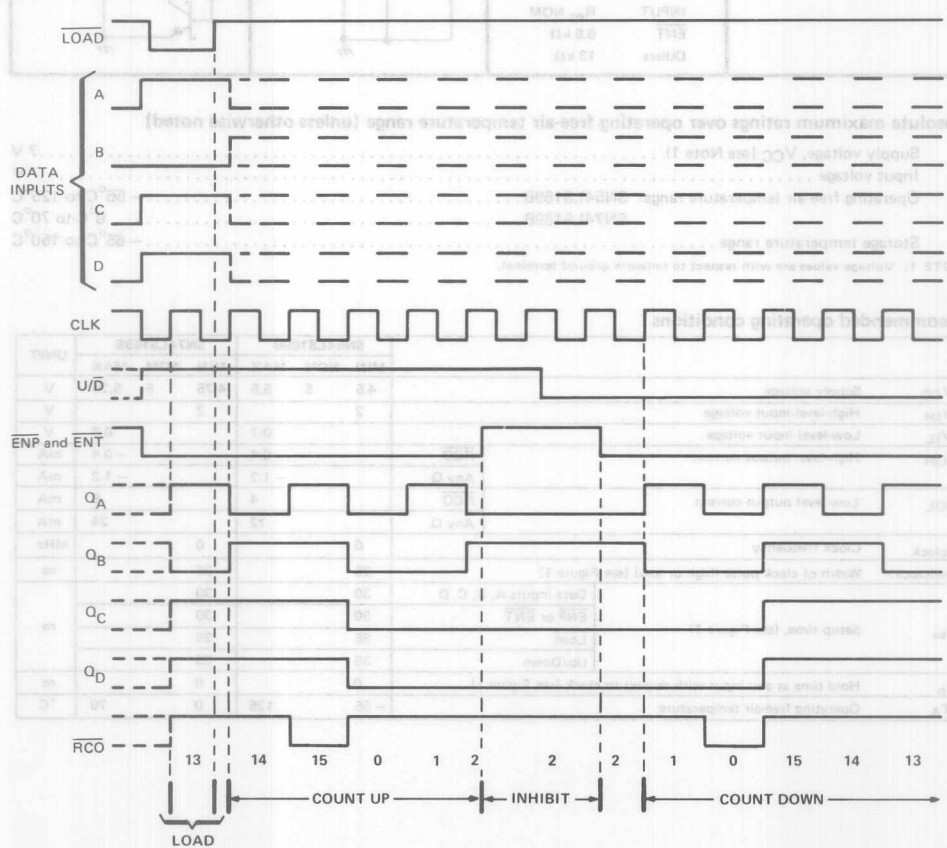
TYPES SN54LS169B, SN54S169, SN74LS169B, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

'LS169B, 'S169 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen

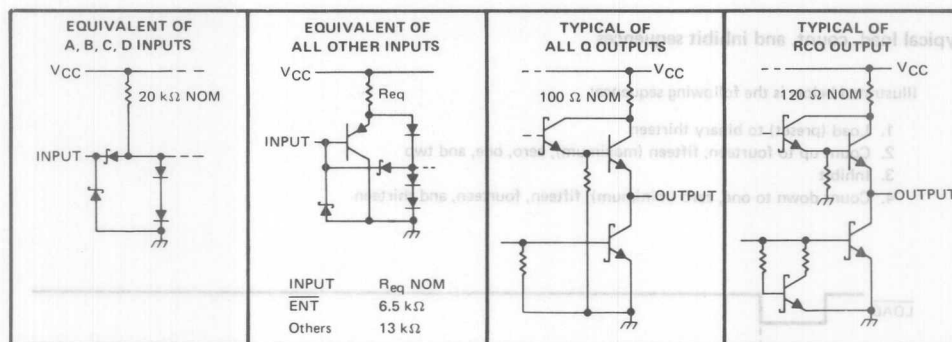


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TTL DEVICES

TYPES SN54LS169B, SN74LS169B SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1).	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS169B	-55°C to 125°C
SN74LS169B	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

recommended operating conditions

		SN54LS169B			SN74LS169B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			-1.2			-1.2	mA
				4			8	mA
				12			24	mA
f_{clock}	Clock frequency	0			0			MHz
$t_{w(clock)}$	Width of clock pulse (high or low) (see Figure 1)	25			25			ns
t_{su}	Setup time, (see Figure 1)							ns
t_h	Hold time at any input with respect to clock (see Figure 1)	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

TYPES SN54LS169B, SN74LS169B SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS169B			SN74LS169B			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN.}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX.}$	\overline{RCO} Any Q	$I_{OH} = -0.4 \text{ mA}$ $I_{OH} = -1.2 \text{ mA}$	2.5 3.4 2.4 3.2		2.7 3.4 2.4 3.2		V
V_{OL}	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX.}$	\overline{RCO}	$I_{OH} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25 0.4		0.25 0.4		V
		Any Q	$I_{OL} = 12 \text{ mA}$	0.25		0.25		
			$I_{OL} = 24 \text{ mA}$	0.4		0.4		
						0.35 0.5		
I_I	$V_{CC} = \text{MAX.}$, $V_I = 7 \text{ V}$			0.1		0.1		mA
I_{IH}	$V_{CC} = \text{MAX.}$, $V_I = 2.7 \text{ V}$			20		20		μA
I_{IL}	$V_{CC} = \text{MAX.}$, $V_I = 0.4 \text{ V}$	U/D, LOAD, ENP, CLK		-0.2		-0.2		mA
		All other inputs		-0.4		-0.4		
$I_{OS}§$	$V_{CC} = \text{MAX.}$, $V_O = 0 \text{ V}$	\overline{RCO}		-20		-100		mA
		Any Q		-30		-130		
I_{CC}	$V_{CC} = \text{MAX.}$, See Note 2			28 45		28 45		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS169B			UNIT
				MIN	TYP	MAX	
f_{max}				20	35		MHz
t_{PLH}	CLK	$\overline{\text{RCO}}$	$R_L = 2 \text{ k}\Omega$ $C_L = 15 \text{ pF}$		26	40	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$			15	25	ns
t_{PHL}					11	20	
t_{PLH}	U/D	$\overline{\text{RCO}}$			23	35	ns
t_{PHL}					15	25	
t_{PLH}	CLK	Any Q	$R_L = 667 \Omega$ $C_L = 45 \text{ pF}$		16	25	ns
t_{PHL}					17	25	

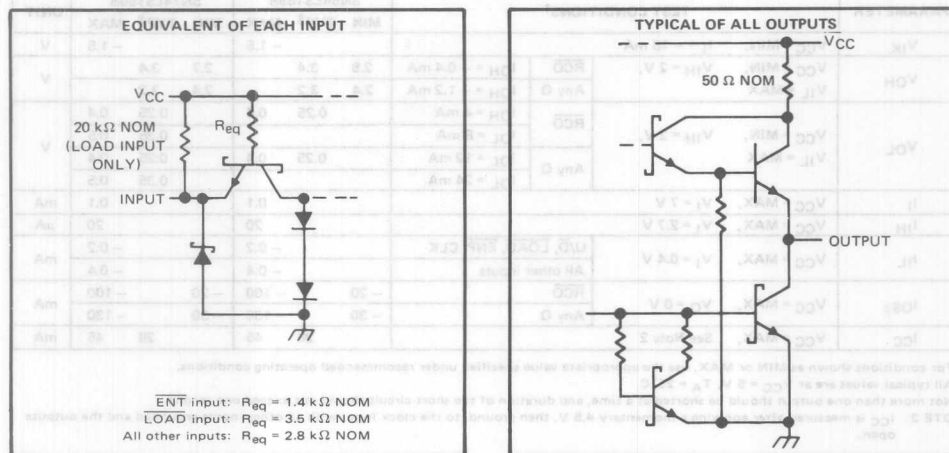
¶ Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (15), the ripple carry output will be out of phase.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54S168, SN54S169, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4)	7 V
Input voltage	5.5 V
Intermittent voltage (see Note 5)	5.5 V
Operating free-air temperature range: SN54S168, SN54S169 (see Note 6)	-55°C to 125°C
SN74S168, SN74S169	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54S168 SN54S169			SN74S168 SN74S169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{W(clock)}$ (high or low) (see Figure 1)		10			10			ns
Setup time, t_{SU} (see Figure 1)	Data inputs A, B, C, D	4			4			ns
	ENP or ENT	14			14			
	Load	6			6			
	Up/Down	20			20			
Hold time at any input with respect to clock, t_H (see Figure 1)		1			1			ns
Operating free-air temperature, T_A (see Note 6)		-55		125	0		70	°C

- NOTES:
4. Voltage values, except intermittent voltage, are with respect to network ground terminal.
 5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs ENP and ENT.
 6. An SN54S168 or SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

TYPES SN54S168, SN54S169, SN74S168, SN74S169 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S168 SN54S169			SN74S168 SN74S169			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	ENT			100			100	µA
	Load			-10			-200	
	Other inputs			50			50	
I _{IL} Low-level input current	ENT			-4			-4	mA
	Other inputs			-2			-2	
I _{OS} Short-circuit output current§	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	100	160		100	160		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	UP/DOWN = HIGH			UP/DOWN = LOW			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}				40	70		40	55		MHz
t _{PLH}	CLK	RCO			14	21		14	21	ns
t _{PHL}					20	28		20	28	
t _{PLH}	CLK	Any Q			8	15		8	15	ns
t _{PHL}					11	15		11	15	
t _{PLH}	ENT	RCO			7.5	11		6	12	ns
t _{PHL}					15	22		15	25	
t _{PLH} °	U/D	RCO			9	15		8	15	ns
t _{PHL} °					10	15		16	22	

¶ f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'S169), the ripple carry output will be out of phase.

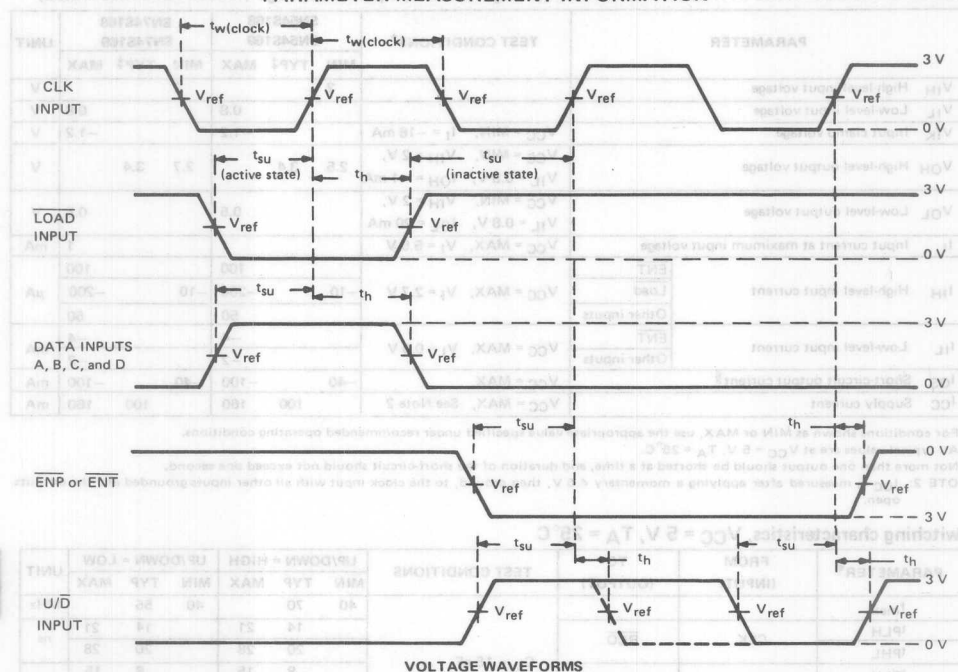
NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

**TYPES SN54LS169B, SN54S168, SN54S169,
SN74LS169B, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS**

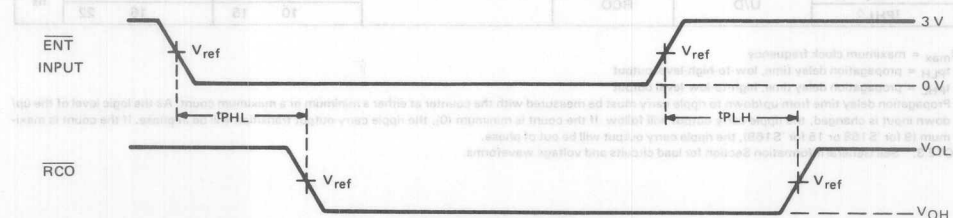
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns, and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

FIGURE 1—PULSE WIDTHS, SETUP TIMES, HOLD TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. t_{PLH} and t_{PHL} from enable T input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S168, all Q outputs high for 'LS169B and 'S169).
C. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'LS169B and 'S169), the ripple carry output will be out of phase.

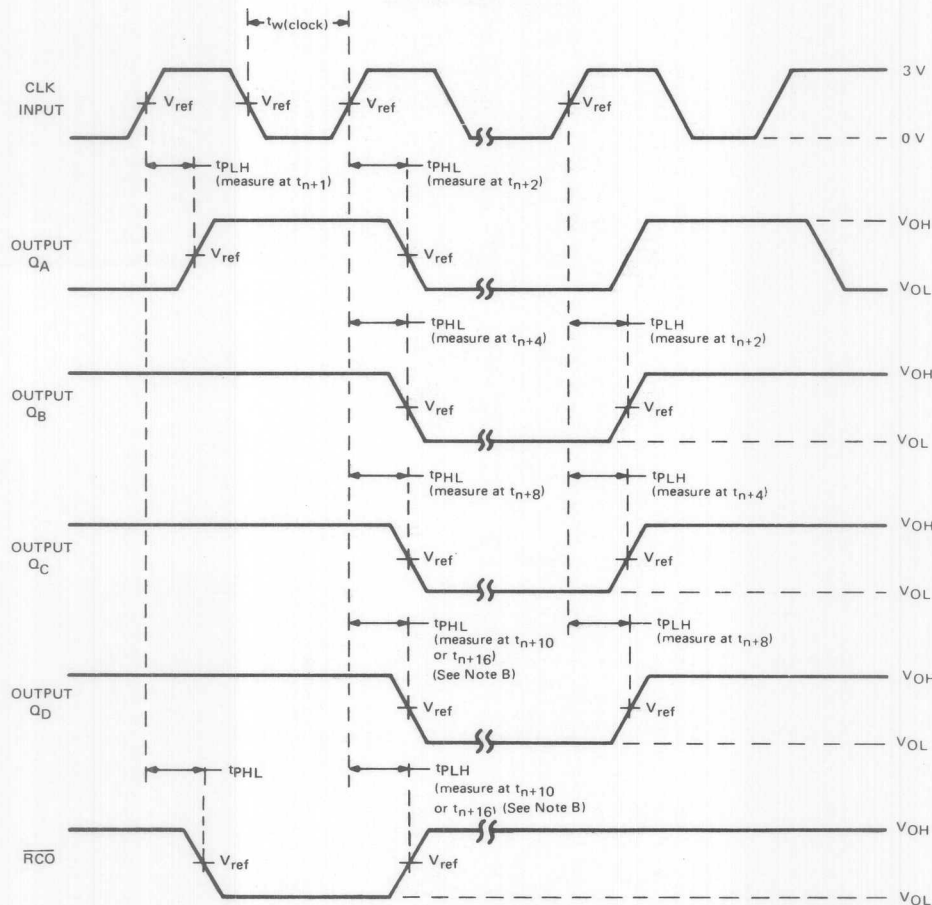
FIGURE 2—PROPAGATION DELAY TIMES TO CARRY OUTPUT

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TTL DEVICES

TYPES SN54LS169B, SN54S168, SN54S169,
SN74LS169B, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{out} \approx 50 \Omega$; for 'LS169B, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$; and for 'S168 and 'S169, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$. Vary PRR to measure f_{max} .
- B. Outputs Q_D and carry are tested at t_{n+10} for the 'S168 and at t_{n+16} for the 'LS169B and 'S169, where t_n is the bit-time when all outputs are low.
- C. For 'LS169B, $V_{ref} = 1.3 \text{ V}$; for 'S168 and 'S169, $V_{ref} = 1.5 \text{ V}$.

FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK

PARAMETER MEASUREMENT INFORMATION

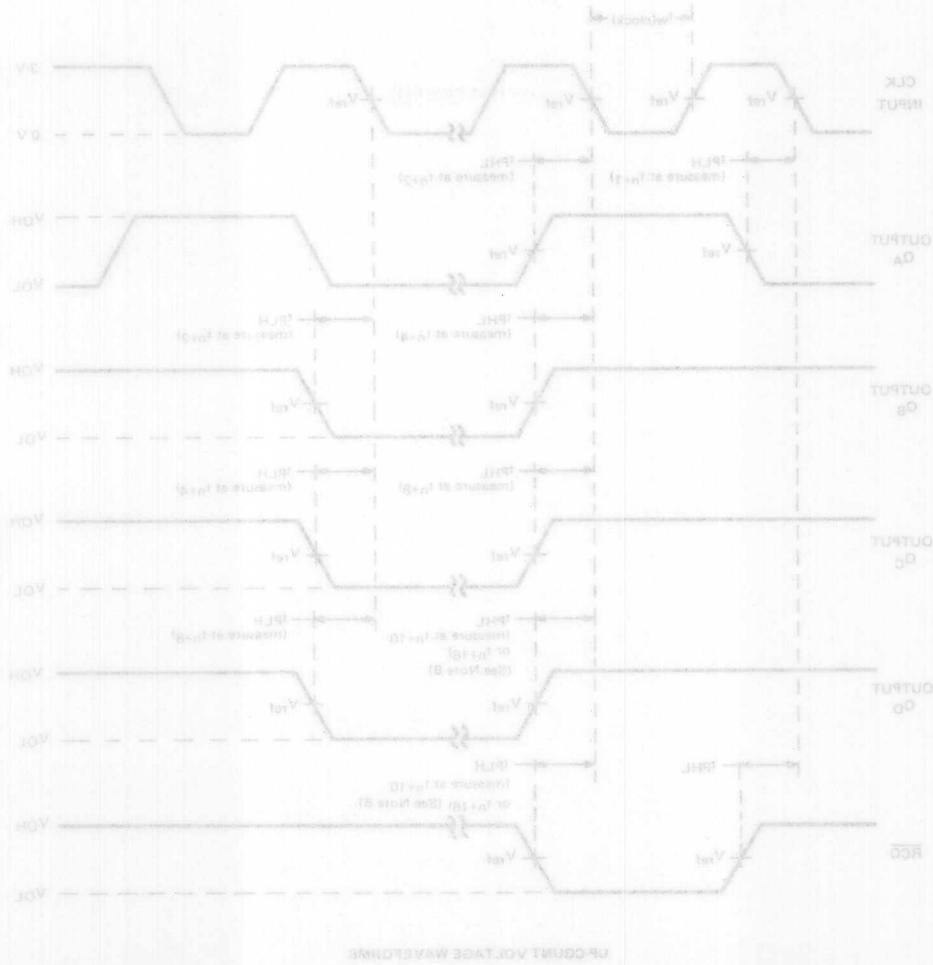


FIGURE 3-PROPAGATION DELAY TIMES FROM CLOCK

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TTL DEVICES

TYPES SN54170, SN54LS170, SN74170, SN74LS170

4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

MARCH 1974—REVISED DECEMBER 1983

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
Scratch-Pad Memory
Buffer Storage between Processors
Bit Storage in Fast Multiplication Designs
- Open-Collector Outputs with Low Maximum Off-State Current:
'170 . . . 30 μ A
'LS170 . . . 20 μ A
- SN54LS670 and SN74LS670 Are Similar But Have 3-State Outputs

description

The '170 and 'LS170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, \overline{G}_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, \overline{G}_R , is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

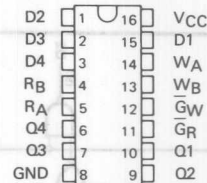
This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All '170 inputs and all inputs except the read enable and write enable of the 'LS170 are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54170 and SN54LS170 are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74170 and SN74LS170 are characterized for operation from 0°C to 70°C .

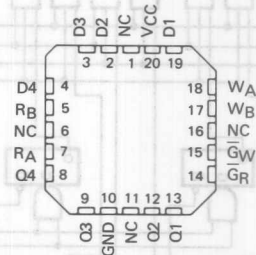
SN54170, SN54LS170 . . . J OR W PACKAGE
SN74170 . . . J OR N PACKAGE
SN74LS170 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS170 . . . FK PACKAGE
SN74LS170

(TOP VIEW)



NC - No internal connection

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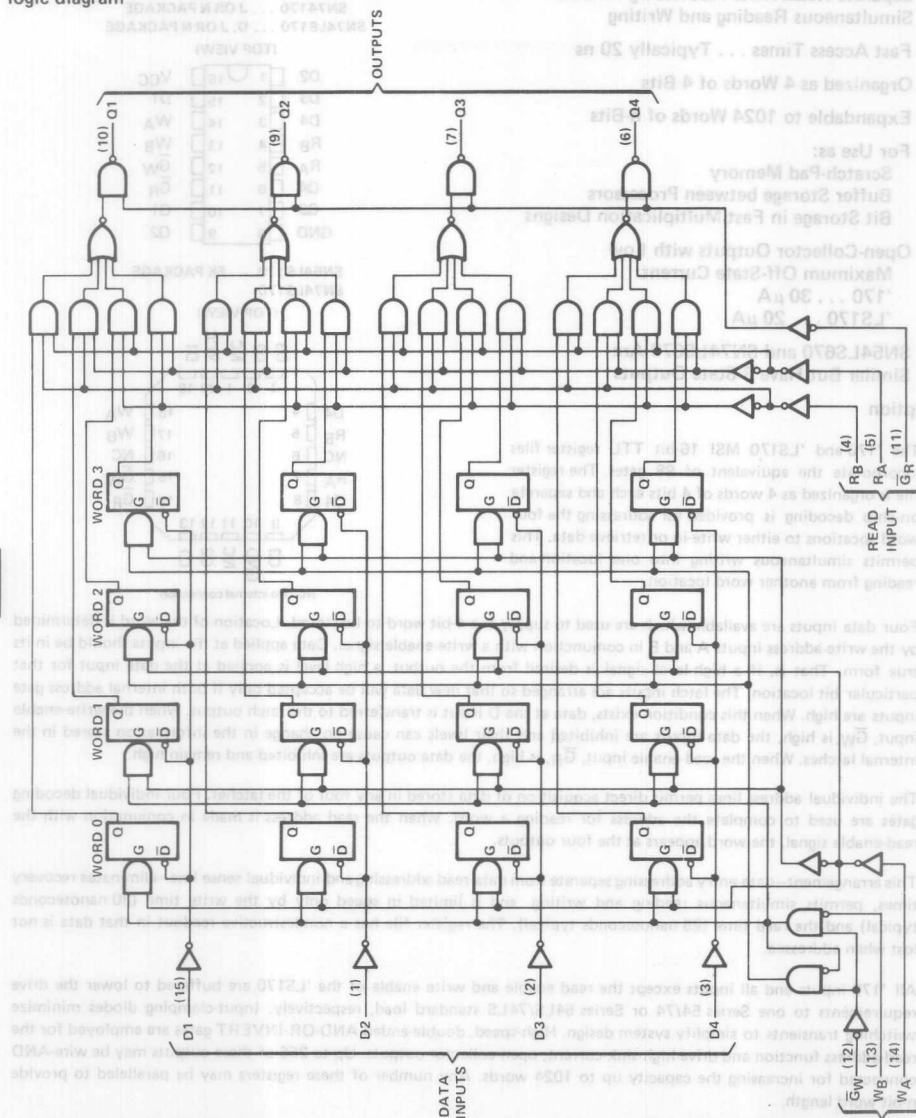
TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

logic diagram



DATA INPUTS

(1) D0 (2) D1 (3) D2 (4) D3 (5) D4 (6) D5 (7) D6 (8) D7 (9) D8 (10) D9 (11) D10 (12) D11 (13) D12 (14) D13 (15) D14 (16) D15

WRITE INPUT

WE

DATA INPUTS

(1) D0 (2) D1 (3) D2 (4) D3 (5) D4 (6) D5 (7) D6 (8) D7 (9) D8 (10) D9 (11) D10 (12) D11 (13) D12 (14) D13 (15) D14 (16) D15

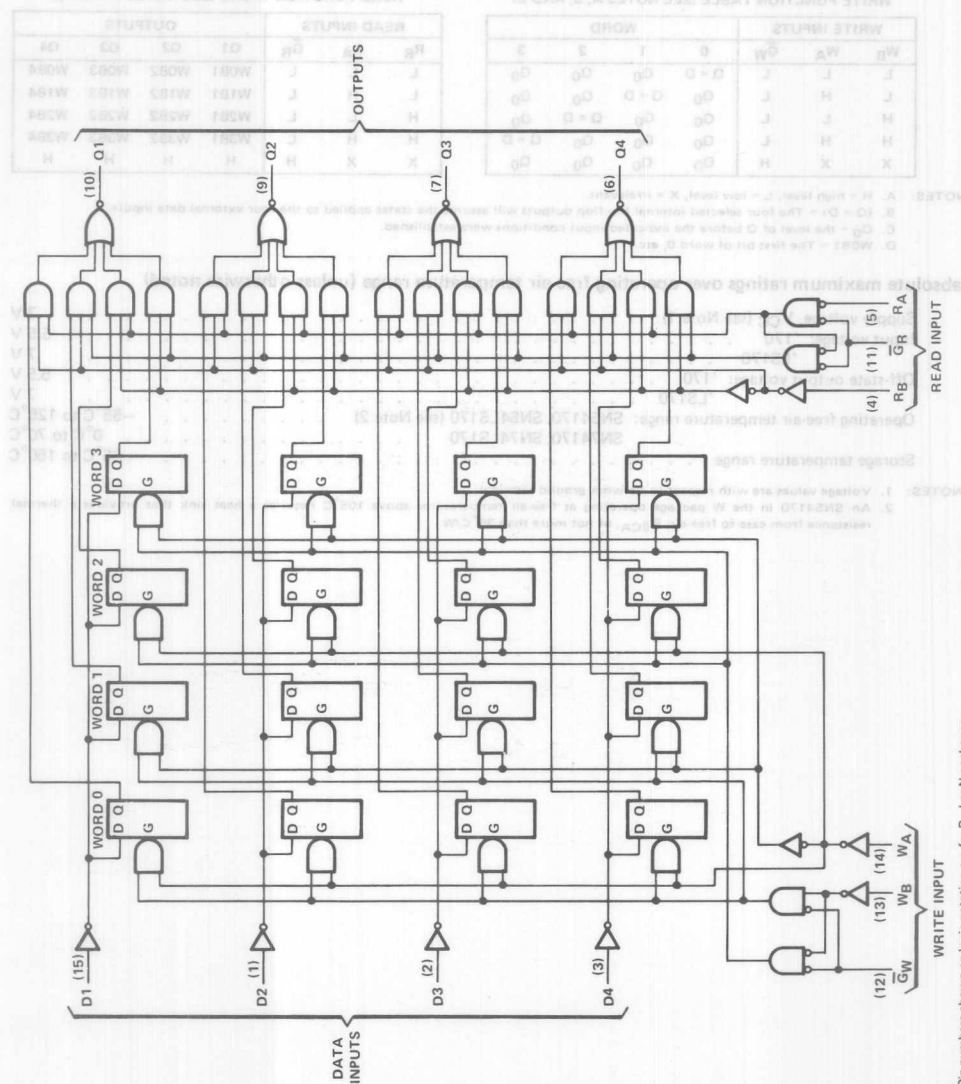
WRITE INPUT

WE

TTL DEVICES

TYPES SN54LS170, SN74LS170 4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

logic diagram



3 TTL DEVICES

Pin numbers shown on logic notation are for D, J or N packages.

3 TTL DEVICES

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

READ FUNCTION TABLE (SEE NOTES A AND D)

NOTES: A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q₀ = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

Supply voltage, V _{CC} (see Note 1)		7 V
Input voltage: '170		5.5 V
'LS170		7 V
Off-state output voltage: '170		5.5 V
'LS170		7 V
Operating free-air temperature range:	SN54170, SN54LS170 (see Note 2) SN74170, SN74LS170	-55°C to 125°C 0°C to 70°C
Storage temperature range		-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W

TYPES SN54170, SN74170 4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_W		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su}(D)$	10			10			ns
	Write select with respect to write enable, $t_{su}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_h(D)$	15			15			ns
	Write select with respect to write enable, $t_h(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A (see Note 2)		-55		125	0		70	°C

- NOTES: 2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W.
3. Write select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_h(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}$			30	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{SN54170}$		127§	140	mA
	See Note 5, SN74170		127§	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Typical supply current shown is an average for 50% duty cycle.

NOTE 5: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

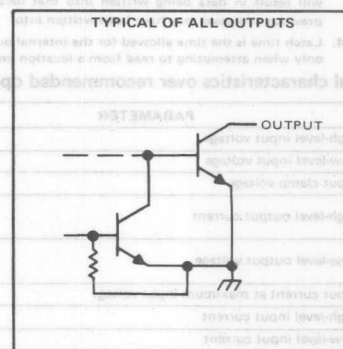
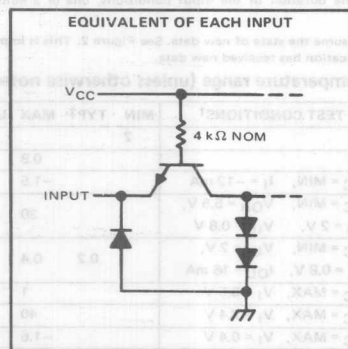
TYPES SN54170, SN74170 4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Figures 1 and 2	10	15	ns	
t_{PHL}				20	30		
t_{PLH}				23	35		
t_{PHL}	Read Select	Any Q	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Figures 1 and 3	30	40	ns	
t_{PLH}				25	40		
t_{PHL}				34	45		
t_{PLH}	Write enable	Any Q	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Figures 1 and 3	20	30	ns	
t_{PHL}				30	45		
t_{PLH}				30	45		

¹ t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

schematics of inputs and outputs



3
TTL DEVICES

TYPES SN54LS170, SN74LS170 4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54LS170			SN74LS170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su}(D)$	10			10			ns
	Write select with respect to write enable, $t_{su}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_h(D)$	15			15			ns
	Write select with respect to write enable, $t_h(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A		-55	125		0		70	°C

NOTES: 3. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_h(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS170			SN74LS170			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					-1.5			-1.5	V
I_{OH}	High-level output current		$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{IH} = 2 \text{ V}$					100			100	μA
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$			0.25	0.4		0.25	0.4	V
				$I_{OL} = 8 \text{ mA}$						0.35	0.5	
I_I	Input current at maximum input voltage	Any D, R, or W	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.1			0.1		mA
		$\overline{G_R}$ or $\overline{G_W}$					0.2			0.2		
I_{IH}	High-level input current	Any D, R, or W	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				20			20		μA
		$\overline{G_R}$ or $\overline{G_W}$					40			40		
I_{IL}	Low-level input current	Any D, R, or W	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.4			-0.4		mA
		$\overline{G_R}$ or $\overline{G_W}$					-0.8			-0.8		
I_{CC}	Supply current		$V_{CC} = \text{MAX},$ See Note 5			25	40		25	40		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 5: I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are ground, and all outputs are open.

3

TTL DEVICES

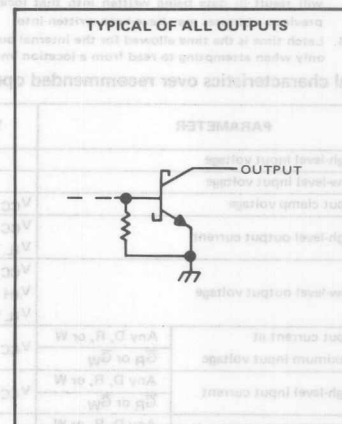
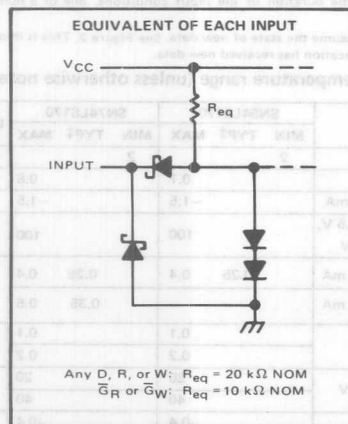
TYPES SN54LS170, SN74LS170 4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figures 1 and 2	20	30		ns
t_{PHL}				20	30		ns
t_{PLH}	Read select	Any Q	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figures 1 and 2	25	40		ns
t_{PHL}				24	40		ns
t_{PLH}	Write enable	Any Q	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figures 1 and 3	30	45		ns
t_{PHL}				26	40		ns
t_{PLH}	Data	Any Q	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figures 1 and 3	30	45		ns
t_{PHL}				22	35		ns

¹ t_{PLH} propagation delay time, low-to-high-level output
 t_{PHL} propagation delay time, high-to-low-level output

schematics of inputs and outputs



TYPES SN54170, SN54LS170, SN74170, SN74LS170 4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

PARAMETER MEASUREMENT INFORMATION

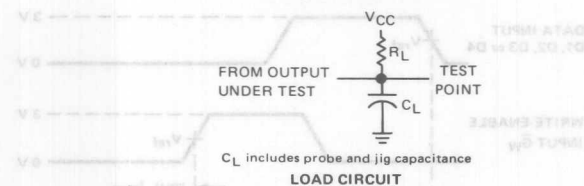
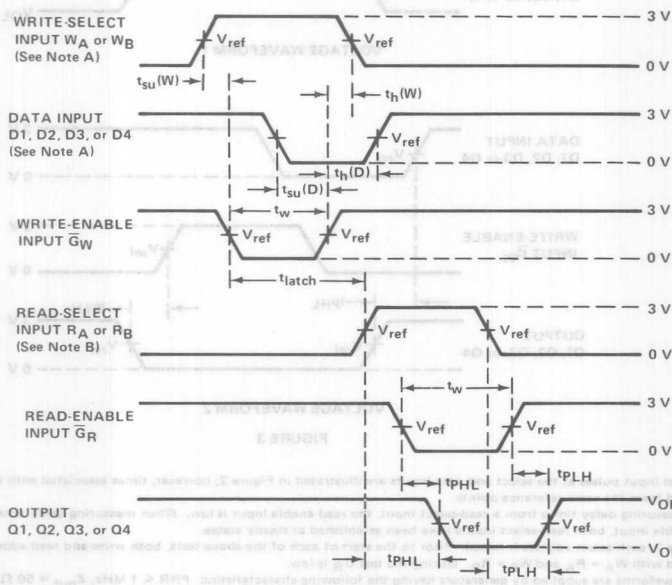


FIGURE 1



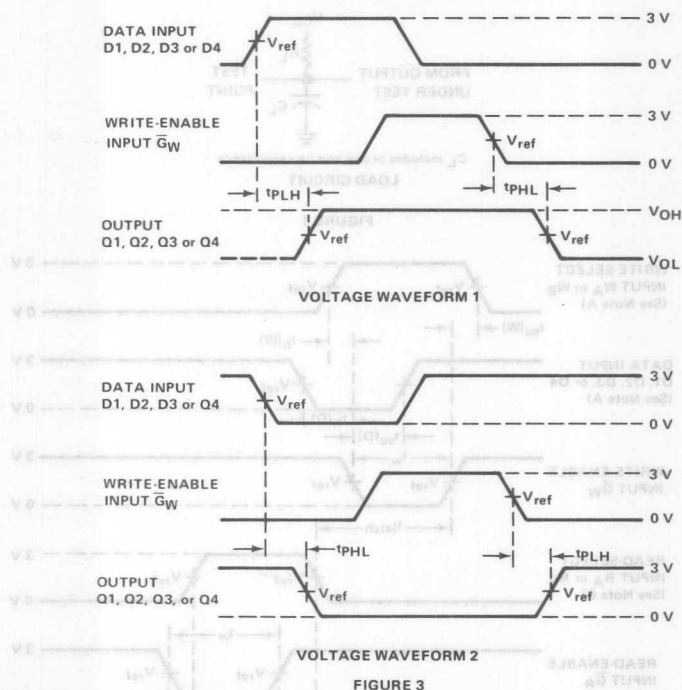
VOLTAGE WAVEFORMS

FIGURE 2

- NOTES:
- High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.
 - When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
 - In Figure 3, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test \bar{G}_R is low.
 - Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{OUT} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 10$ ns and $t_f \leq 10$ ns for '170, and $t_r \leq 15$ ns and $t_f \leq 6$ ns for 'LS170.
 - For '170, $V_{ref} = 1.5$ V; for 'LS170, $V_{ref} = 1.3$ V.

TYPES SN54170, SN54LS170, SN74170, SN74LS170
4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.
- B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
- C. In Figure 3, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
- D. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 10$ ns and $t_f \leq 10$ ns for '170, and $t_r \leq 15$ ns and $t_f \leq 6$ ns for 'LS170.
- E. For '170, $V_{ref} = 1.5$ V; for 'LS170, $V_{ref} = 1.3$ V.

3

TTL DEVICES

TYPES SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

REVISED DECEMBER 1983

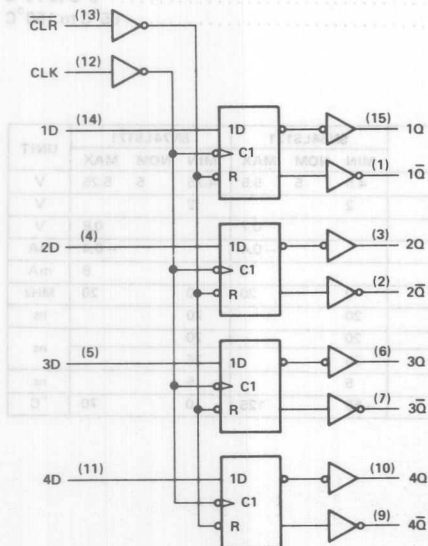
- Contains Four Flip-Flops with Double Rail Outputs
- Buffered Clock and Clear Inputs
- Individual Data Inputs to Each Flip-Flop

description

These monolithic, positive-edge triggered flip-flops utilize the latest low-power Schottky circuitry to implement D-type flip-flop logic. They have a direct clear input and complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

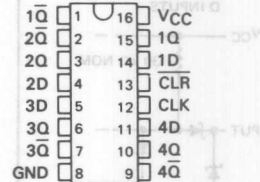
logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

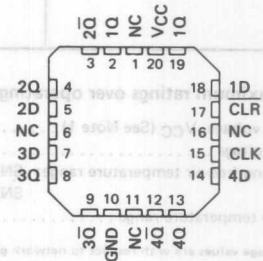
SN54LS171 ... J OR W PACKAGE
SN74LS171 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS171 ... FK PACKAGE
SN74LS171

(TOP VIEW)



NC-No internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

3

TTL DEVICES

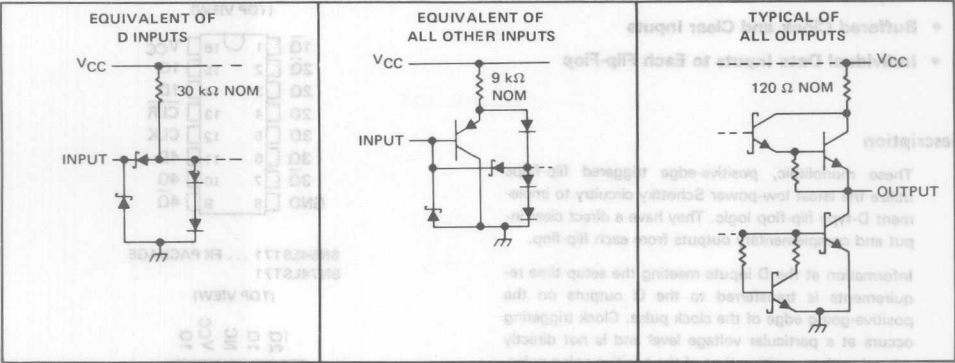
PRODUCTION DATA
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TEXAS
INSTRUMENTS

3-555

TYPES SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS171 Circuits	−55°C to 125°C
SN74LS171 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS171			SN74LS171			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0	20		0	20		MHz
t_w	Width of clock or clear pulse	20			20			ns
t_{su}	Setup time	20			20			ns
	Clear inactive-state	25			25			
t_h	Data hold time	5			5			ns
T_A	Operating free-air temperature	−55	125		0	70		°C

3

TTL DEVICES

TYPES SN54LS171, SN74LS171 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS171			SN74LS171			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	Input clamp voltage	V _{CC} = MIN, V _{IL} = MAX	I _I = − 18 mA			− 1.5			− 1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V, I _{OH} = − 1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX	V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I _{OL} = 8 mA				0.35	0.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				20			20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	D inputs All others			− 0.4			− 0.4	mA
					− 0.2			− 0.2	mA	
I _{OS} §	Short-circuit output current	V _{CC} = MAX, V _O = 0 V		− 20		− 100	− 20		− 100	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 1		14		25	14		25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS171			UNIT
				MIN	TYP	MAX	
f _{max}	CLK	Q, \overline{Q}	R _L = 2 kΩ, C _L = 15 pF	20	30		MHz
t _{PLH}					15	25	ns
t _{PHL}					18	30	ns
t _{PLH}				\overline{CLR}	Q		18
t _{PHL}		24				40	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

NOTE 3: See General Information Section for load circuit and voltage waveform.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TYPICAL	
				MIN	MAX
t_{PLH}	CLK	\overline{Q}	$R_L = 30 \Omega$ $C_L = 15 \text{ pF}$	20	30
t_{PLL}				15	25
t_{PHL}				15	25
t_{PLH}	CLR	\overline{Q}	$R_L = 30 \Omega$ $C_L = 15 \text{ pF}$	15	25
t_{PHL}				15	25

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$ (see note 2)

NOTE 1: t_{CC} is measured with all inputs grounded and all outputs open.
 2: Not more than one output should be asserted at a time and the duration of the high-impedance should not exceed one second.
 3: All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.
 4: For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER	TEST CONDITIONS	TYPICAL		TYPICAL	
		MIN	MAX	MIN	MAX
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 1	14	25	14	25
I_{OS} Short-circuit output current	$V_{CC} = \text{MAX}$, $V_O = 0 \text{ V}$	— 50	— 100	— 50	— 100
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	— 0.3	— 0.3	— 0.3	— 0.3
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	30		30	
i_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	0.1		0.1	
V_{OL} Low-level output voltage	$V_{CC} = \text{MAX}$, $V_{IH} = 2.7 \text{ V}$, $I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4
V_{OH} High-level output voltage	$V_{CC} = \text{MAX}$, $V_{IH} = 2.7 \text{ V}$, $I_{OH} = -1 \text{ mA}$	2.3	2.4	2.3	2.4
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -15 \text{ mA}$	— 1.5		— 1.5	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TYPE SN74172 16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

MAY 1972—REVISED APRIL 1985

- Independent Read/Write Addressing Permits Simultaneous Reading and Writing

- Organized as Eight Words of Two Bits Each

- Fast Access Times:
From Read Enable . . . 15 ns Typical
From Read Select . . . 33 ns Typical

- 3-State Outputs Simplify Use in Bus-Organized Systems

- Applications:

Stacked Data Registers
Scratch-Pad Memory
Buffer Storage Between Processors
Fast Multiplication Schemes

description

The SN74172, containing the equivalent of 201 gates on a monolithic chip, is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections (see Figure 1).

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

- 1) Writing new data into two bits
- 2) Reading from two bits
- 3) Writing into and simultaneously reading from the same two bits.

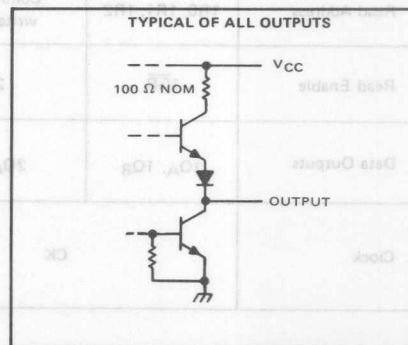
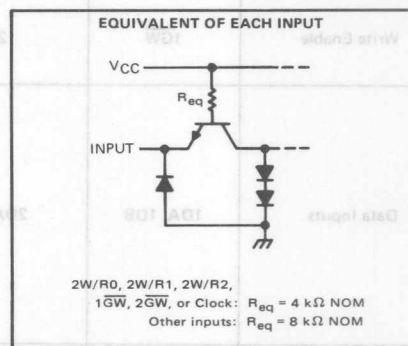
Regardless of the mode, the operation of section 2 is entirely independent of section 1.

SN74172 . . . J OR N PACKAGE

(TOP VIEW)

1W1	1	24	VCC
1W0	2	23	1W2
1GW	3	22	1DA
1DB	4	21	2DA
2DB	5	20	2GW
CLK	6	19	2W/R2
1R2	7	18	2W/R1
1R1	8	17	2W/R0
1R0	9	16	2GR
1QB	10	15	1GR
2QB	11	14	1QA
GND	12	13	2QA

schematics of inputs and outputs



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TEXAS
INSTRUMENTS

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TTL DEVICES

TYPE SN74172 16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

description (continued)

The three-state outputs of this register file permit connection of up to 129 compatible outputs and one Series 54/74 high-logic-level load to a common system bus. The outputs are controlled by the read-enable circuitry so that they operate as standard TTL totem-pole outputs when the appropriate read-enable input is low or they are placed in a high-impedance state when the associated read-enable input is at a high logic level. To minimize the possibility that two outputs from separate register files will attempt to take a common bus to opposite logic levels, the read-enable circuitry is designed such that disable times are shorter than enable times.

All inputs are buffered to lower the drive requirements of the clock, read/write address, and write-enable inputs to one normalized Series 54/74 load, and of all other inputs to one-half of one normalized Series 54/74 load.

Functions of the inputs and outputs of the SN74172 are as shown in the following table.

FUNCTION	SECTION 1	SECTION 2	DESCRIPTION
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA ≠ 2DA and/or 1DB ≠ 2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	1QA, 1QB	2QA, 2QB	
Clock		CK	The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

3

TTL DEVICES

TYPE SN74172 16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

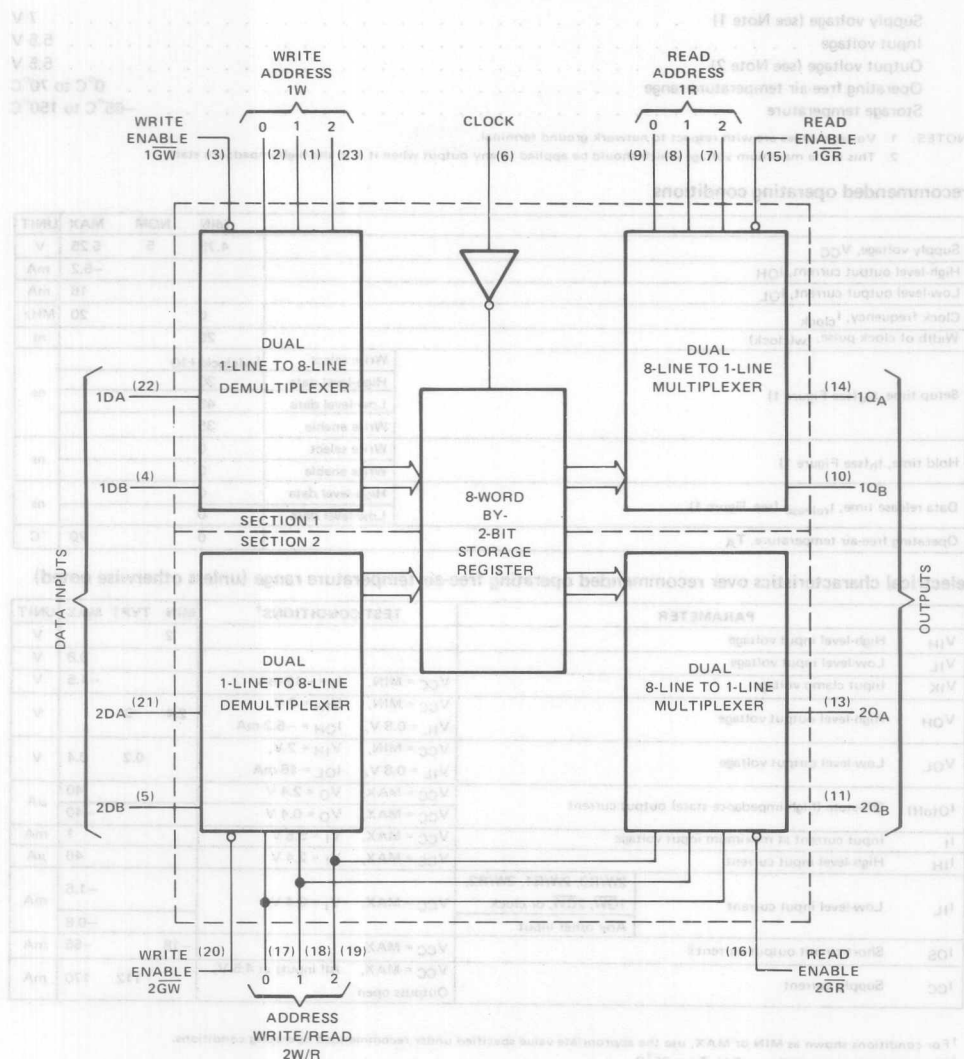


FIGURE 1

TYPE SN74172

16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Output voltage (see Note 2)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the high-impedance state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-5.2	mA
Low-level output current, I_{OL}			16	mA
Clock frequency, f_{clock}	0		20	MHz
Width of clock pulse, $t_w(\text{clock})$	25			ns
Setup time, t_{SU} (see Figure 1)	Write select	$t_w(\text{clock})+10$		ns
	High-level data	30		
	Low-level data	45		
	Write enable	35		
Hold time, t_H (see Figure 1)	Write select	0		ns
	Write enable	0		
Data release time, $t_{release}$ (see Figure 1)	High-level data	0		ns
	Low-level data	0		
Operating free-air temperature, T_A	0		70	°C

3

TTL DEVICES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -5.2 \text{ mA}$	2.4	3		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
$I_{O(\text{off})}$ Off-state (high-impedance state) output current	$V_{CC} = \text{MAX}, V_O = 2.4 \text{ V}$ $V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}$			40 -40	µA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	µA
I_{IL} Low-level input current	2W/R0, 2W/R1, 2W/R2, 1GW, 2GW, or clock			-1.6	mA
	Any other input			-0.8	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-18		-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ All inputs at 4.5 V, Outputs open		112	170	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

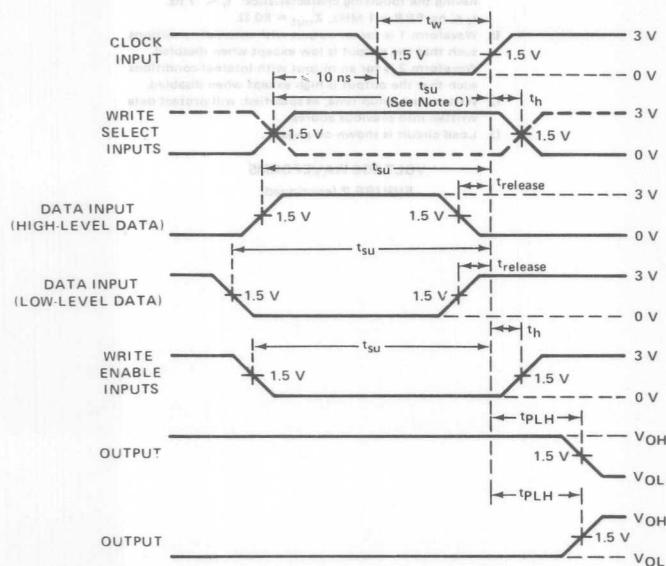
§ Not more than one output should be shorted at a time.

TYPE SN74172 16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 400\ \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max} Maximum clock frequency		20			MHz
t_{PLH} Propagation delay time, low-to-high-level output from read select	$C_L = 50\text{ pF}$, See Figure 2		33	45	ns
t_{PHL} Propagation delay time, high-to-low-level output from read select			30	45	
t_{PLH} Propagation delay time, low-to-high-level output from clock			35	50	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			35	50	
t_{PZH} Output enable time to high level			14	30	ns
t_{PZL} Output enable time to low level			16	30	
t_{PHZ} Output disable time from high level	$C_L = 5\text{ pF}$, See Figure 2		6	20	ns
t_{PLZ} Output disable time from low level			11	20	

PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES FROM CLOCK INPUT

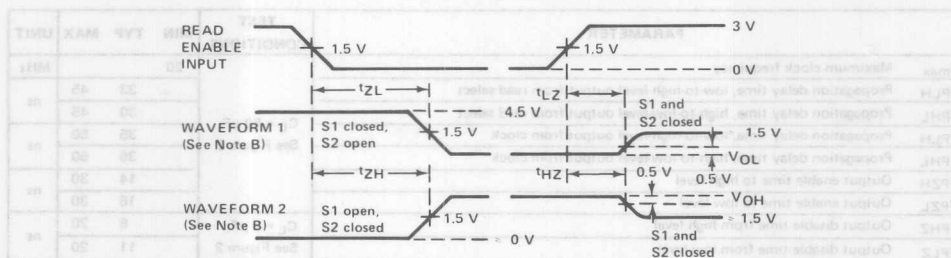
VOLTAGE WAVEFORMS

FIGURE 2

3

TTL DEVICES

PARAMETER MEASUREMENT INFORMATION

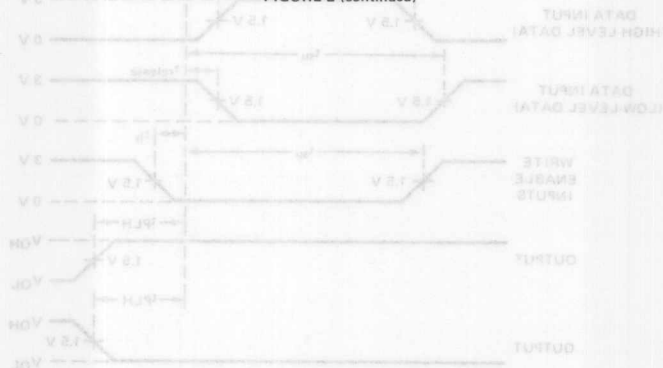


ENABLE AND DISABLE TIMES FROM READ ENABLE

- NOTES: A. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq$ ns, PRR = 1 MHz, $Z_{out} \approx 50 \Omega$.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled. Waveform 2 is for an output with internal conditions such that the output is high except when disabled.
 C. Write select setup time, as specified, will protect data written into previous address.
 D. Load circuit is shown on page .

VOLTAGE WAVEFORMS

FIGURE 2 (continued)



SWITCHING TIMES FROM CLOCK INPUT

VOLTAGE WAVEFORMS
FIGURE 2

TYPES SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

OCTOBER 1976—REVISED APRIL 1985

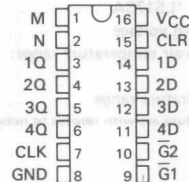
- 3-State Outputs Interface Directly with System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:

Parallel Load
Do Nothing (Hold)

- For application as Bus Buffer Registers

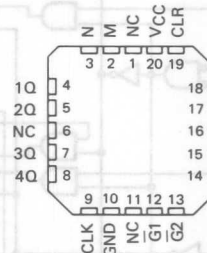
SN54173, SN54LS173A ... J OR W PACKAGE
SN74173 ... J OR N PACKAGE
SN74LS173A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS173A ... FK PACKAGE
SN74LS173A

(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'173	23 ns	35 MHz	250 mW
'LS173A	18 ns	50 MHz	95 mW

description

The '173 and 'LS173A four-bit registers include D-type flip-flops featuring totem-pole three-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs may be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

FUNCTION TABLE

CLEAR	CLOCK	INPUTS		DATA D	OUTPUT Q
		DATA ENABLE G1	DATA ENABLE G2		
H	X	X	X	X	L
L	L	X	X	X	Q ₀
L	↑	H	X	X	Q ₀
L	↑	X	H	X	Q ₀
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

3

TTL DEVICES

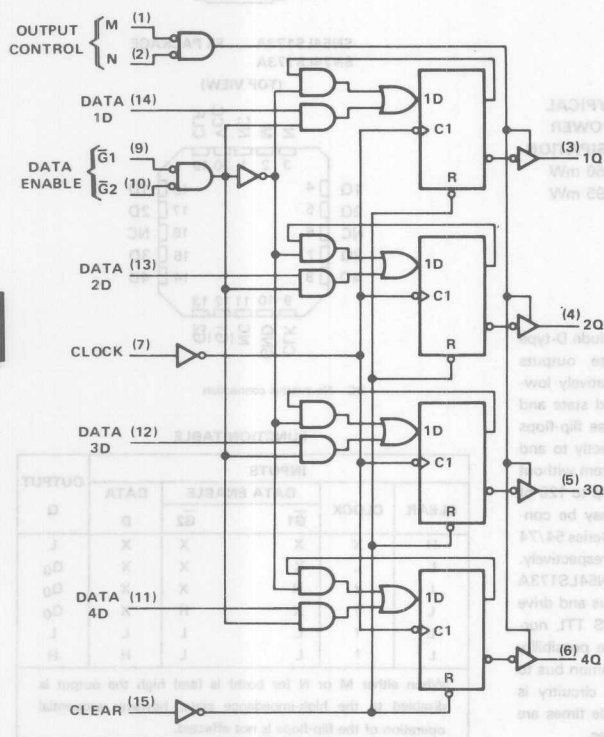
TYPE SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '173	5.5 V
'LS173A	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54173, SN54LS173A	-55°C to 125°C
SN74173, SN74LS173A	0°C to 70°C
Storage temperature range	-65°C to 150°C

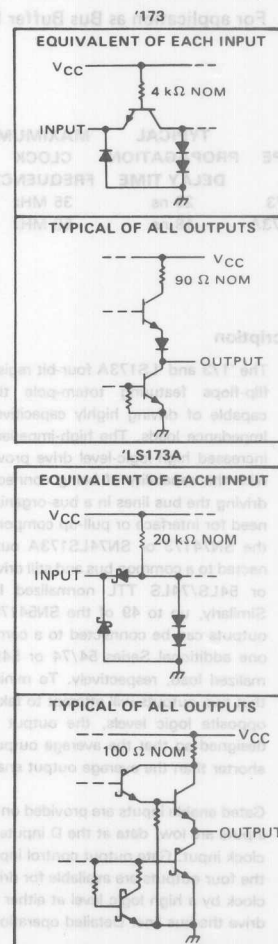
NOTE 1: Voltage values are with respect to network ground terminals.

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



TYPES SN54173, SN74173 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-2			-5.2	mA
Low-level output current, I_{OL}				16			16	mA
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_{WV}		20			20			ns
Setup time, t_{su}	Data enable	17			17			ns
	Data	10			10			
	Clear inactive state	10			10			
Hold time, t_h	Data enable	2			2			ns
	Data	10			10			
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$			0.4	V
$I_{O(\text{off})}$	Off-state (high-impedance state) output current	$V_{CC} = \text{MAX}, V_O = 2.4 \text{ V}$ $V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$		40	-40	µA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-70	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		50	72	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}, R_L = 400 \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input	$C_L = 50 \text{ pF}$		28	43	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input	See Note 3		19	31	
t_{PZH}	Output enable time to high level		7	16	30	ns
t_{PZL}	Output enable time to low level		7	21	30	
t_{PHZ}	Output disable time from high level	$C_L = 5 \text{ pF}$	3	5	14	ns
t_{PLZ}	Output disable time from low level	See Note 3	3	11	20	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS173A, SN74LS173A

4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54LS173A			SN74LS173A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			12			24	mA
Input clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, t_w	25			25			ns
Setup time, t_{su}	Data enable	35		35			ns
	Data	17		17			
	Clear inactive state	10		10			
Hold time, t_h	Data enable	0		0			ns
	Data	3		3			
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS173A			SN74LS173A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.1		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}, I_{OL} = 24 \text{ mA}$		0.25	0.4		0.25	0.4	V
$I_{O(off)}$ Off-state (high-impedance state) output current	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}, V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$		20			20		µA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		µA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30	-130		-30	-130		mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	19	30		19	24		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}, R_L = 667 \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		30	50		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear input			26	35	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock input	$C_L = 45 \text{ pF},$		17	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock input	See Note 3		22	30	
t_{PZH} Output enable time to high level			15	23	ns
t_{PZL} Output enable time to low level			18	27	
t_{PHZ} Output disable time from high level	$C_L = 5 \text{ pF},$		11	20	ns
t_{PLZ} Output disable time from low level	See Note 3		11	17	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

DECEMBER 1972—REVISED DECEMBER 1983

'174, 'LS174, 'S174 ... HEX D-TYPE FLIP-FLOPS

'175, 'LS175, 'S175 ... QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q_0 = the level of Q before the indicated steady-state input conditions were established.

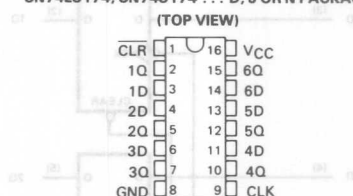
† = '175, 'LS175, and 'S175 only.

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY PER FLIP-FLOP	POWER DISSIPATION
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

SN54174, SN54LS174, SN54S174 ... J OR W PACKAGE

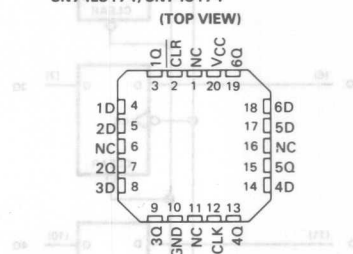
SN74174 ... J OR N PACKAGE

SN74LS174, SN74S174 ... D, J OR N PACKAGE



SN54LS174, SN54S174 ... FK PACKAGE

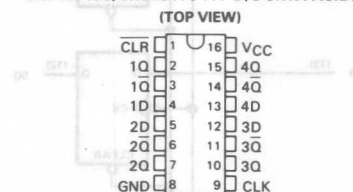
SN74LS174, SN74S174



SN54175, SN54LS175, SN54S175 ... J OR W PACKAGE

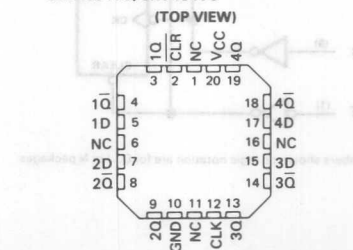
SN74175 ... J OR N PACKAGE

SN74LS175, SN74S175 ... D, J OR N PACKAGE



SN54LS175, SN54S175 ... FK PACKAGE

SN74LS175, SN74S175



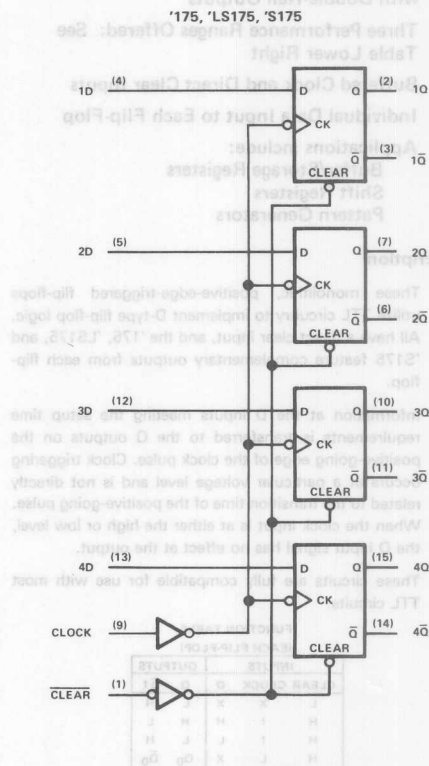
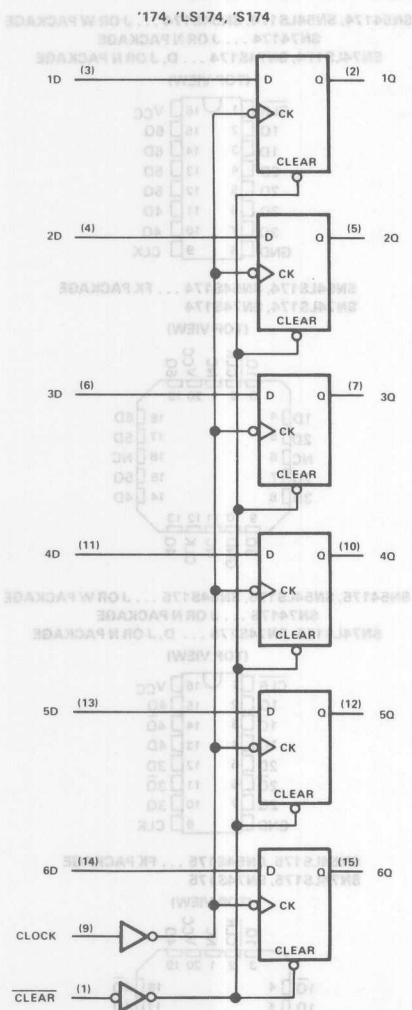
NC - No internal connection

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

**TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175,
SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

logic diagrams



3 TTL DEVICES

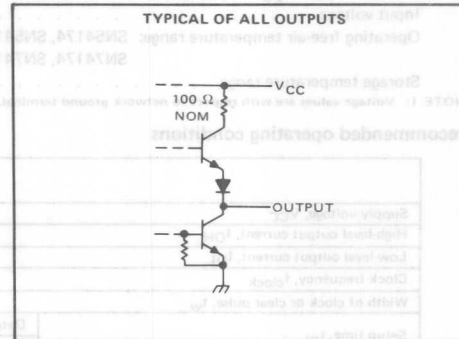
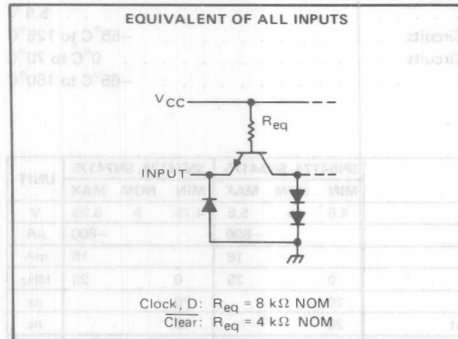
3-570

**TEXAS
INSTRUMENTS**

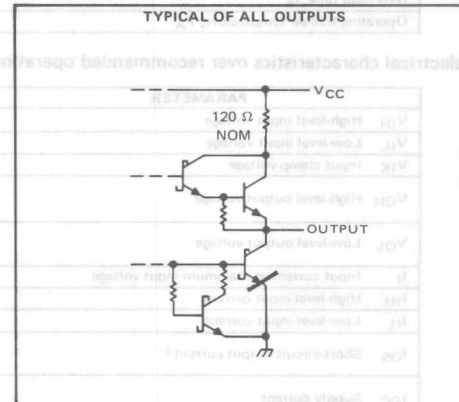
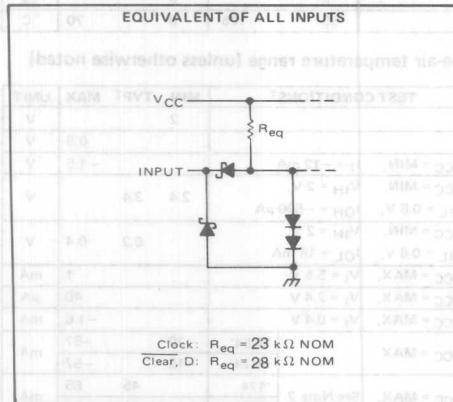
TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175,
SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

schematics of inputs and outputs

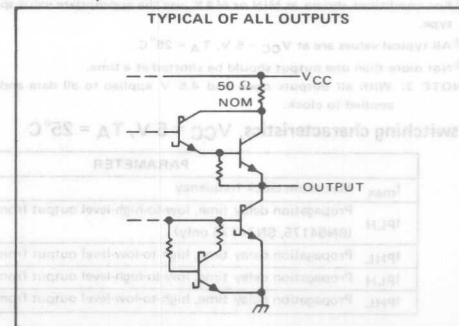
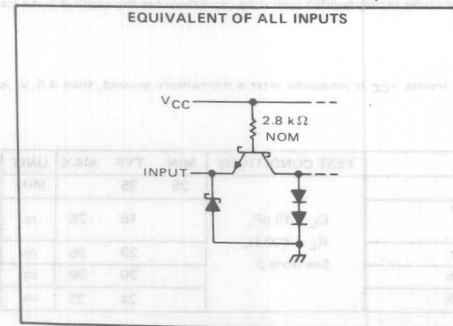
SN54174, SN54175, SN74174, SN74175



SN54LS174, SN54LS175, SN74LS174, SN74LS175



SN54S174, SN54S175, SN74S174, SN74S175



3

TTL DEVICES

TYPES SN54174, SN54175, SN74174, SN74175 HEXQUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54174, SN54175 Circuits	-55°C to 125°C
SN74174, SN74175 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54174, SN54175			SN74174, SN74175			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W	20		20				ns
Setup time, t_{SU}	Data input			20		20	ns
	Clear inactive-state			25		25	ns
Data hold time, t_H	5		5				ns
Operating free-air temperature, T_A	-55	125	0	70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54' -20 SN74' -18		-57 -57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	'174 '175	45 30	65 45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	35		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clear (SN54175, SN74175 only)	$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Note 3}$		16	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			24	35	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS174, SN54LS175, SN74LS174, SN74LS175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS174, SN54LS175 Circuits	-55°C to 125°C
SN74LS174, SN74LS175 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20		ns
Setup time, t_{su}	Data input			20			ns
	Clear inactive-state			25			ns
Data hold time, t_h	5			5			ns
Operating free-air temperature, T_A	-55			0			70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{IL} = V_{ILmax}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	'LS174	16	26	16	26		mA
		'LS175	11	18	11	18		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	'LS174			'LS175			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{max} Maximum clock frequency		30	40		30	40		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clear	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$				20	30		ns
t_{PHL} Propagation delay time, high-to-low-level output from clear		23	35		20	30		ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Note 3	20	30		13	25		ns
t_{PHL} Propagation delay time, high-to-low-level output from clock		21	30		16	25		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S174, SN54S175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S174, SN54S175 Circuits	-55°C to 125°C
SN74S174, SN74S175 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S174, SN54S175			SN74S174, SN74S175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		75	0		75	MHz
Pulse width, t_W	Clock	7			7			ns
	Clear	10			10			
Setup time, t_{SU}	Data input	5			5			ns
	Clear inactive-state	5			5			
Data hold time, t_H		3			3			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		V
	SN54S' SN74S'	2.7	3.4		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		90	144	mA
		'174 '175	60	96	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		75	110		MHz
t_{PLH} Propagation delay time, low-to-high-level Q output from clear (SN54S175, SN74S175 only)	$C_L = 15 \text{ pF}, R_L = 280 \Omega, \text{ See Note 3}$		10	15	ns
t_{PHL} Propagation delay time, high-to-low-level Q output from clear			13	22	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL} Propagation time, high-to-low-level output from clock			11.5	17	ns

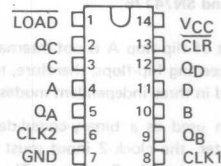
NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54176, SN54177, SN74176, SN74177 35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

MAY 1971—REVISED DECEMBER 1983

- Reduced-Power Versions of SN54196, SN54197, SN74196, and SN74197 50-MHz Counters
- D-C Coupled Counters Designed to Replace Signetics 8280, 8281, 8290, and 8291 Counters in Most Applications
- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 35 MHz
- Input Clamping Diodes Simplify System Design

SN54176, SN54177 . . . J OR W PACKAGE
SN74176, SN74177 . . . J OR N PACKAGE
(TOP VIEW)



description

These high-speed monolithic counters consist of four d-c coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54176, SN74176) or a divide-by-two and a divide-by-eight counter (SN54177, SN74177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The circuits are compatible with most TTL logic families. Typical power dissipation is 150 milliwatts. The SN54176 and SN54177 circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74176 and SN74177 circuits are characterized for operation from 0°C to 70°C .

3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-575

TYPES SN54176, SN54177, SN74176, SN74177

35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

typical count configurations

SN54176 and SN74176

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

- When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at right.
- If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.

- For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B , Q_C , and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54177 and SN74177

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

- When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A , Q_B , Q_C , and Q_D outputs as shown in the function table at right.
- When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B , Q_C , and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

FUNCTION TABLES

SN54176, SN74176

DECADE (BCD)

(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

BI-QUINARY (5-2)

(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

FUNCTION TABLE

SN54177, SN74177

(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level

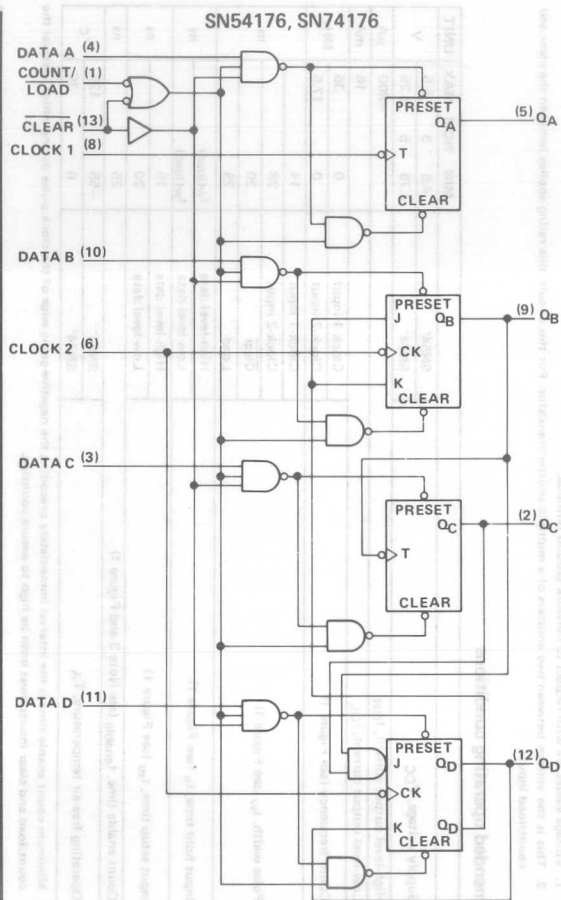
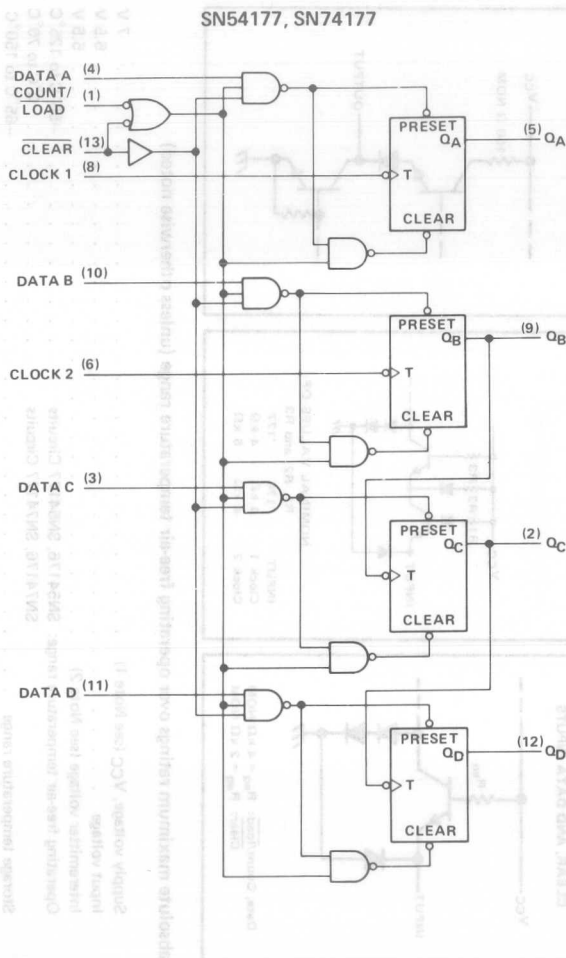
NOTE A: Output Q_A connected to clock-2 input.

3

TTL DEVICES

TYPES SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND
BINARY COUNTERS/LATCHES

logic diagrams



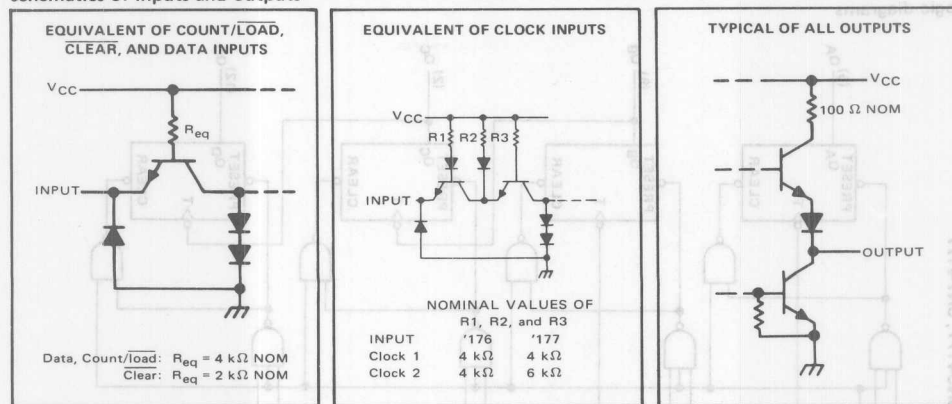
Pin numbers shown on logic notation are for J or N packages.

TTL DEVICES

3

TYPES SN54176, SN54177, SN74176, SN74177 35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54176, SN54177 Circuits	-55°C to 125°C
SN74176, SN74177 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54'	4.5	5	5.5	V
	SN74'	4.75	5	5.25	
High-level output current, I_{OH}				-800	μA
Low-level output current, I_{OL}				16	mA
Count frequency (see Figure 1)	Clock-1 input	0		35	MHz
	Clock-2 input	0		17.5	
Pulse width, t_w (see Figure 1)	Clock-1 input		14		ns
	Clock-2 input		28		
	Clear		20		
	Load		25		
Input hold time, t_h (see Figure 1)	High-level data	$t_{w(\text{load})}$			ns
	Low-level data	$t_{w(\text{load})}$			
Input setup time, t_{su} (see Figure 1)	High-level data	15			ns
	Low-level data	20			
Count enable time, t_{enable} (see Note 3 and Figure 1)			25		ns
Operating free-air temperature, T_A	SN54'	-55		125	°C
	SN74'	0		70	

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

3

TTL DEVICES

TYPES SN54176, SN54177, SN74176, SN74177 35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54176, SN74176			SN54177, SN74177			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	Data, count/load			40			40	µA
	Clear, clock 1			80			80	
	Clock 2			120			80	
I _{IL} Low-level input current	Data, count/load			-1.6			-1.6	mA
	Clear			-3.2			-3.2	
	Clock 1			-4.8			-4.8	
	Clock 2			-4.8			-3.2	
I _{OS} Short-circuit output current§	V _{CC} = MAX	SN54'	-20	-57	-20	-57		mA
		SN74'	-18	-57	-18	-57		
I _{CC} Supply current	V _{CC} = MAX, See Note 4		30	48		30	48	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, see figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54176, SN74176			SN54177, SN74177			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Clock 1	Q _A	35	50		35	50		MHz
t _{PLH}	Clock 1	O _A	8	13		8	13		ns
t _{PHL}			11	17		11	17		
t _{PLH}	Clock 2	Q _B	11	17		11	17		ns
t _{PHL}			17	26		17	26		
t _{PLH}	Clock 2	Q _C	27	41		27	41		ns
t _{PHL}			34	51		34	51		
t _{PLH}	Clock 2	Q _D	13	20		44	66		ns
t _{PHL}			17	26		50	75		
t _{PLH}	A, B, C, D	Q _A , Q _B , Q _C , Q _D	19	29		19	29		ns
t _{PHL}			31	46		31	46		
t _{PLH}	Load	Any	29	43		29	43		ns
t _{PHL}			32	48		32	48		
t _{PHL}	Clear	Any	32	48		32	48		ns

f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

TYPES SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND
BINARY COUNTERS/LATCHES

PARAMETER MEASUREMENT INFORMATION

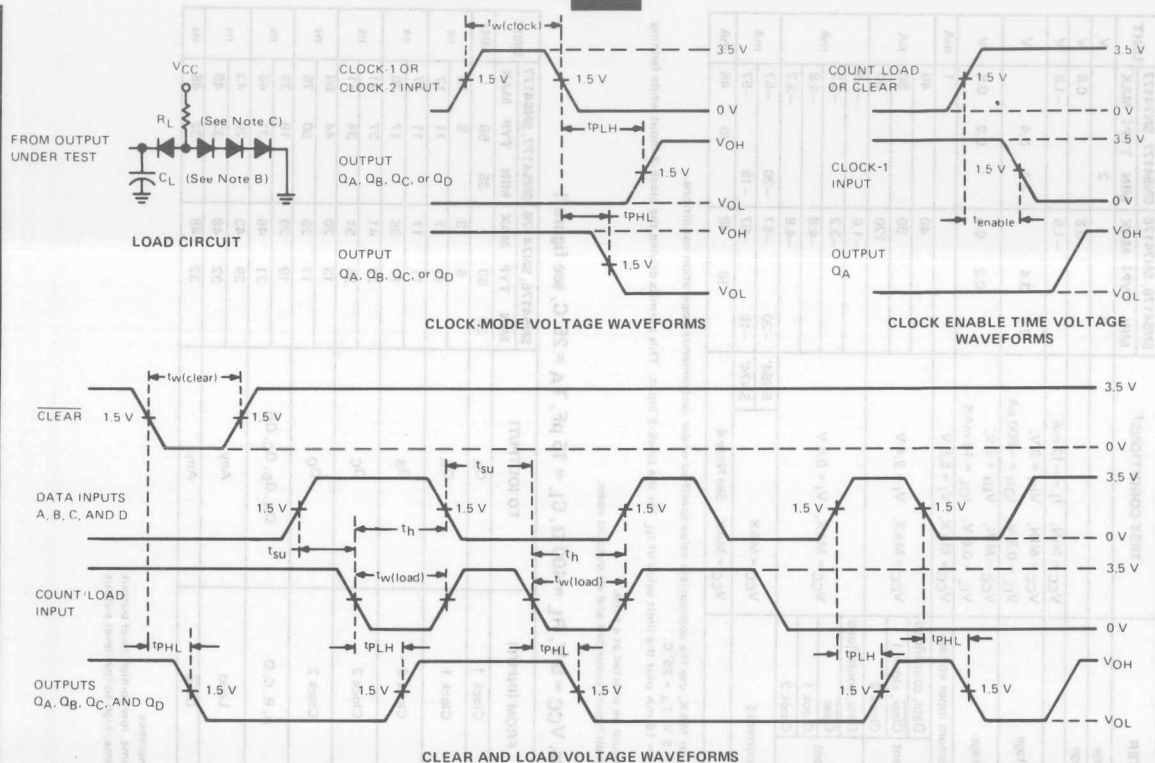


FIGURE 1

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $t_r < 5$ ns, and unless specified, $t_f < 5$ ns. When testing f_{max} , vary PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. Unless otherwise specified, Q_A is connected to clock 2.

TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

DECEMBER 1972—REVISED DECEMBER 1983

- Typical Maximum Clock Frequency . . . 39 MHz
- Three Operating Modes:
Synchronous Parallel Load
Right Shift
Hold (Do Nothing)
- Negative-Edge-Triggered Clocking
- D-C Coupling Simplifies System Designs

description

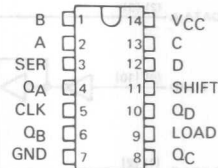
These shift registers utilize fully d-c coupled storage elements and feature synchronous parallel inputs and parallel outputs. The SN54179/SN74179 has a direct clear line and complementary output from the D flip-flop, thereby differing from the SN54178/SN74178.

Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is inhibited.

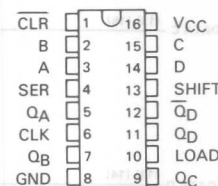
Shift right is also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input.

When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register.

SN54178 . . . J OR W PACKAGE
SN74178 . . . J OR N PACKAGE
(TOP VIEW)



SN54179 . . . J OR W PACKAGE
SN74179 . . . J OR N PACKAGE
(TOP VIEW)



'178, '179[†]
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR [†]	SHIFT	LOAD	CLOCK	SERIAL	PARALLEL				Q _A	Q _B	Q _C	Q _D	Q _D [†]
					A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	X	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	L	L	↓	X	a	b	c	d	a	b	c	d	d
H	H	X	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}
H	H	X	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}

[†]The columns for clear, QD, and the top line of the table apply for the '179 only.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↓ = transition from high to low level

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady state input conditions were established.

QA_n, QB_n, QC_n = the level of QA, QB, or QC, respectively, before the most-recent ↓ transition of the clock.

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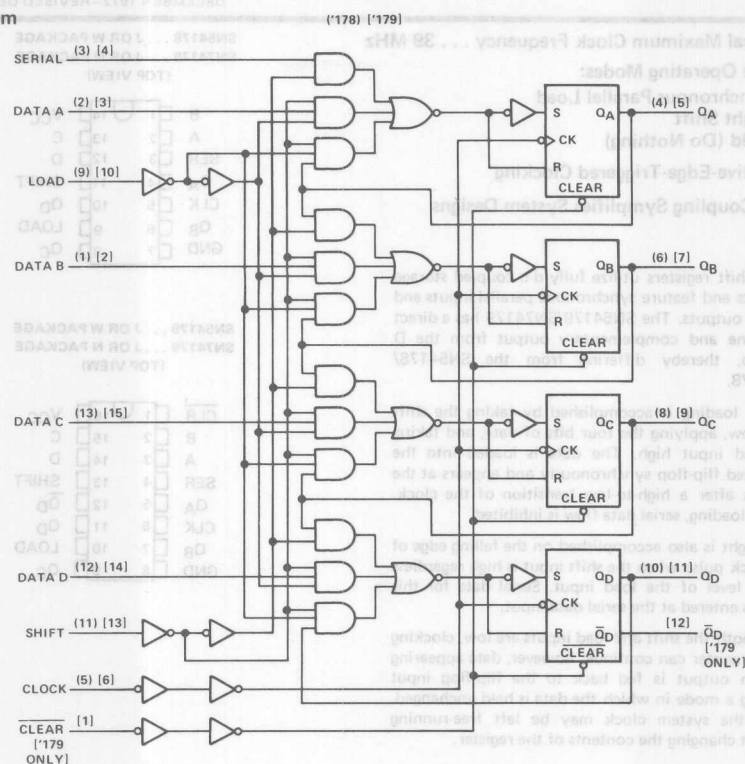
TEXAS
INSTRUMENTS

3

TTL DEVICES

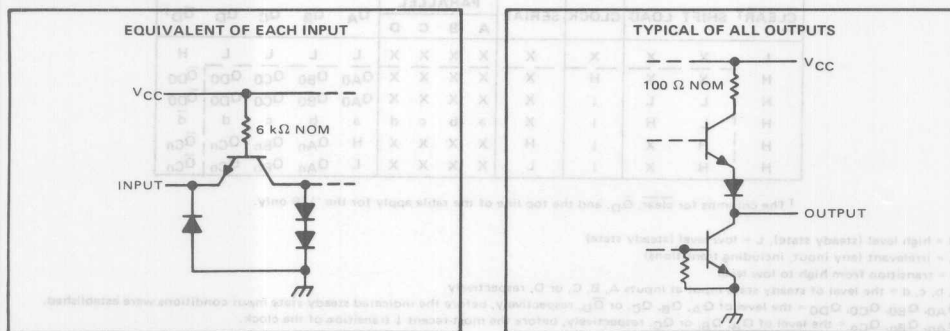
TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

logic diagram



Pin numbers shown on logic notation are for J or N packages.

schematics of inputs and outputs



TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54178, SN54179 Circuits	-55°C to 125°C
SN74178, SN74179 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54178, SN54179			SN74178, SN74179			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					-800			-800	μ A
Low-level output current, I_{OL}					16			16	mA
Clock frequency, f_{clock}			0		25	0		25	MHz
Width of clock or clear pulse, t_W (see Figure 1)			20			20			ns
Setup time, t_{SU} (see Figure 1)	Shift (H or L) or load		35			35			ns
	Data		30			30			
	Clear-inactive-state (SN54179 and SN74179)		15			15			
Hold time at any input, t_H			5			5			ns
Operating free-air temperature, T_A			-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54178, SN54179			SN74178, SN74179			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	46		70	46		75	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured as follows:

- 4.5 V is applied to serial inputs, load, shift, and clear,
- Parallel inputs A through D are grounded.
- 4.5 V is momentarily applied to clock which is then grounded.

TYPES SN54178, SN54179, SN74178, SN74179 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

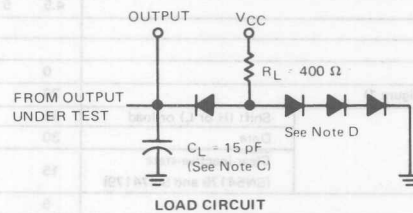
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	39		MHz
t _{PLH}	Clear	\overline{Q}_D	C _L = 15 pF, R _L = 400 Ω, See Figure 1		15	23	ns
t _{PHL}		Q _A , Q _B , Q _C , Q _D			24	36	
t _{PLH}	Clock	Any output			17	26	ns
t _{PHL}					23	35	

[†] f_{\max} = Maximum clock frequency

t_{PHL} = Propagation delay time, high-to-low-level output

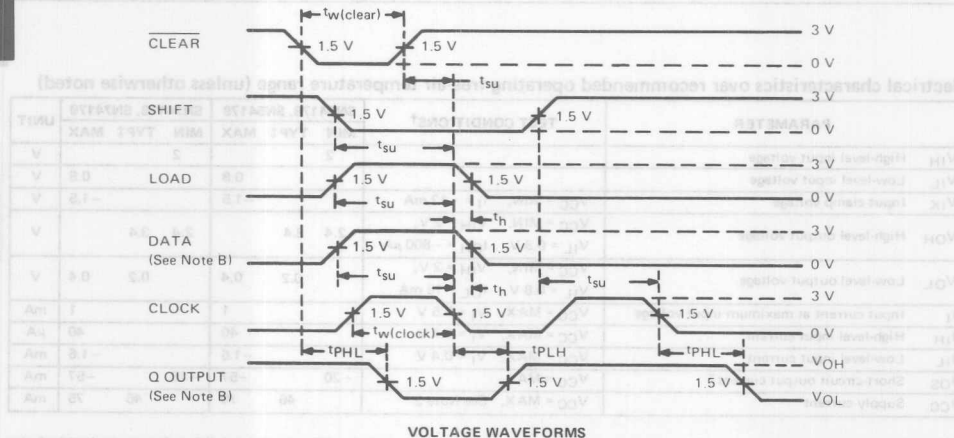
t_{PLH} = Propagation delay time, low-to-high-level output

PARAMETER MEASUREMENT INFORMATION



3

TTL DEVICES



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_{TLH} \leq 10\text{ ns}$, $t_{THL} \leq 10\text{ ns}$, $PRR \leq 1\text{ MHz}$, $Z_{out} \approx 50\ \Omega$.

B. Data input and Q output are any related pair. Serial and other data inputs are at GND. Serial data input is tested in conjunction with Q_A output in the shift mode.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES

TYPES SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

DECEMBER 1972—REVISED DECEMBER 1983

SN54180 . . . J OR W PACKAGE
SN74180 . . . J OR N PACKAGE
(TOP VIEW)

FUNCTION TABLE					
INPUTS			OUTPUTS		
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD	
EVEN	H	L	H	L	
ODD	H	L	L	H	
EVEN	L	H	L	H	
ODD	L	H	H	L	
X	H	H	L	L	
X	L	L	H	H	

H = high level, L = low level, X = irrelevant

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of -55°C to 125°C ; and the SN74180 is characterized for operation from 0°C to 70°C .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54180 Circuits	-55°C to 125°C
SN74180 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54180			SN74180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

TYPES SN54180, SN74180
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54180			SN74180			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.3		2.4	3.3		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	Any data input			40			40	µA
	Even or odd input			80			80	
I _{IL} Low-level input current	Any data input			-1.6			-1.6	mA
	Even or odd input			-3.2			-3.2	
I _{OS} Short-circuit output current§	V _{CC} = MAX	-20		-55	-18		-55	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2		34	49		34	56	mA

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Σ Even	C _L = 15 pF, R _L = 400 Ω, Odd input grounded, See Note 3	40	60		ns
t _{PHL}				45	68		
t _{PLH}	Data	Σ Odd	C _L = 15 pF, R _L = 400 Ω, Even input grounded, See Note 3	32	48		ns
t _{PHL}				25	38		
t _{PLH}	Data	Σ Even	C _L = 15 pF, R _L = 400 Ω, Even input grounded, See Note 3	32	48		ns
t _{PHL}				25	38		
t _{PLH}	Data	Σ Odd	C _L = 15 pF, R _L = 400 Ω, See Note 3	40	60		ns
t _{PHL}				45	68		
t _{PLH}	Even or Odd	Σ Even or Σ Odd	C _L = 15 pF, R _L = 400 Ω, See Note 3	13	20		ns
t _{PHL}				7	10		

NOTE 3: See General Information Section for load circuits and voltage waveforms.

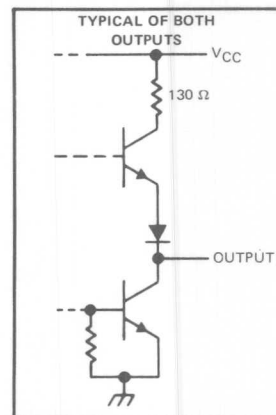
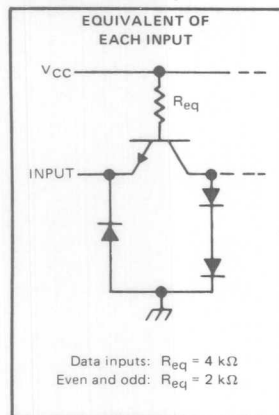
UNIT	SN54180			SN74180		
	MAX	NOM	MIN	MAX	NOM	MIN
V	4.75	5	4.75	4.75	5	4.75
A _u	100			100		
A _{vi}	10			10		
C	10			10		

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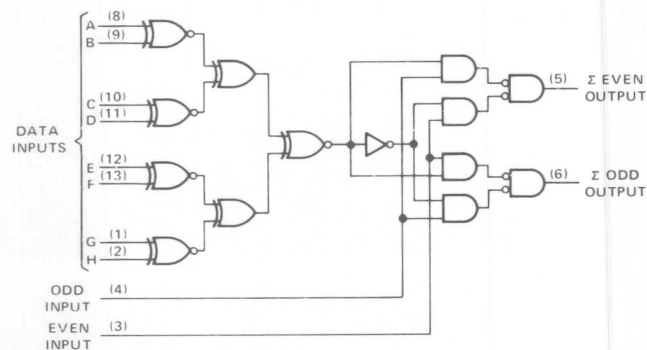
TTL DEVICES

TYPES SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

schematics of inputs and outputs



logic diagram

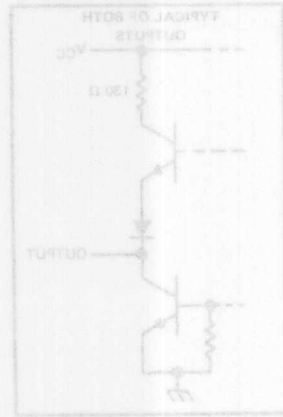
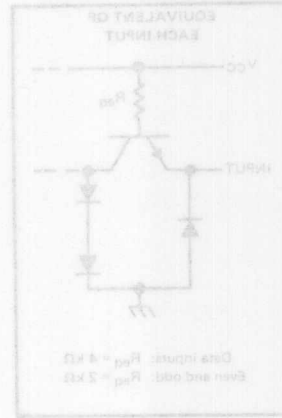


Pin numbers shown on logic notation are for J or N packages.

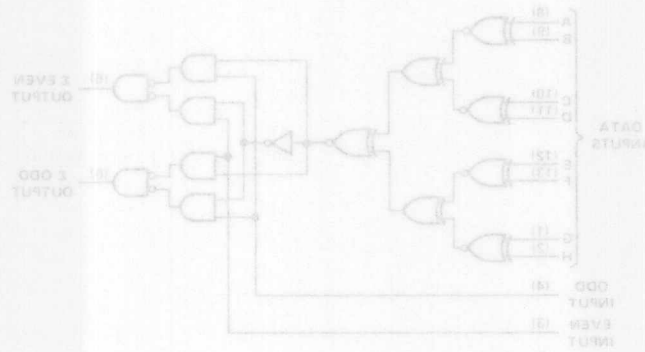
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TTL DEVICES

schematic of inputs and outputs



logic diagram



Pin numbers shown on logic diagram are for 14-pin package.

**TYPES SN54181, SN54LS181, SN54S181,
SN74181, SN74LS181, SN74S181**
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS
DECEMBER 1972 — REVISED DECEMBER 1983

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
 - Plus Ten Other Logic Operations

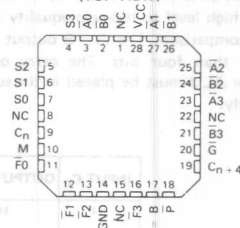
SN54181, SN54LS181, SN54S181 ... J OR W PACKAGE
SN74181 ... J OR N PACKAGE
SN74LS181, SN74S181 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS181, SN54S181 ... FK PACKAGE
SN74LS181, SN74S181

(TOP VIEW)



NC - No internal connection

TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALU's
	USING '181 AND '182	USING 'LS181 AND '182	USING 'S181 AND 'S182	ARITHMETIC/ LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	24 ns	24 ns	11 ns	1		NONE
5 to 8	36 ns	40 ns	18 ns	2		RIPPLE
9 to 16	36 ns	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	60 ns	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54182, SN54S182, SN74182, or SN74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading '182 or 'S182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

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**TEXAS
INSTRUMENTS**

3-589

3

TTL DEVICES

TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description (continued)

The '181, 'LS181, and 'S181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	A ₀	B ₀	A ₁	B ₁	A ₂	B ₂	A ₃	B ₃	F ₀	F ₁	F ₂	F ₃	C _n	C _{n+4}	P	G
Active-high data (Table 2)	A ₀	B ₀	A ₁	B ₁	A ₂	B ₂	A ₃	B ₃	F ₀	F ₁	F ₂	F ₃	C _n	C _{n+4}	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The '181, 'LS181, or 'S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F₀, F₁, F₂, F₃) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S₃, S₂, S₁, S₀ at L, H, H, L, respectively.

INPUT C _n	OUTPUT C _{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A > B	A < B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A < B	A > B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S₀, S₁, S₂, S₃) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, 74LS, and 74S devices are characterized for operation from 0°C to 70°C.

signal designations

The '181, 'LS181, and 'S181 together with the '182 and 'S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators (O) and the bars over the terminal letter symbols (e.g., C̄) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at C̄ means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

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TTL DEVICES

TYPES SN54181, SN54LS181, SN54S181,
SN74181, SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

signal designations (continued)

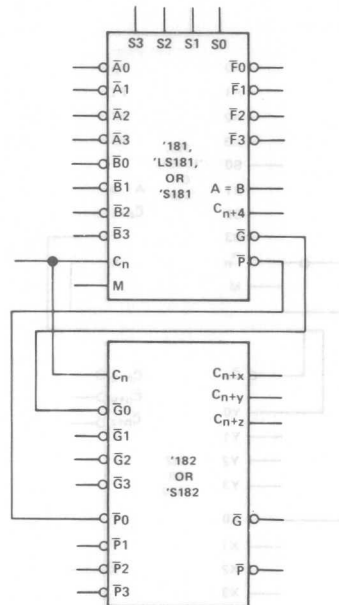


FIGURE 1

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	$F = \overline{A}$	$F = A \text{ MINUS } 1$	$F = A$
L	L	L	H	$F = \overline{AB}$	$F = AB \text{ MINUS } 1$	$F = AB$
L	L	H	L	$F = \overline{A + B}$	$F = \overline{AB} \text{ MINUS } 1$	$F = \overline{AB}$
L	L	H	H	$F = 1$	$F = \text{MINUS } 1 \text{ (2's COMP)}$	$F = \text{ZERO}$
L	H	L	L	$F = \overline{A + B}$	$F = A \text{ PLUS } (A + B)$	$F = A \text{ PLUS } (A + B) \text{ PLUS } 1$
L	H	L	H	$F = \overline{B}$	$F = AB \text{ PLUS } (A + B)$	$F = AB \text{ PLUS } (A + B) \text{ PLUS } 1$
L	H	H	L	$F = \overline{A \oplus B}$	$F = A \text{ MINUS } B \text{ MINUS } 1$	$F = A \text{ MINUS } B$
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + B) \text{ PLUS } 1$
H	L	L	L	$F = \overline{AB}$	$F = A \text{ PLUS } (A + B)$	$F = A \text{ PLUS } (A + B) \text{ PLUS } 1$
H	L	L	H	$F = A \oplus B$	$F = A \text{ PLUS } B$	$F = A \text{ PLUS } B \text{ PLUS } 1$
H	L	H	L	$F = B$	$F = \overline{AB} \text{ PLUS } (A + B)$	$F = \overline{AB} \text{ PLUS } (A + B) \text{ PLUS } 1$
H	L	H	H	$F = A + B$	$F = (A + B)$	$F = (A + B) \text{ PLUS } 1$
H	H	L	L	$F = 0$	$F = A$	$F = A \text{ PLUS } A \text{ PLUS } 1$
H	H	L	H	$F = \overline{AB}$	$F = \overline{AB} \text{ PLUS } A$	$F = \overline{AB} \text{ PLUS } A \text{ PLUS } 1$
H	H	H	L	$F = AB$	$F = \overline{AB} \text{ PLUS } A$	$F = \overline{AB} \text{ PLUS } A \text{ PLUS } 1$
H	H	H	H	$F = A$	$F = A$	$F = A \text{ PLUS } 1$

TYPES SN54181, SN54LS181, SN54S181,
SN74181, SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

signal designations (continued)

(baunifnoo) znoltsngizab limga

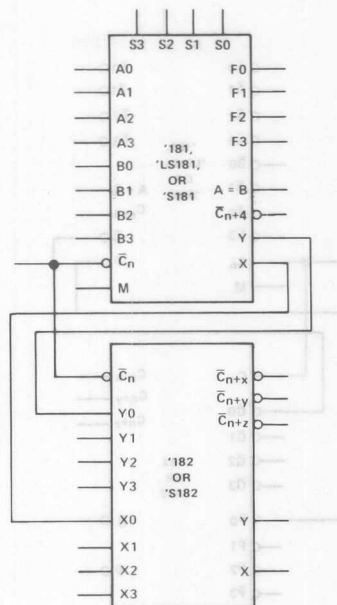


FIGURE 2

TABLE 2

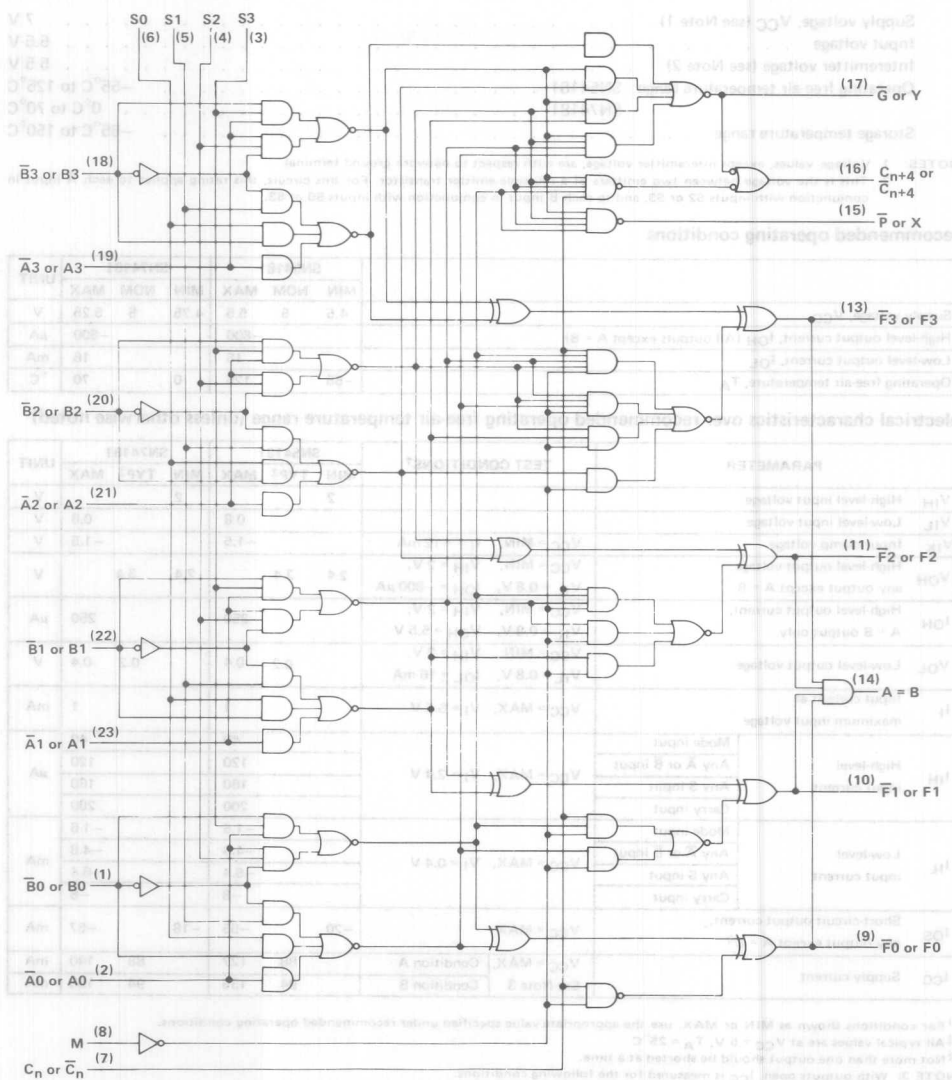
SELECTION					ACTIVE-HIGH DATA		
					M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\bar{C}_n = H$ (no carry)	$\bar{C}_n = L$ (with carry)	
L	L	L	L	$F = \bar{A}$	$F = A$	$F = A \text{ PLUS } 1$	
L	L	L	H	$F = A + B$	$F = A + B$	$F = (A + B) \text{ PLUS } 1$	
L	L	H	L	$F = \bar{A}B$	$F = A + \bar{B}$	$F = (A + B) \text{ PLUS } 1$	
L	L	H	H	$F = 0$	$F = \text{MINUS } 1 \text{ (2's COMPL)}$	$F = \text{ZERO}$	
L	H	L	L	$F = \bar{A}B$	$F = A \text{ PLUS } \bar{A}B$	$F = A \text{ PLUS } \bar{A}B \text{ PLUS } 1$	
L	H	L	H	$F = \bar{B}$	$F = (A + B) \text{ PLUS } \bar{A}B$	$F = (A + B) \text{ PLUS } \bar{A}B \text{ PLUS } 1$	
L	H	H	L	$F = A \oplus B$	$F = A \text{ MINUS } B \text{ MINUS } 1$	$F = A \text{ MINUS } B$	
L	H	H	H	$F = \bar{A}B$	$F = \bar{A}B \text{ MINUS } 1$	$F = \bar{A}B$	
H	L	L	L	$F = \bar{A} + B$	$F = A \text{ PLUS } AB$	$F = A \text{ PLUS } AB \text{ PLUS } 1$	
H	L	L	H	$F = A \oplus B$	$F = A \text{ PLUS } B$	$F = A \text{ PLUS } B \text{ PLUS } 1$	
H	L	H	L	$F = \bar{B}$	$F = (A + B) \text{ PLUS } AB$	$F = (A + B) \text{ PLUS } AB \text{ PLUS } 1$	
H	L	H	H	$F = AB$	$F = \bar{A}B \text{ MINUS } 1$	$F = \bar{A}B$	
H	H	L	L	$F = 1$	$F = A \text{ PLUS } A$	$F = A \text{ PLUS } A \text{ PLUS } 1$	
H	H	L	H	$F = A + \bar{B}$	$F = (A + B) \text{ PLUS } A$	$F = (A + B) \text{ PLUS } A \text{ PLUS } 1$	
H	H	H	L	$F = A + B$	$F = (A + B) \text{ PLUS } A$	$F = (A + B) \text{ PLUS } A \text{ PLUS } 1$	
H	H	H	H	$F = A$	$F = A \text{ MINUS } 1$	$F = A$	

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TTL DEVICES

TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram



Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54181, SN74181

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54181	-55°C to 125°C
SN74181	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each \bar{A} input in conjunction with inputs S2 or S3, and to each \bar{B} input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54181			SN74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54181			SN74181			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage, any output except A = B	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
I_{OH}	High-level output current, A = B output only	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250			250	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	Mode input			40			40	μA
		Any \bar{A} or \bar{B} input			120			120	
		Any S input			160			160	
		Carry input			200			200	
I_{IL}	Low-level input current	Mode input			-1.6			-1.6	mA
		Any \bar{A} or \bar{B} input			-4.8			-4.8	
		Any S input			-6.4			-6.4	
		Carry input			-8			-8	
I_{OS}	Short-circuit output current, any output except A = B §	$V_{CC} = \text{MAX}$	-20	-55		-18	-57	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{Condition A}$	88	127		88	140	mA	
		See Note 3, Condition B	94	135		94	150	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M, and \bar{A} inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

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TTL DEVICES

TYPES SN54181, SN74181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ ($C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, see note 4)

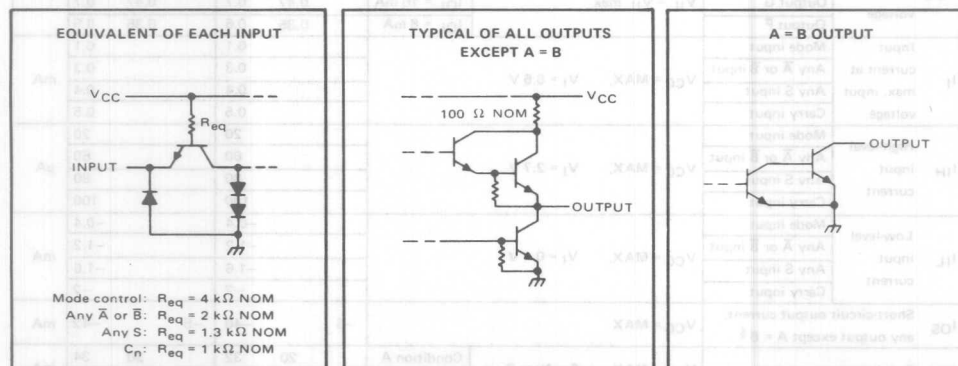
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}		12	18	ns	
t_{PHL}				13	19		
t_{PLH}	Any \bar{A} or \bar{B}	C_{n+4}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)	28	43	ns	
t_{PHL}				27	41		
t_{PLH}	Any \bar{A} or \bar{B}	C_{n+4}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)	35	50	ns	
t_{PHL}				33	50		
t_{PLH}	C_n	Any \bar{F}	$M = 0\text{ V}$ (SUM or DIFF mode)	13	19	ns	
t_{PHL}				12	18		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{G}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)	13	19	ns	
t_{PHL}				13	19		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{G}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)	17	25	ns	
t_{PHL}				17	25		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{P}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)	13	19	ns	
t_{PHL}				17	25		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{P}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)	17	25	ns	
t_{PHL}				17	25		
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)	28	42	ns	
t_{PHL}				21	32		
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)	32	48	ns	
t_{PHL}				23	34		
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 4.5\text{ V}$ (logic mode)	32	48	ns	
t_{PHL}				23	34		
t_{PLH}	Any \bar{A} or \bar{B}	$A = B$	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)	35	50	ns	
t_{PHL}				32	48		

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



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TTL DEVICES

TYPES SN54LS181, SN74LS181

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54LS181	-55°C to 125°C
SN74LS181	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each \bar{A} input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54LS181			SN74LS181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS181			SN74LS181			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage			0.7			0.8		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage, any output except A = B	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$		100			100		μ A
V_{OL}	Low-level output voltage	All outputs							V
		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$							
		Output G							
		Output P							
I_I	Input current at max. input voltage	Mode input			0.1			0.1	mA
		Any \bar{A} or \bar{B} input			0.3			0.3	
		Any S input			0.4			0.4	
		Carry input			0.5			0.5	
		Mode input			20			20	
I_{IH}	High-level input current	Any \bar{A} or \bar{B} input			60			60	μ A
		Any S input			80			80	
		Carry input			100			100	
		Mode input			-0.4			-0.4	
I_{IL}	Low-level input current	Any \bar{A} or \bar{B} input			-1.2			-1.2	mA
		Any S input			-1.6			-1.6	
		Carry input			-2			-2	
		Mode input			-6			-6	
I_{OS}	Short-circuit output current, any output except A = B §	$V_{CC} = \text{MAX}$	-6	-40		-5	-42		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3							mA
		Condition A	20	32		20	34		
		Condition B	21	35		21	37		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M, and \bar{A} inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

3

TTL DEVICES

TYPES SN54LS181, SN74LS181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, ($C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, see note 4)

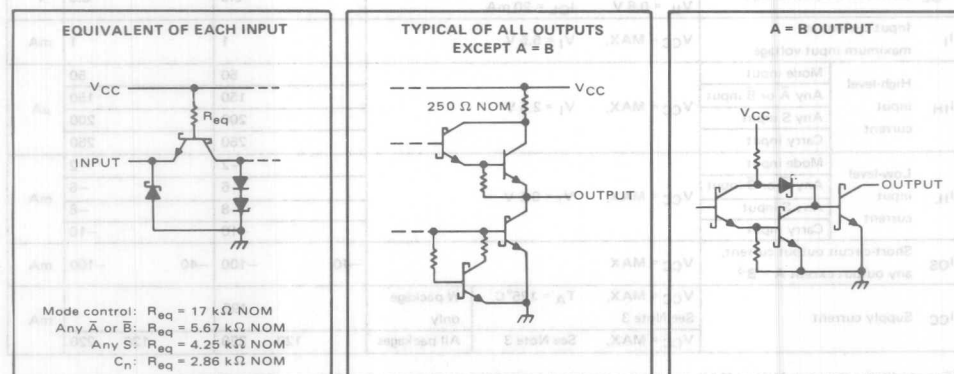
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}		18	27	ns	
t_{PHL}				13	20		
t_{PLH}	Any \bar{A} or \bar{B}	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)	25	38	ns	
t_{PHL}				25	38		
t_{PLH}	Any \bar{A} or \bar{B}	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	27	41	ns	
t_{PHL}				27	41		
t_{PLH}	C_n	Any F	M = 0 V (SUM or DIFF mode)	17	26	ns	
t_{PHL}				13	20		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{G}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)	19	29	ns	
t_{PHL}				15	23		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{G}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	21	32	ns	
t_{PHL}				21	32		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{P}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)	20	30	ns	
t_{PHL}				20	30		
t_{PLH}	Any \bar{A} or \bar{B}	\bar{P}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	20	30	ns	
t_{PHL}				22	33		
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)	21	32	ns	
t_{PHL}				13	20		
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	21	32	ns	
t_{PHL}				21	32		
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	M = 4.5 V (logic mode)	22	33	ns	
t_{PHL}				26	38		
t_{PLH}	Any \bar{A} or \bar{B}	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	33	50	ns	
t_{PHL}				41	62		

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



TYPES SN54S181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature: SN54S181	-55°C to 125°C
SN74S181	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For this circuit, this rating applies to each \bar{A} input in conjunction with inputs S2 or S3, and to each \bar{B} input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54S181			SN74S181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S181			SN74S181			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	High-level output voltage, any output except A = B	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250			250	µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.5 \text{ V}$			50			50	µA
	Mode input				150			150	
	Any \bar{A} or \bar{B} input				200			200	
	Any S input				250			250	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
	Mode input				-6			-6	
	Any \bar{A} or \bar{B} input				-8			-8	
	Any S input				-10			-10	
I_{OS}	Short-circuit output current, any output except A = B §	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, T_A = 125^\circ \text{C},$ W package only			195				mA
		$V_{CC} = \text{MAX},$ See Note 3 All packages	120	220		120	220		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured for the following conditions (the typical and maximum values apply to both):

- A. S0 through S3, M, and \bar{A} inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.
- B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.

TYPES SN54S181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ ($C_L = 15\text{ pF}$, $R_L = 280\ \Omega$, see note 4)

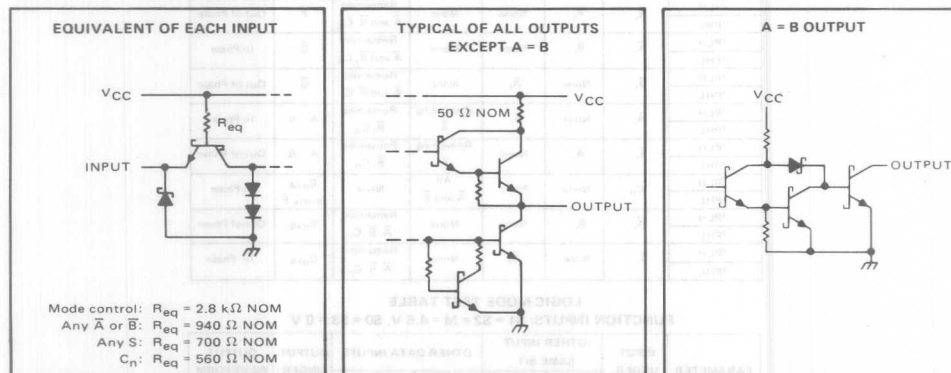
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			7	10.5	ns
t_{PHL}					7	10.5	ns
t_{PLH}	Any \bar{A} or \bar{B}	C_{n+4}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)		12.5	18.5	ns
t_{PHL}					12.5	18.5	ns
t_{PLH}	Any \bar{A} or \bar{B}	C_{n+4}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)		15.5	23	ns
t_{PHL}					15.5	23	ns
t_{PLH}	C_n	Any \bar{F}	$M = 0\text{ V}$ (SUM or DIFF mode)		7	12	ns
t_{PHL}					7	12	ns
t_{PLH}	Any \bar{A} or \bar{B}	\bar{G}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)		8	12	ns
t_{PHL}					7.5	12	ns
t_{PLH}	Any \bar{A} or \bar{B}	\bar{G}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)		10.5	15	ns
t_{PHL}					10.5	15	ns
t_{PLH}	Any \bar{A} or \bar{B}	\bar{P}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)		7.5	12	ns
t_{PHL}					7.5	12	ns
t_{PLH}	Any \bar{A} or \bar{B}	\bar{P}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)		10.5	15	ns
t_{PHL}					10.5	15	ns
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode)		11	16.5	ns
t_{PHL}					11	16.5	ns
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)		14	20	ns
t_{PHL}					14	22	ns
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 4.5\text{ V}$ (logic mode)		14	20	ns
t_{PHL}					14	22	ns
t_{PLH}	Any \bar{A} or \bar{B}	$A = B$	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode)		15	23	ns
t_{PHL}					20	30	ns

[†] t_{PLH} \equiv propagation delay time, low-to-high-level output

t_{PHL} \equiv propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5 \text{ V}$, $S_1 = S_2 = M = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PHL}	B_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i	In-Phase
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}	B_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PHL}	B_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}	In-Phase
t_{PLH}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C_{n+4}	In-Phase
t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}	B_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	C_{n+4}	Out-of-Phase

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5 \text{ V}$, $S_0 = S_3 = M = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i	In-Phase
t_{PHL}	B_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i	Out-of-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	In-Phase
t_{PHL}	B_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}	Out-of-Phase
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}	In-Phase
t_{PHL}	B_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}	Out-of-Phase
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	$A - B$	In-Phase
t_{PHL}	B_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	$A - B$	Out-of-Phase
t_{PLH}	C_n	None	None	All \bar{A} and \bar{B}	None	C_{n+4} or any \bar{F}	In-Phase
t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} , \bar{B} , C_n	C_{n+4}	Out-of-Phase
t_{PHL}	B_i	None	\bar{A}_i	None	Remaining \bar{A} , \bar{B} , C_n	C_{n+4}	In-Phase

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5 \text{ V}$, $S_0 = S_3 = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{F}_i	Out-of-Phase
t_{PHL}	B_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{F}_i	Out-of-Phase

NOTE 4: See General Information Section for load circuits and voltage waveforms.

3

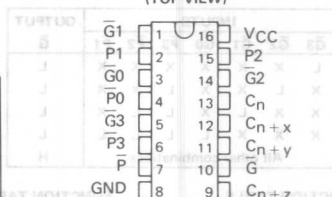
TTL DEVICES

TYPES SN54182, SN54S182, SN74182, SN74S182 LOOK-AHEAD CARRY GENERATORS

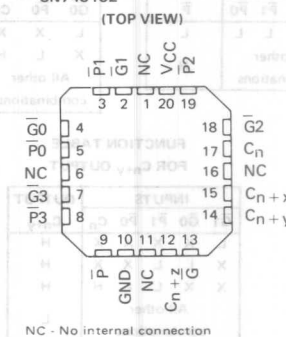
BULLETIN NO. DL-S 7611823, DECEMBER 1972 - REVISED OCTOBER 1976

- Directly Compatible for Use With:
SN54181/SN74181, SN54LS181/SN74LS181,
SN54S281/SN74S281, SN54S381, SN74S381,
SN54S481/SN74S481

SN54182, SN54S182 ... J OR W PACKAGE
SN74182 ... J OR N PACKAGE
SN74S182 ... D, J OR N PACKAGE
(TOP VIEW)



SN54S182 ... FK PACKAGE
SN74S182
(TOP VIEW)

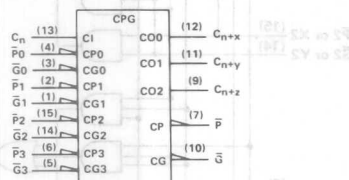


PIN DESIGNATIONS

ALTERNATIVE	DESIGNATIONS†	PIN NOS.	FUNCTION
G0, G1, G2, G3	G0, G1, G2, G3	3, 1, 14, 5	CARRY GENERATE INPUTS
P0, P1, P2, P3	P0, P1, P2, P3	4, 2, 15, 6	CARRY PROPAGATE INPUTS
C _n	C _n	13	CARRY INPUT
C _{n+x} , C _{n+y} , C _{n+z}	C _{n+x} , C _{n+y} , C _{n+z}	12, 11, 9	CARRY OUTPUTS
G	Y	10	CARRY GENERATE OUTPUT
P	X	7	CARRY PROPAGATE OUTPUT
VCC		16	SUPPLY VOLTAGE
GND		8	GROUND

† Interpretations are illustrated in the '181, 'LS181, 'S181 data sheet.

logic symbol†



Pin numbers shown on logic notation are for D, J or N packages.

description

The SN54182, SN54S182, SN74182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with the '181, 'LS181, or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '182 or 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '182 or 'S182 circuits to perform multi-level look-ahead is illustrated under typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the '181, 'LS181, and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the '182 and 'S182 are:

$$\begin{aligned} C_{n+x} &= G0 + P0 C_n \\ C_{n+y} &= G1 + P1 G0 + P1 P0 C_n \\ C_{n+z} &= G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 C_n \\ \bar{C} &= \bar{G3} + \bar{P3} \bar{G2} + \bar{P3} \bar{P2} \bar{G1} + \bar{P3} \bar{P2} \bar{P1} \bar{P0} \\ \bar{P} &= \bar{P3} \bar{P2} \bar{P1} \bar{P0} \end{aligned} \quad \begin{aligned} C_{n+x} &= Y0 (X0 + C_n) \\ C_{n+y} &= Y1 (X1 + Y0 (X0 + C_n)) \\ C_{n+z} &= Y2 (X2 + Y1 (X1 + Y0 (X0 + C_n))) \\ Y &= Y3 (X3 + Y2) (X3 + X2 + Y1) (X3 + X2 + X1 + Y0) \\ X &= X3 + X2 + X1 + X0 \end{aligned}$$

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-601

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TTL DEVICES

TYPES SN54182, SN54S182, SN74182, SN74S182 LOOK-AHEAD CARRY GENERATORS

logic

FUNCTION TABLE FOR \bar{G} OUTPUT

INPUTS							OUTPUT
\bar{G}_3	\bar{G}_2	\bar{G}_1	\bar{G}_0	\bar{P}_3	\bar{P}_2	\bar{P}_1	\bar{G}
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR \bar{P} OUTPUT

INPUTS				OUTPUT
\bar{P}_3	\bar{P}_2	\bar{P}_1	\bar{P}_0	\bar{P}
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
\bar{G}_0	\bar{P}_0	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
\bar{G}_1	\bar{G}_0	\bar{P}_1	\bar{P}_0	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
\bar{G}_2	\bar{G}_1	\bar{G}_0	\bar{P}_2	\bar{P}_1	\bar{P}_0	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

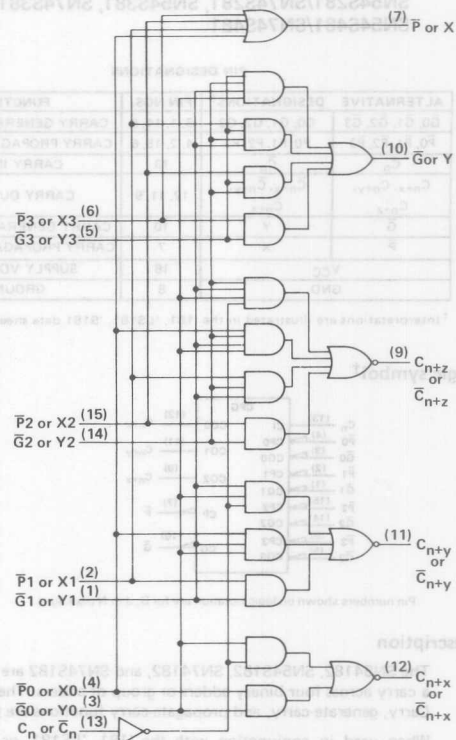
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermittent voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits	-55°C to 125°C
SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except intermittent voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each \bar{G} input in conjunction with any other \bar{G} input or in conjunction with any \bar{P} input.

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

SN74182, SN74182 LOOK-AHEAD CARRY GENERATORS

recommended operating conditions

PARAMETER	SN54182			SN74182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54182			SN74182			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.8			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$		-1.5			-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH} High-level input current	C_H input		80			80		μ A
	P_3 input		120			120		
	P_2 input		160			160		
	$P_0, P_1, \text{ or } G_3$ input		200			200		
	G_0 or G_2 input		360			360		
	G_1 input		400			400		
I_{IL} Low-level input current	C_H input		-3.2			-3.2		mA
	P_3 input		-4.8			-4.8		
	P_2 input		-6.4			-6.4		
	$P_0, P_1, \text{ or } G_3$ input		-8			-8		
	G_0 or G_2 input		-14.4			-14.4		
	G_1 input		-16			-16		
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH} Supply current, all outputs high	$V_{CC} = 5 \text{ V}, \text{ See Note 3}$	27			27	65		mA
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX}, \text{ See Note 4}$	45	65		45	72		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTES: 3. I_{CCH} is measured with all outputs open, inputs P_3 and G_3 at 4.5 V, and all other inputs grounded.

4. I_{CCL} is measured with all outputs open; inputs G_0, G_1 , and G_2 at 4.5 V; and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$		11	17	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 5		15	22	ns

NOTE 5: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

recommended operating conditions

PARAMETER	SN54S182			SN74S182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S182			SN74S182			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	C_n input			50			50	μA
	P_3 input			100			100	
	P_2 input			150			150	
	P_0, P_1 , or G_3 input			200			200	
	G_0 or G_2 input			350			350	
	G_1 input			400			400	
I_{IL} Low-level input current	C_n input			-2			-2	mA
	P_3 input			-4			-4	
	P_2 input			-6			-6	
	P_0, P_1 , or G_3 input			-8			-8	
	G_0 or G_2 input			-14			-14	
	G_1 input			-16			-16	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CCH} Supply current, all outputs high	$V_{CC} = 5 \text{ V}$, See Note 3		35	70		35	70	mA
I_{CCL} Supply current, all outputs low	$V_{CC} = \text{MAX}$, See Note 4		69	99		69	109	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTES: 3. I_{CCH} is measured with all outputs open, inputs P_3 and G_3 at 4.5 V, and all other inputs grounded.

4. I_{CCL} is measured with all outputs open; inputs G_0, G_1 , and G_2 at 4.5 V; and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	G_0, G_1, G_2, G_3	C_{n+x}, C_{n+y}	$R_L = 280 \Omega, C_L = 15 \text{ pF}$, See Note 5	4.5	7		ns
t_{PHL}	P_0, P_1, P_2 , or P_3	or C_{n+z}		4.5	7		
t_{PLH}	G_0, G_1, G_2, G_3	G		5	7.5		ns
t_{PHL}	P_1, P_2 , or P_3	G		7	10.5		
t_{PLH}	P_0, P_1, P_2 , or P_3	P		4.5	6.5		ns
t_{PHL}	P_0, P_1, P_2 , or P_3	P		6.5	10		
t_{PLH}	C_n	C_{n+x}, C_{n+y}		6.5	10		ns
t_{PHL}	C_n	or C_{n+z}		7	10.5		

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

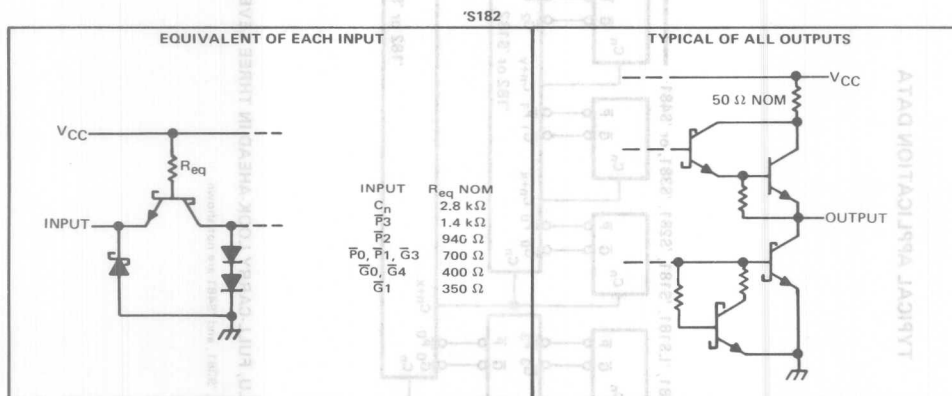
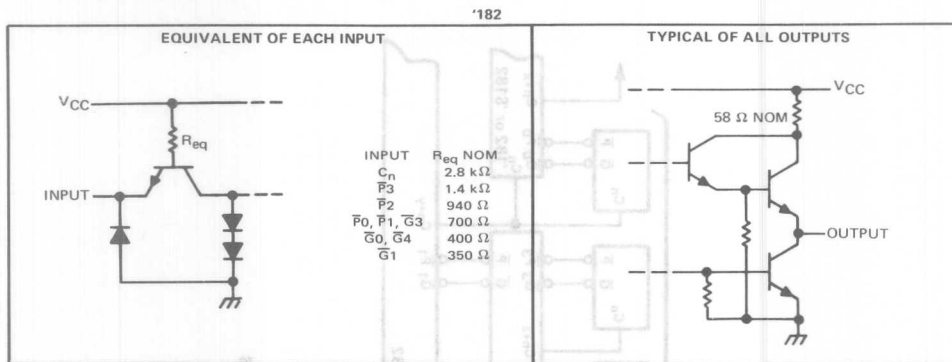
NOTE 5: See General Information Section for load circuits and voltage waveforms.

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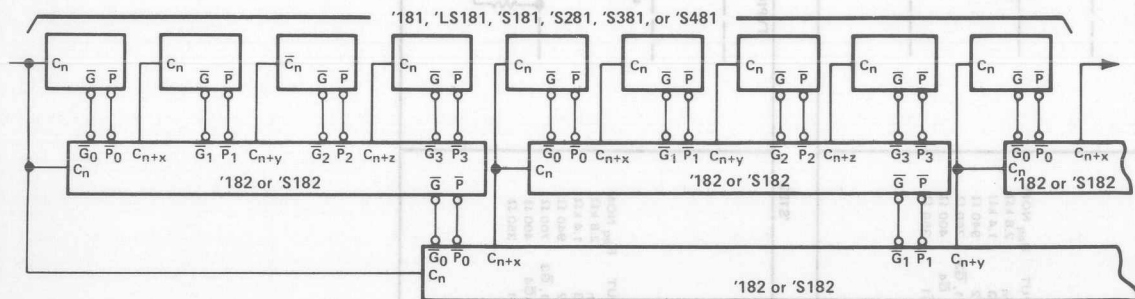
TTL DEVICES

TYPES SN54182, SN54S182, SN74182, SN74S182 LOOK-AHEAD CARRY GENERATORS

schematics of inputs and outputs



TYPICAL APPLICATION DATA



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

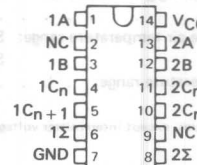
Remaining inputs and outputs of '181, 'LS181, 'S181, 'S281, 'S381, and 'S481 are not shown.

TYPES SN54LS183, SN74LS183 DUAL CARRY-SAVE FULL ADDERS

BULLETIN NO. DL-S 7711848, OCTOBER 1976 — REVISED OCTOBER 1983

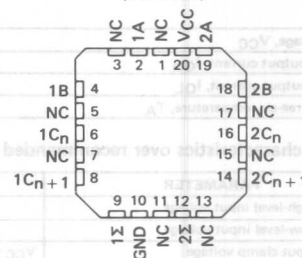
- For Use in High-Speed Wallace-Tree Summing Networks
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design

SN54LS183 ... J OR W PACKAGE
SN74LS183 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS183 ... FK PACKAGE
SN74LS183

(TOP VIEW)



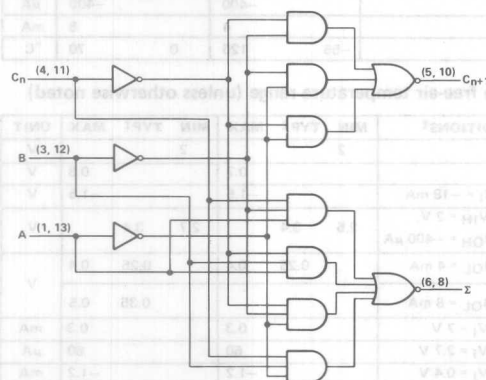
NC - No internal connection

FUNCTION TABLE
(EACH ADDER)

INPUTS			OUTPUTS	
C _n	B	A	Σ	C _{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

TYPES	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'LS183	15 ns	23 mW per bit

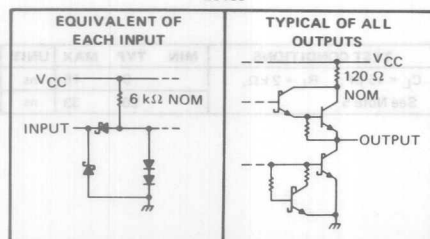
logic diagram (each adder)



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs

'LS183



PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-607

3
TTL DEVICES

TYPES SN54LS183, SN74LS183 DUAL CARRY-SAVE FULL ADDERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS183 Circuits	-55°C to 125°C
SN74LS183 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values, except intermitter voltage, are with respect to network ground terminal.

recommended operating conditions

	SN54LS183			SN74LS183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operation free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.3			0.3	mA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			60			60	μ A
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.2			-1.2	mA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, See Note 3	-20		-100	-20		-100	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$, See Note 4		10	17		10	17	mA
I_{CCL} Supply current, all outputs low			8	14		8	14	mA
I_{CCH} Supply current, all outputs high								

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. I_{CCL} is measured with all outputs open and all inputs grounded.

4. I_{CCH} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 5	9	15		ns
t_{PHL} Propagation delay time, high-to-low-level output		20	33		ns

NOTE 5: See General Information Section for load circuits and voltage waveforms.

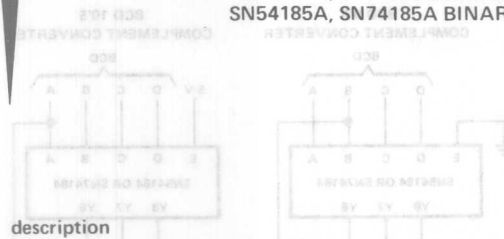
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TTL DEVICES

TYPES SN54184, SN54185A, SN74184, SN74185A BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

FEBRUARY 1971 - REVISED DECEMBER 1972

SN54184, SN74184 BCD-TO-BINARY CONVERTERS SN54185A, SN74185A BINARY-TO-BCD CONVERTERS



description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the function tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the '185A and all "don't care" conditions of the '184 are programmed high. The outputs are of the open-collector type.

The SN54184 and SN54185A are characterized for operation over the full military temperature range of -55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

- Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
- Shift right; examine; and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

SN54184, SN54185A ... J OR W PACKAGE
SN74184, SN74185A ... J OR N PACKAGE

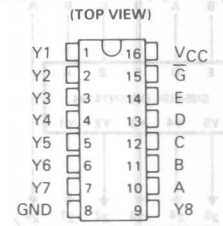


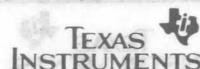
TABLE I
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	56	80
3	6	140	200
4	11	196	280
5	19	280	400
6	28	364	520

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table (following page, right) when the devices are connected as shown above the function table.

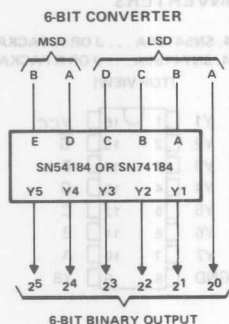
PRODUCTION DATA

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TYPES SN54184, SN74184 BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

SN54184 and SN74184 BCD-to-binary converters (continued)



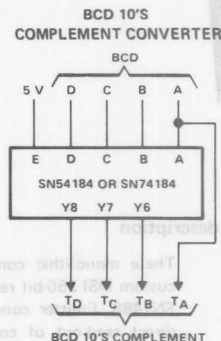
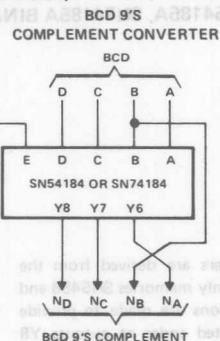
**FUNCTION TABLE
BCD-TO-BINARY
CONVERTER**

BCD WORDS	INPUTS (See Note A)					OUTPUTS (See Note B)				
	E	D	C	B	A	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	H	H
8-9	L	L	H	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	H	H	L
14-15	L	H	L	H	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L
18-19	L	H	H	L	L	L	L	H	L	H
20-21	H	L	L	L	L	L	L	H	L	L
22-23	H	L	L	L	H	L	L	H	L	H
24-25	H	L	L	H	L	L	L	H	H	L
26-27	H	L	L	H	H	L	L	H	L	H
28-29	H	L	H	L	L	L	L	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H
32-33	H	H	L	L	H	L	L	L	L	L
34-35	H	H	L	H	L	L	L	L	L	H
36-37	H	H	L	H	H	L	L	L	H	L
38-39	H	H	H	L	L	L	L	L	L	H
ANY	X	X	X	X	X	H	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.

B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.



**FUNCTION TABLE
BCD 9'S OR BCD 10'S
COMPLEMENT CONVERTER**

BCD WORD	INPUTS (See Note C)					OUTPUTS (See Note D)		
	E†	D	C	B	A	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L
1	L	L	L	L	H	L	H	L
2	L	L	L	H	L	L	H	H
3	L	L	L	H	H	L	L	H
4	L	L	H	L	L	L	L	H
5	L	L	H	L	H	L	L	L
6	L	L	H	H	L	L	L	L
7	L	L	H	H	H	L	L	L
8	L	H	L	L	L	L	L	L
9	L	H	L	L	H	L	L	L
0	H	L	L	L	L	L	L	L
1	H	L	L	L	H	L	L	L
2	H	L	L	H	L	L	L	L
3	H	L	L	H	H	L	L	H
4	H	L	H	L	L	L	L	H
5	H	L	H	L	H	L	L	L
6	H	L	H	H	L	L	L	L
7	H	L	H	H	H	L	L	L
8	H	H	L	L	L	L	L	L
9	H	H	L	L	H	L	L	L
ANY	X	X	X	X	X	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

TYPES SN54185A, SN74185A BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

- Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
- Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
- Repeat step b until the least-significant binary bit is in the least-significant BCD location.

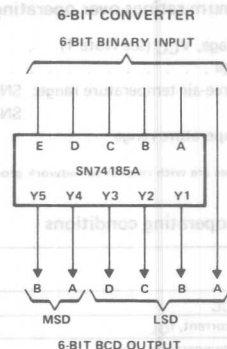


TABLE II

SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

FUNCTION TABLE

BINARY WORDS	BINARY SELECT					ENABLE G	OUTPUTS									
	E	D	C	B	A		Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1		
0 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
2 3	L	L	L	L	H	L	H	H	L	L	L	L	L	L	H	H
4 5	L	L	L	H	L	L	H	H	L	L	L	L	L	H	L	L
6 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H	L	L
8 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L	L	L
10 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L	L	L
12 13	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
14 15	L	L	H	H	H	L	H	H	L	L	H	H	L	L	H	H
16 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H	L	L
18 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L	L	L
20 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L	L	L
22 23	L	H	L	H	H	L	H	H	L	H	L	L	L	L	H	H
24 25	L	H	H	L	L	L	H	H	L	H	L	L	L	H	L	L
26 27	L	H	H	L	H	L	H	H	L	H	L	L	L	H	H	H
28 29	L	H	H	H	L	L	H	H	L	H	L	L	L	L	L	L
30 31	L	H	H	H	H	L	H	H	L	H	L	L	L	L	L	L
32 33	H	L	L	L	L	L	H	H	L	H	H	L	L	L	H	H
34 35	H	L	L	L	H	L	H	H	L	H	H	L	L	L	H	H
36 37	H	L	L	H	L	L	H	H	L	H	H	L	L	L	H	H
38 39	H	L	L	H	H	L	H	H	L	H	H	L	L	L	L	L
40 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L	L	L
42 43	H	L	H	L	H	L	H	H	H	L	L	L	L	L	L	L
44 45	H	L	H	H	L	L	H	H	H	L	L	L	L	L	L	L
46 47	H	L	H	H	H	L	H	H	H	L	L	L	L	L	H	H
48 49	H	H	L	L	L	L	H	H	H	L	L	L	L	L	L	L
50 51	H	H	L	L	H	L	H	H	H	L	L	L	L	L	L	L
52 53	H	H	L	H	L	L	H	H	H	L	L	L	L	L	L	L
54 55	H	H	L	H	H	L	H	H	H	L	L	L	L	L	L	L
56 57	H	H	H	L	L	L	H	H	H	L	L	L	L	L	H	H
58 59	H	H	H	L	H	L	H	H	H	L	L	L	L	L	L	L
60 61	H	H	H	H	L	L	H	H	H	L	L	L	L	L	L	L
62 63	H	H	H	H	H	L	H	H	H	L	L	L	L	L	L	L
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

3

TTL DEVICES

3 TTL DEVICES

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54184, SN54185A	-55°C to 125°C
SN74184, SN74185A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54184, SN54185A			SN74184, SN74185A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

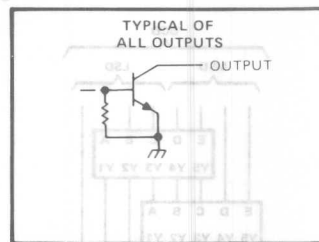
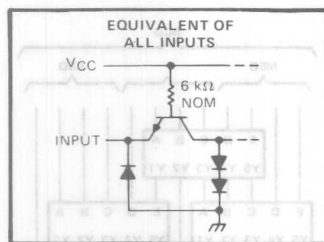
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			100	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 12 \text{ mA}$			0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = \text{MAX}$		50		mA
I_{CCL}	Supply current, all programmed outputs low			62	99	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

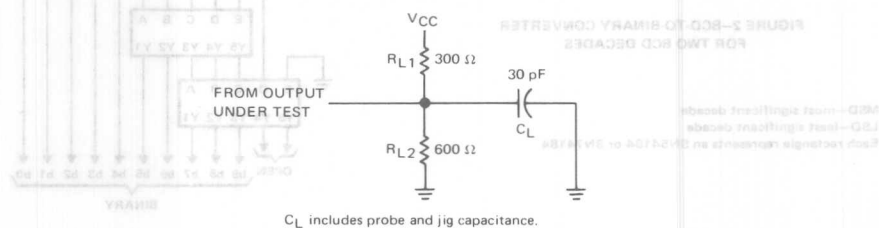
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output from enable \overline{G}	C _L = 30 pF,		19	30	ns
t _{PHL}	Propagation delay time, high-to-low-level output from enable \overline{G}	R _{L1} = 300 Ω ,		22	35	ns
t _{PLH}	Propagation delay time, low-to-high-level output from binary select	R _{L2} = 600 Ω ,		27	40	ns
t _{PHL}	Propagation delay time, high-to-low-level output from binary select	See Figure 1 and Note 2		23	40	ns

TYPES SN54184, SN54185A, SN74184, SN74185A BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

schematics of inputs and outputs



PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT
FIGURE 1

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54184, SN74184 BCD-TO-BINARY CONVERTERS

TYPICAL APPLICATION DATA SN54184, SN74184

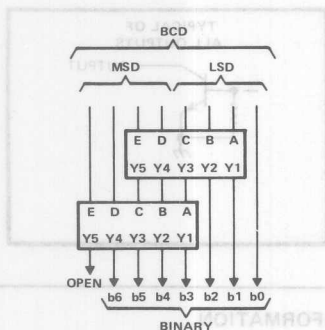


FIGURE 2—BCD-TO-BINARY CONVERTER
FOR TWO BCD DECADES

MSD—most significant decade
LSD—least significant decade
Each rectangle represents an SN54184 or SN74184

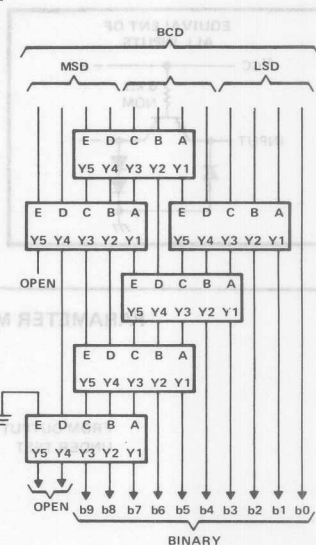


FIGURE 3—BCD-TO-BINARY CONVERTER
FOR THREE BCD DECADES

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TTL DEVICES

TYPES SN54184, SN74184 BCD-TO-BINARY CONVERTERS

TYPICAL APPLICATION DATA SN54184, SN74184

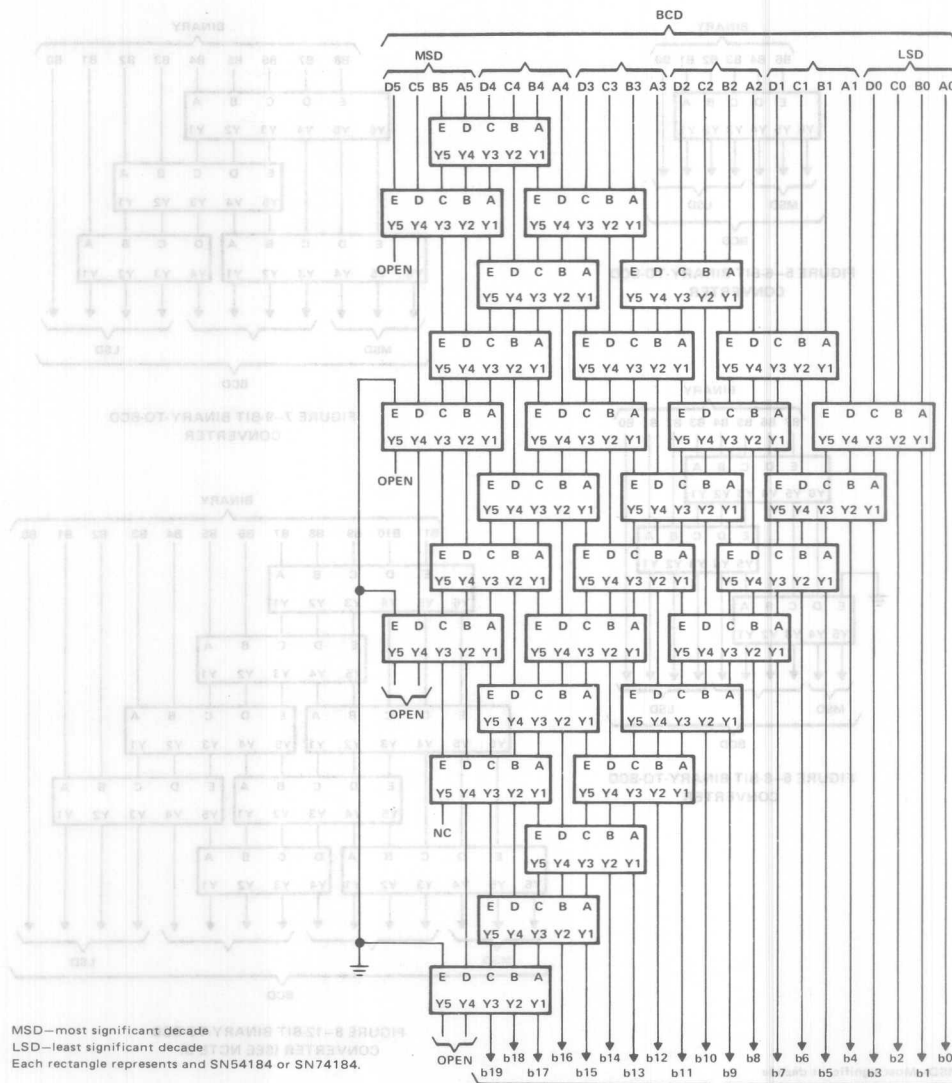


FIGURE 4—BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

TYPES SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

TYPICAL APPLICATION DATA SN54185A, SN74185A

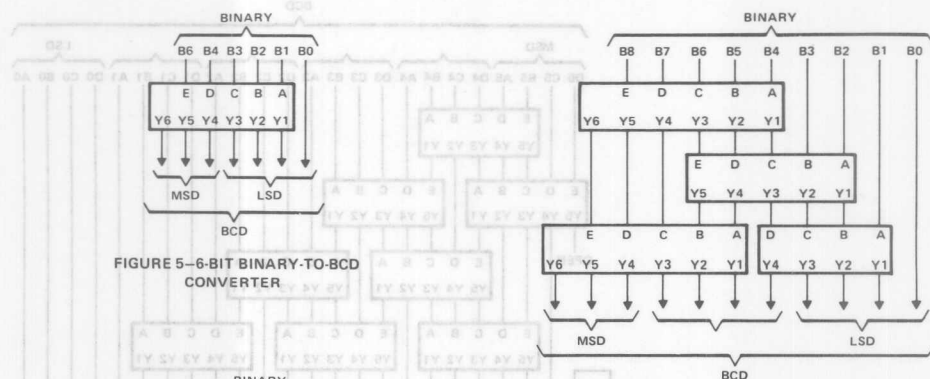


FIGURE 5—6-BIT BINARY-TO-BCD CONVERTER

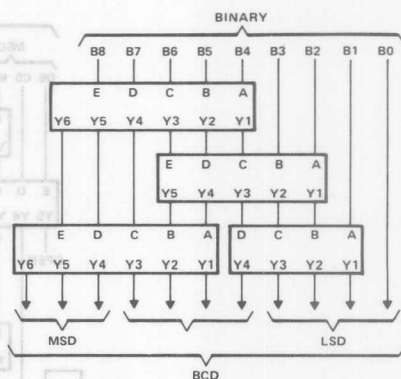


FIGURE 7—9-BIT BINARY-TO-BCD CONVERTER

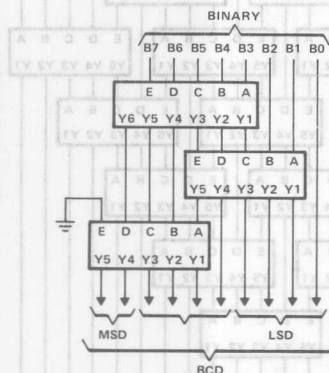


FIGURE 6—8-BIT BINARY-TO-BCD CONVERTER

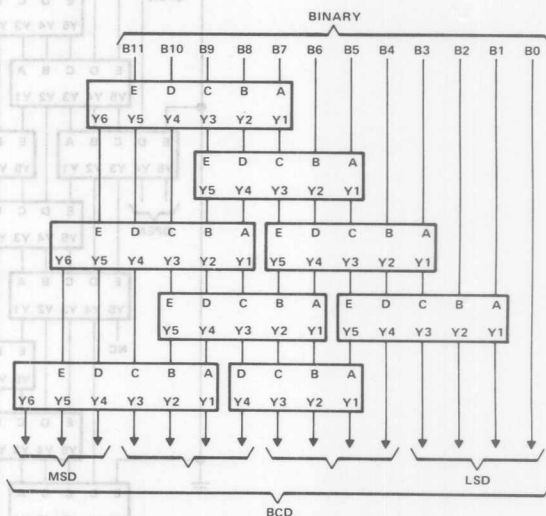


FIGURE 8—12-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

MSD—Most significant decade
LSD—Least significant decade
NOTES: A. Each rectangle represents an SN54185A or an SN74185A.
B. All unused E inputs are grounded.

TYPES SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

TYPICAL APPLICATION DATA SN54185A, SN74185A

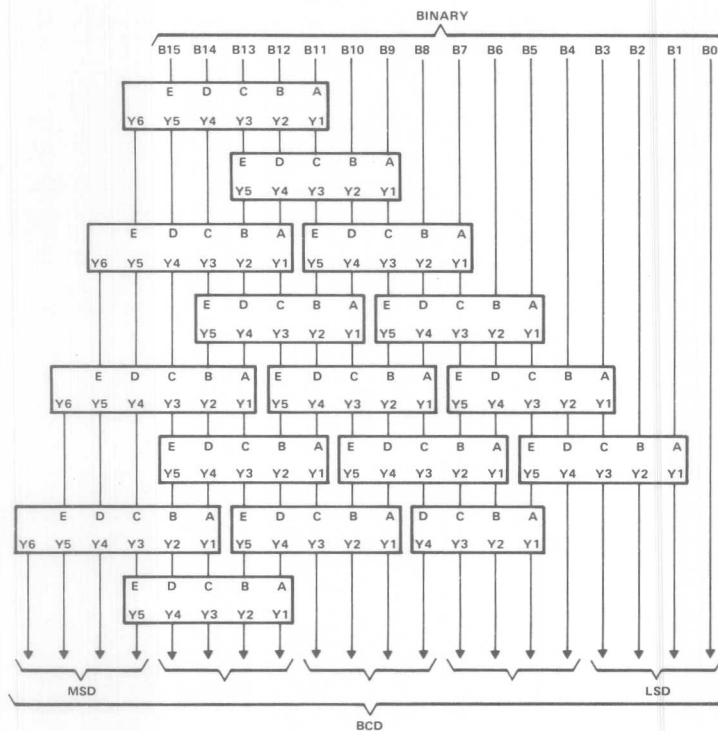


FIGURE 9—16 BIT BINARY-TO-BCD
CONVERTER (SEE NOTE B)

MSD—most significant decade

LSD—least significant decade

NOTES: A. Each rectangle represents an SN54185A or SN74185A.

B. All unused E inputs are grounded.

3

TTL DEVICES

TYPICAL APPLICATION DATA
54188A, 54188A

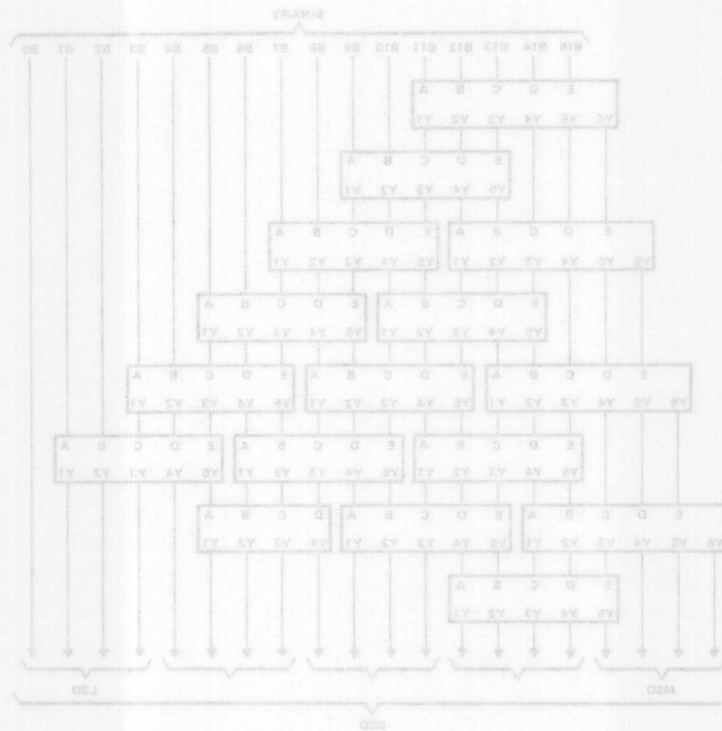


FIGURE 9-16 9-BIT BINARY-TO-BCD
CONVERTER (SEE NOTE B)

MSD—most significant decade
LSD—least significant decade
NOTES: A. Each hex digit represents an 8421BCD digit.
B. All unused B inputs are grounded.

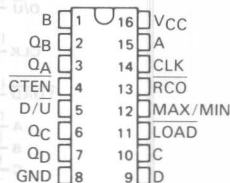
TYPES SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

DECEMBER 1972—REVISED DECEMBER 1983

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presetable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

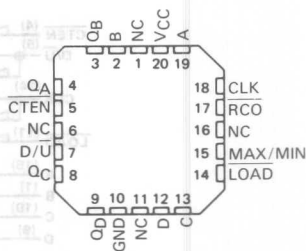
SN54190, SN54191, SN54LS190,
SN54LS191 ... J OR W PACKAGE
SN74190, SN74191 ... J OR N PACKAGE
SN74LS190, SN74LS191 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS190, SN54LS191 ... FK PACKAGE
SN74LS190, SN74LS191

(TOP VIEW)



NC - No internal connection

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

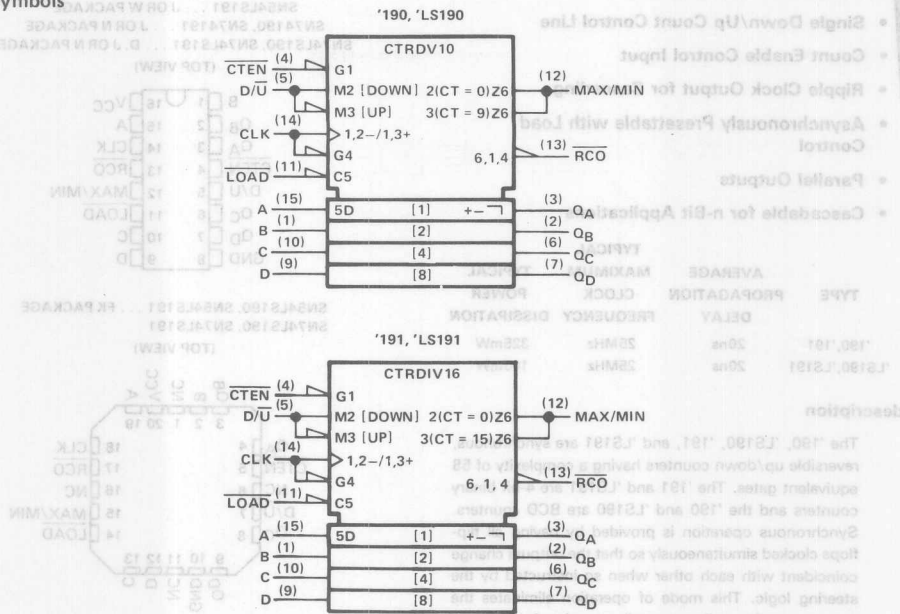
TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN54190, SN54191, SN54LS190, SN54LS191 SN74190, SN74191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

The output of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

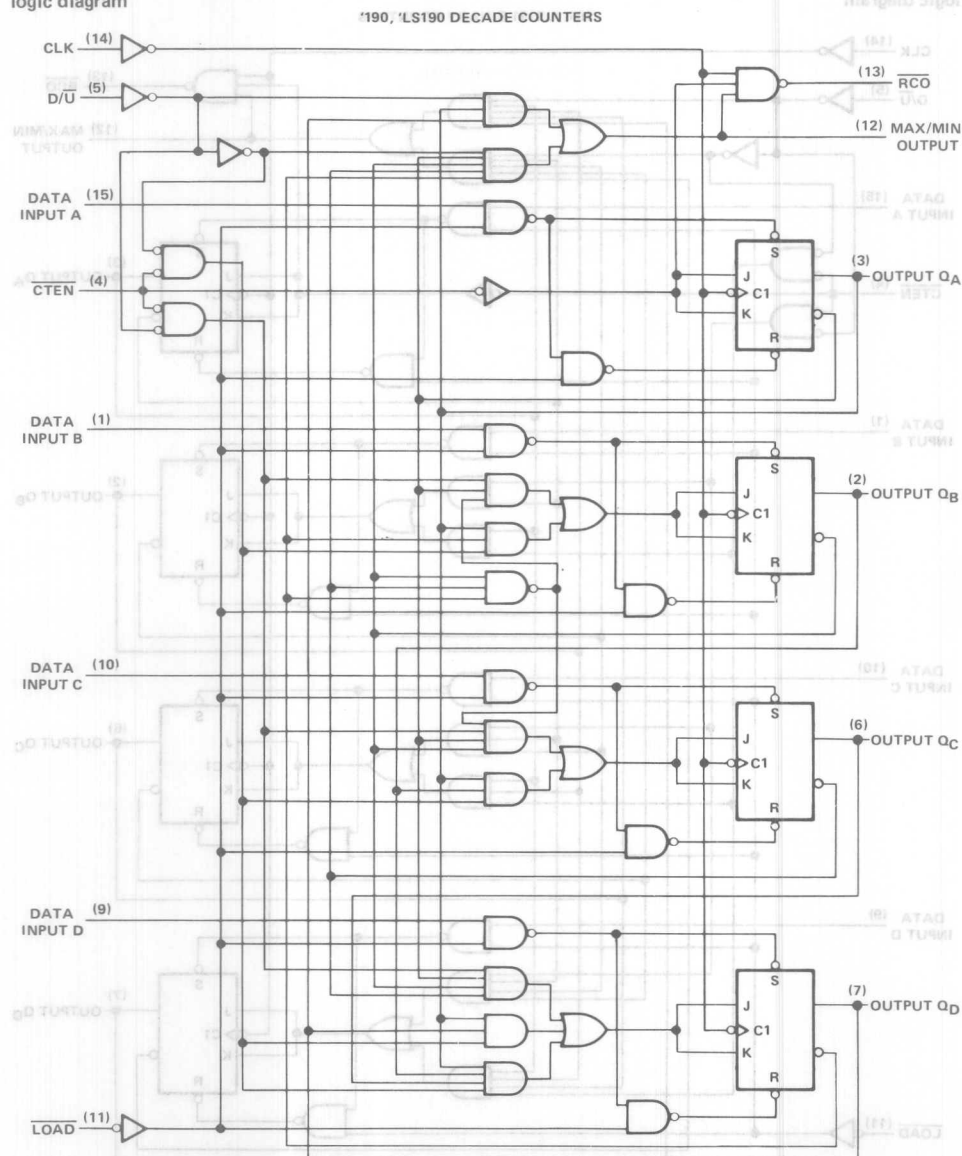
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter. If parallel counting is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54[®] and 54LS[®] are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74[®] and 74LS[®] are characterized for operation from 0°C to 70°C.

TYPES SN54190, SN54LS190, SN74190, SN74LS190
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

logic diagram



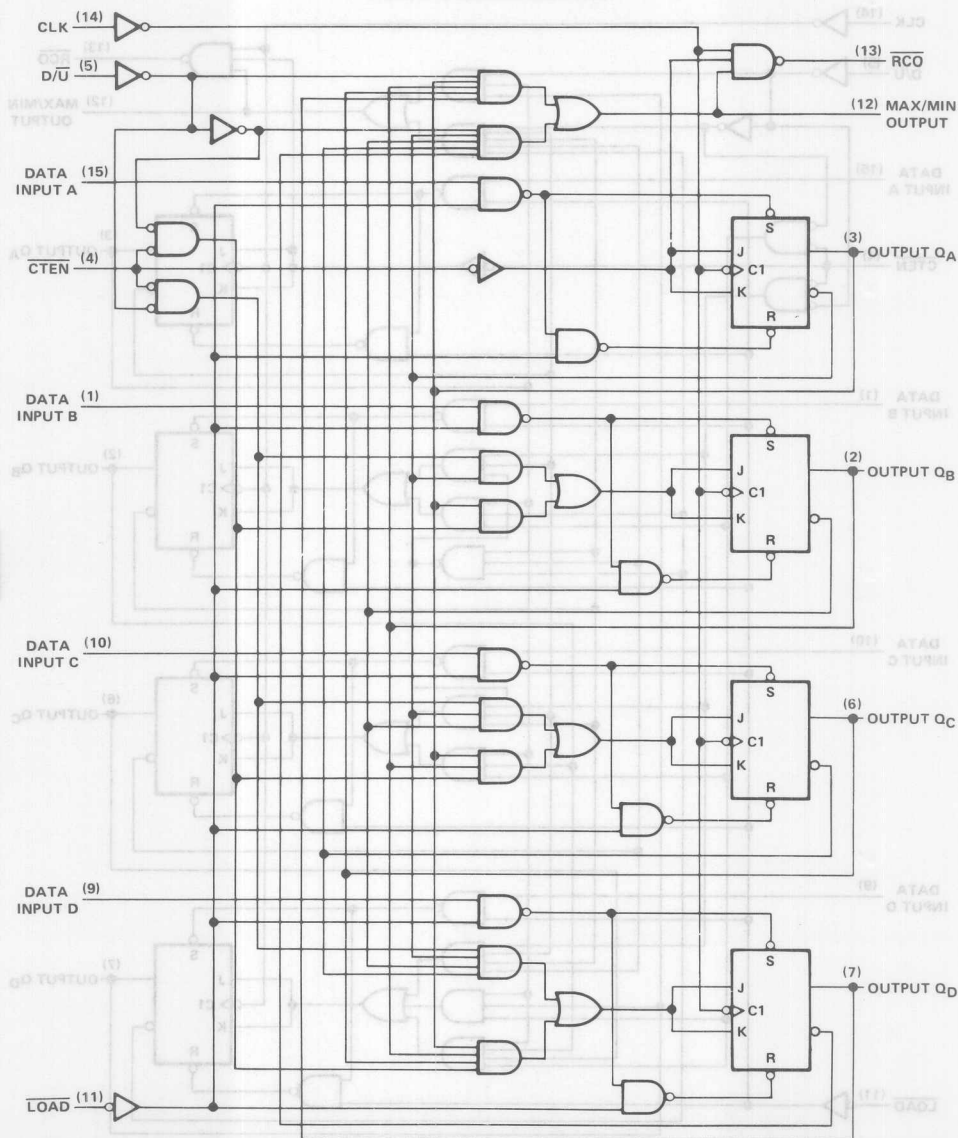
3

TTL DEVICES

TYPES SN54191, SN54LS191, SN74191, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

logic diagram

'191, 'LS191 BINARY COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

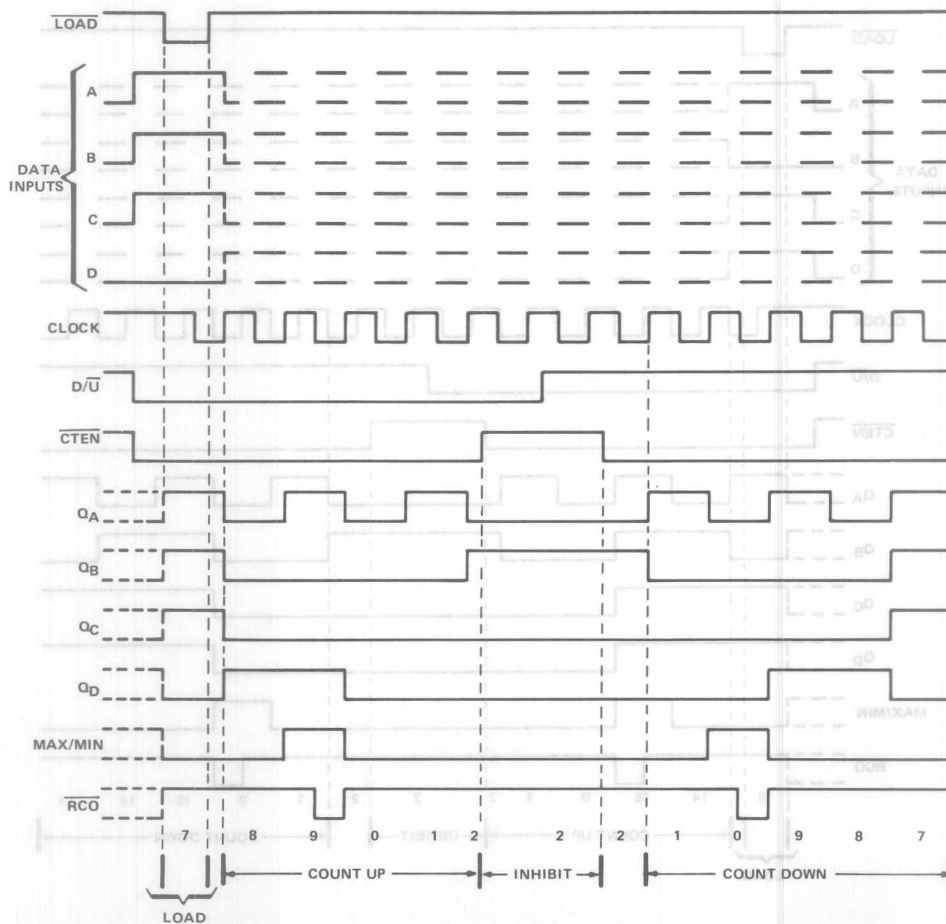
TYPES SN54190, SN54LS190, SN74190, SN74LS190
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

'190, 'LS190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



3

TTL DEVICES

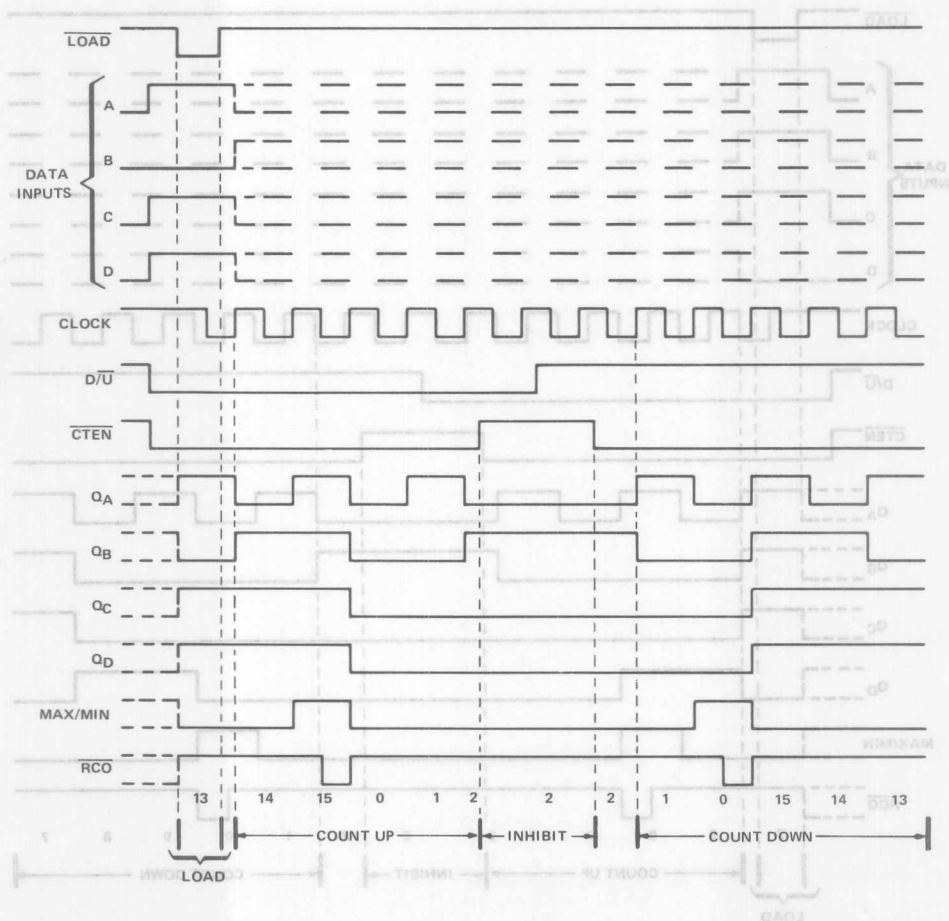
TYPES SN54191, SN54LS191, SN74191, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

'191, 'LS191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



3

TTL DEVICES

**TYPES SN54190, SN54191, SN54LS190, SN54LS191,
SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SN54 ¹ , SN74 ¹ Circuits	5.5 V
SN54LS ¹ , SN74LS ¹ Circuits	7 V
Operating free-air temperature range: SN54 ¹ , SN54LS ¹ Circuits	–55°C to 125°C
SN74 ¹ , SN74LS ¹ Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				–0.8			–0.8	mA
I_{OL}	Low-level output current				16			16	mA
f_{clock}	Input clock frequency		0		20	0		20	MHz
$t_{w(clock)}$	Width of clock input pulse		25			25			ns
$t_{w(load)}$	Width of load input pulse		35			35			ns
t_{su}	Setup time	Data, high or low (See Figure 1 and 2)	20			20			ns
		Load inactive state	20			20			ns
t_{hold}	Data hold time		0			0			ns
T_A	Operating free-air temperature		–55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	$V_{CC} = \text{MIN}$	2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = \text{MIN}$	0.8			0.8			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.5			-1.5			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.8 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	High-level input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$	1			1			mA
I_{IH}	High-level input current at any input except enable	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$	40			40			μA
I_{IH}	High-level input current at enable input		120			120			μA
I_{IL}	Low-level input current at any input except enable	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1.6			-1.6			mA
I_{IL}	Low-level input current at enable input		-4.8			-4.8			mA
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	-20	-65		-18	-65		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 2	65	99		65	105		mA

† For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

3

TTL DEVICES

TYPES SN54190, SN54191, SN74190, SN74191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

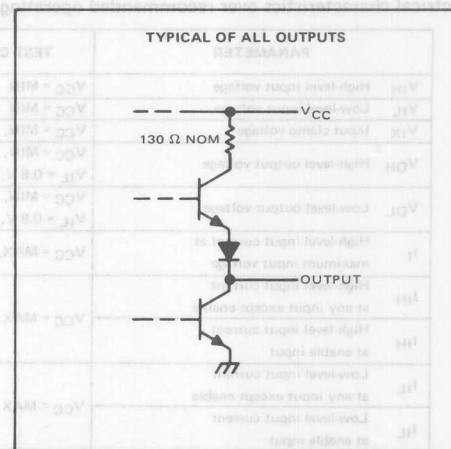
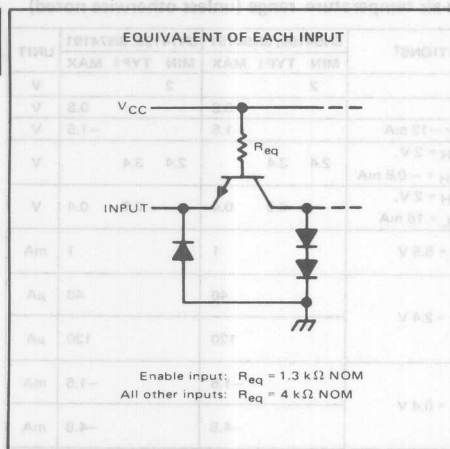
PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'190, '191			UNIT
				MIN	TYP	MAX	
f_{max}				20	25		MHz
t_{PLH}	$\overline{\text{Load}}$	Q_A, Q_B, Q_C, Q_D	$C_L = 15 \text{ pF}, R_L = 400 \Omega$, See Figures 1 and 3 thru 7		22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	CLK	\overline{RCO}			13	20	ns
t_{PHL}					16	24	
t_{PLH}	CLK	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	CLK	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	D/\overline{U}	\overline{RCO}			30	45	ns
t_{PHL}					30	45	
t_{PLH}	D/\overline{U}	Max/Min			21	33	ns
t_{PHL}					22	33	

[†] f_{max} maximum clock frequency
 t_{PLH} propagation delay time, low to high-level output
 t_{PHL} propagation delay time, high to low-level output

schematics of inputs and outputs

3

TTL DEVICES



TYPES SN54LS190, SN54LS191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS190 SN54LS191			SN74LS190 SN74LS191			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		20	0		20	MHz
t _{w(clock)}	Width of clock input pulse	25			25			ns
t _{w(load)}	Width of load input pulse	35			35			ns
t _{su}	Data setup time (See Figures 1 and 2)	20			20			ns
t _{su}	Load inactive state setup time	30			30			ns
t _h	Data hold time	5			5			ns
t _h	Enable hold time	0			0			ns
t _{enable}	Count enable time (see Note 3)	40			40			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS190 SN54LS191			SN74LS190 SN74LS191			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA		2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA	I _{OL} = 8 mA	0.25	0.4		0.25	0.4		V
I _I	High-level input current at maximum input voltage	Enable Others	V _{CC} = MAX, V _I = 7 V			0.3			0.3	mA
						0.1			0.1	
I _{IH}	High-level input current	Enable Others	V _{CC} = MAX, V _I = 2.7 V			60			60	µA
						20			20	
I _{IL}	Low-level input current	Enable Others	V _{CC} = MAX, V _I = 0.4 V			-1.2			-1.2	mA
						-0.4			-0.4	
I _{OS}	Short-circuit output current§	V _{CC} = MAX,		-20		-100	-20		-100	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2		20		35	20		35	mA

† For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 2. I_{CC} is measured with all inputs grounded and all outputs open.

3. Minimum count enable time is the interval immediately preceding the rising edge of the clock pulse during which interval the count enable input must be low to ensure counting.

3

TTL DEVICES

TYPES SN54LS190, SN54LS191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

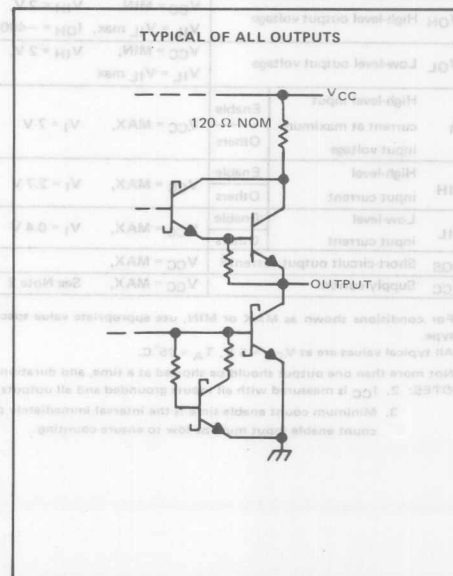
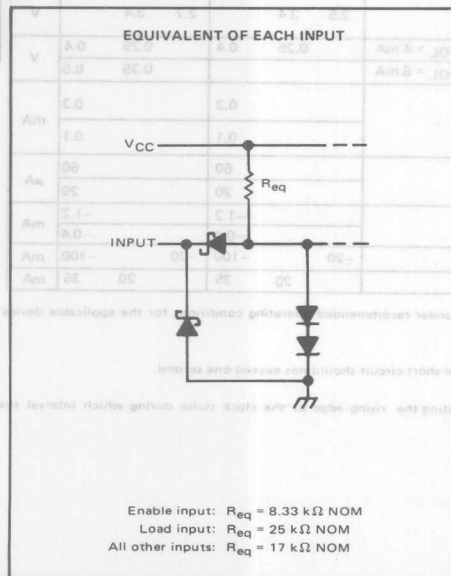
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS190, 'LS191			UNIT
				MIN	TYP	MAX	
f_{\max}				20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D	$C_L = 15\text{ pF}, R_L = 2\text{ k}\Omega$ See Figures 1 and 3 thru 7	22	33		ns
t_{PHL}				33	50		ns
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D		20	32		ns
t_{PHL}				27	40		ns
t_{PLH}	CLK	\overline{RCO}		13	20		ns
t_{PHL}				16	24		ns
t_{PLH}	CLK	Q_A, Q_B, Q_C, Q_D		16	24		ns
t_{PHL}				24	36		ns
t_{PLH}	CLK	Max/Min		28	42		ns
t_{PHL}				37	52		ns
t_{PLH}	$\overline{D/U}$	\overline{RCO}		30	45		ns
t_{PHL}				30	45		ns
t_{PLH}	$\overline{D/U}$	Max/Min		21	33		ns
t_{PHL}				22	33		ns
t_{PLH}	\overline{CTEN}	\overline{RCO}		21	33		ns
t_{PHL}				22	33		ns

f_{\max} = maximum clock frequency
 t_{PLH} = propagation delay time, low to high-level output
 t_{PHL} = propagation delay time, high to low-level output

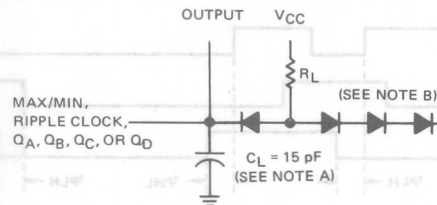
schematics of inputs and outputs

3 TTL DEVICES



**TYPES SN54190, SN54191, SN54LS190, SN54LS191,
SN74190, SN74191, SN74LS190, SN74LS191**
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

PARAMETER MEASUREMENT INFORMATION



**FIGURE 1—LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT**

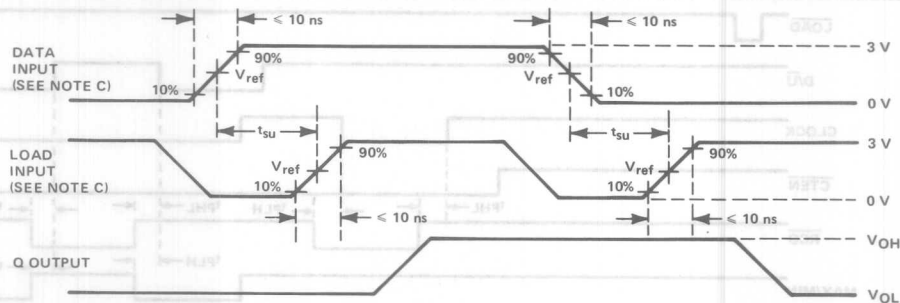
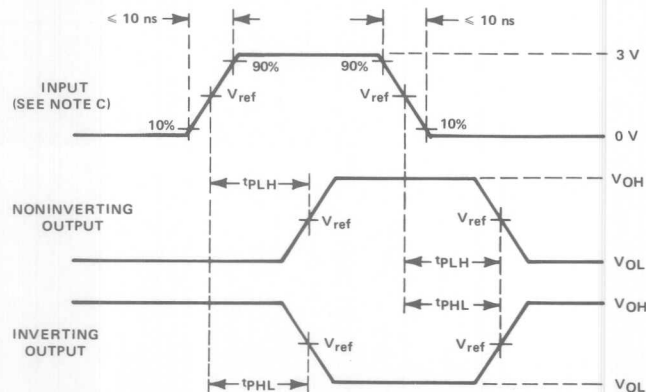


FIGURE 2—DATA SETUP TIME VOLTAGE WAVEFORMS



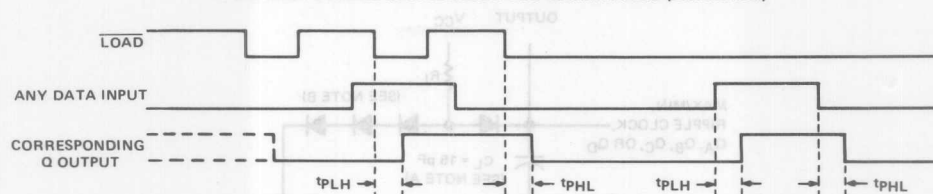
See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

FIGURE 3—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. The input pulses are supplied by generators having the following characteristics: $Z_{OUT} = 50 \Omega$, duty cycle $\leq 50\%$, PRR $\leq 1 \text{ MHz}$.
D. $V_{ref} = 1.5 \text{ V}$ for '190 and '191; 1.3 V for 'LS190 and 'LS191.

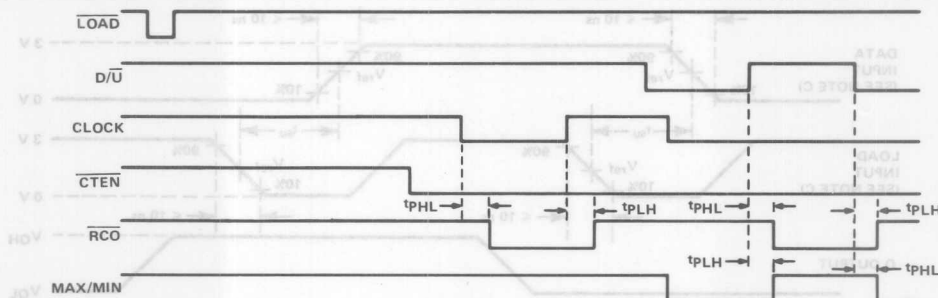
**TYPES SN54190, SN54191, SN54LS190, SN54LS191,
SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

PARAMETER MEASUREMENT INFORMATION (continued)



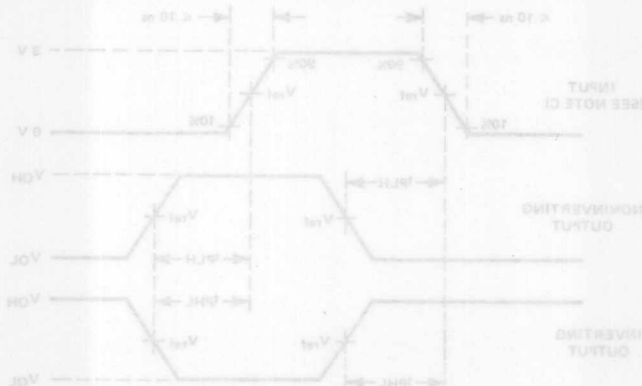
NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4—LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE F: All data inputs are low.

FIGURE 5—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



See waveform pad in Figure 4 for propagation delay from a specific input to a specific output. For simulation, pulse rise time, voltage levels, etc., have not been shown in Figure 4 through 7.

FIGURE 6—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES:
A. V_{CC} includes noise and its capacitance.
B. All diodes are 1N3004 or equivalent.
C. The input pulses are injected by squarewave having the following characteristics: $f_{max} = 50$ kHz, duty cycle $< 50\%$, $V_{OH} = 2.0$ V, $V_{OL} = 0.5$ V.
D. $V_{OH} = 2.5$ V for 190 and 191, $V_{OH} = 1.5$ V for 190 and 191.

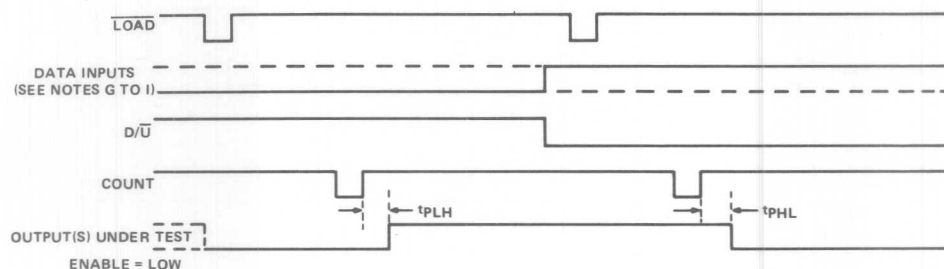
3

TTL DEVICES

TYPES SN54190, SN54191, SN54LS190, SN54LS191,
SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

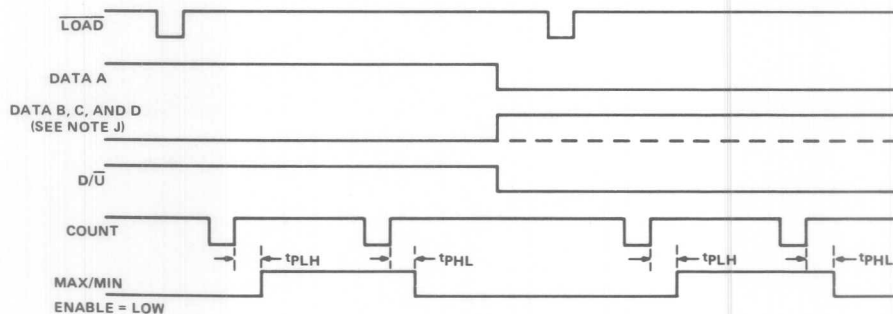
PARAMETER MEASUREMENT INFORMATION (continued)

switching characteristics (continued)



- NOTES: G. To test Q_A , Q_B , and Q_C outputs of '190 and 'LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
H. To test Q_D output of '190 and 'LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
I. To test Q_A , Q_B , Q_C , and Q_D outputs of '191 and 'LS191: All four data inputs are shown by the solid line.

FIGURE 6-CLOCK TO OUTPUT



NOTE J: Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 7-CLOCK TO MAX/MIN

SN54192, SN54193, SN54LS192, SN54LS193 SN74192, SN74193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

DECEMBER 1972—REVISED DECEMBER 1983

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

SN54192, SN54193, SN54LS192,
SN54LS193 ... J OR W PACKAGE

SN74192, SN74193 ... J OR N PACKAGE
SN74LS192, SN74LS193 ... D, J OR N PACKAGE

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'LS192, 'LS193	32 MHz	95 mW

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192 and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

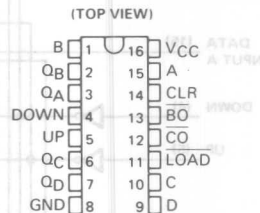
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Operating free-air temperature range	-55 to 125		0 to 70		°C
Storage temperature range	-65 to 150		-65 to 150		°C

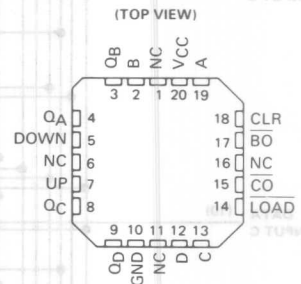
NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCTION DATA
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TEXAS
INSTRUMENTS



SN54LS192, SN54LS193 ... FK PACKAGE
SN74LS192, SN74LS193



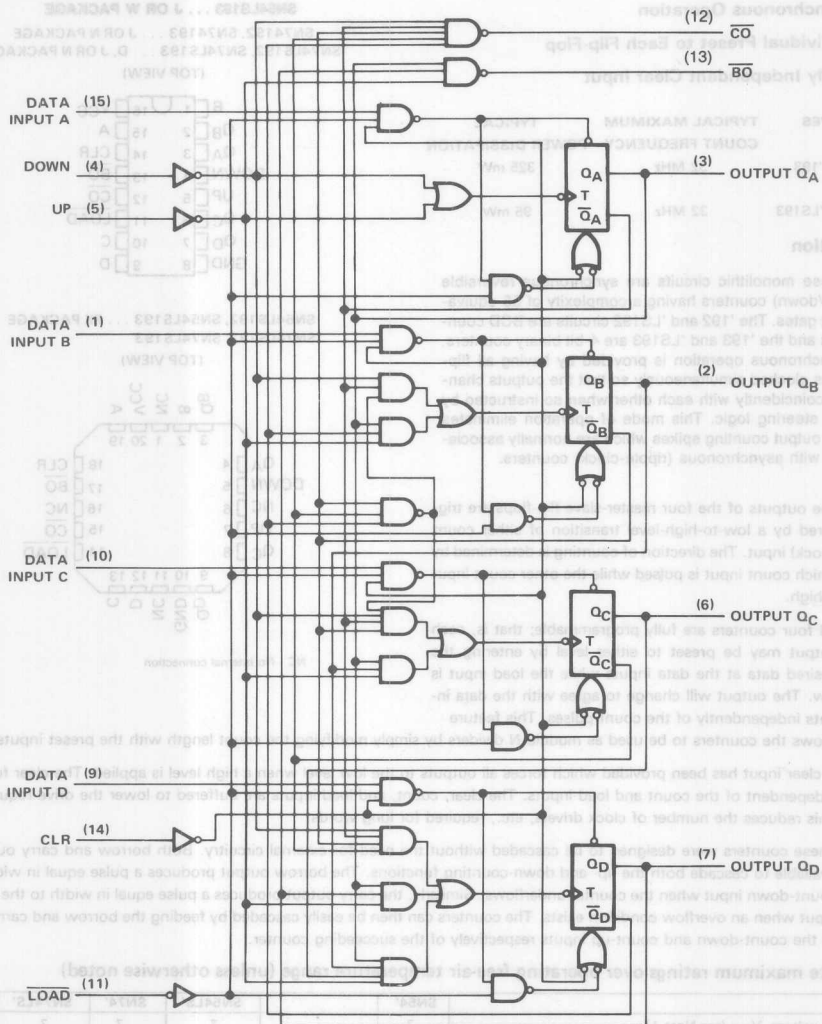
NC - No internal connection

3

TTL DEVICES

TYPES SN54192, SN54LS192, SN74192, SN74LS192 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

logic diagram



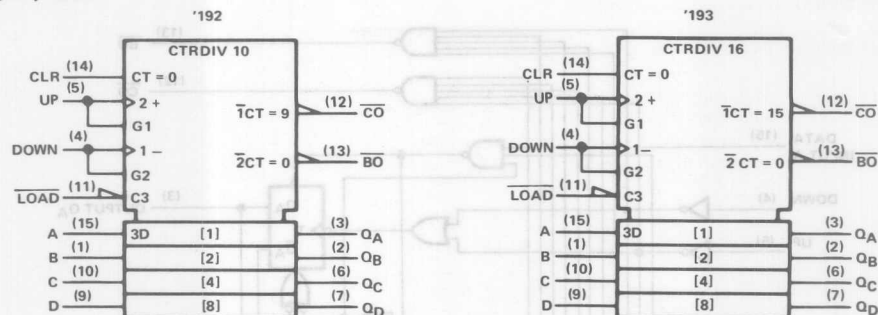
3 TTL DEVICES

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

Load input: $P_{\text{load}} = 50 \text{ kPa}$
All other inputs: $P_{\text{all}} = 15 \text{ kPa}$

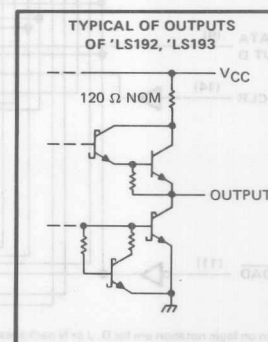
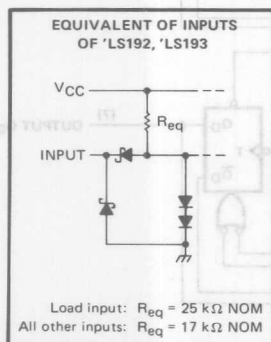
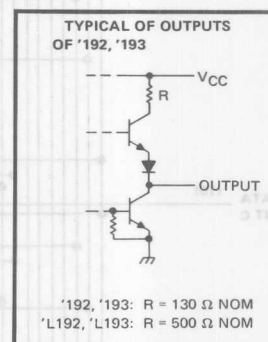
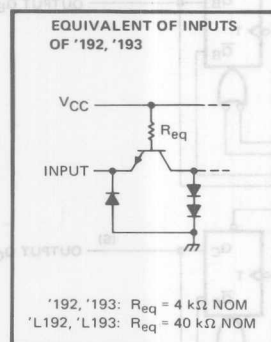
**TYPES SN54192, SN54193, SN54LS192, SN54LS193,
SN74192, SN74LS193, SN74LS192, SN74LS193**
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



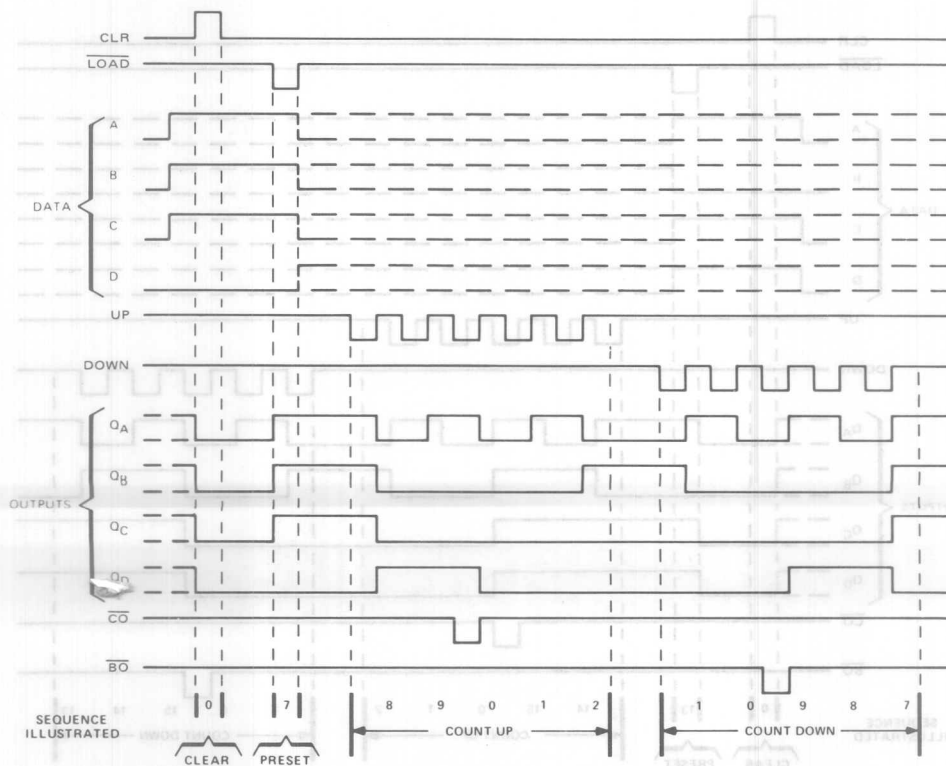
TYPES SN54192, SN54LS192, SN74192, SN74LS192 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

'192, 'LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

TYPES SN54193, SN54LS193, SN74193, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

'193, 'LS193 BINARY COUNTERS

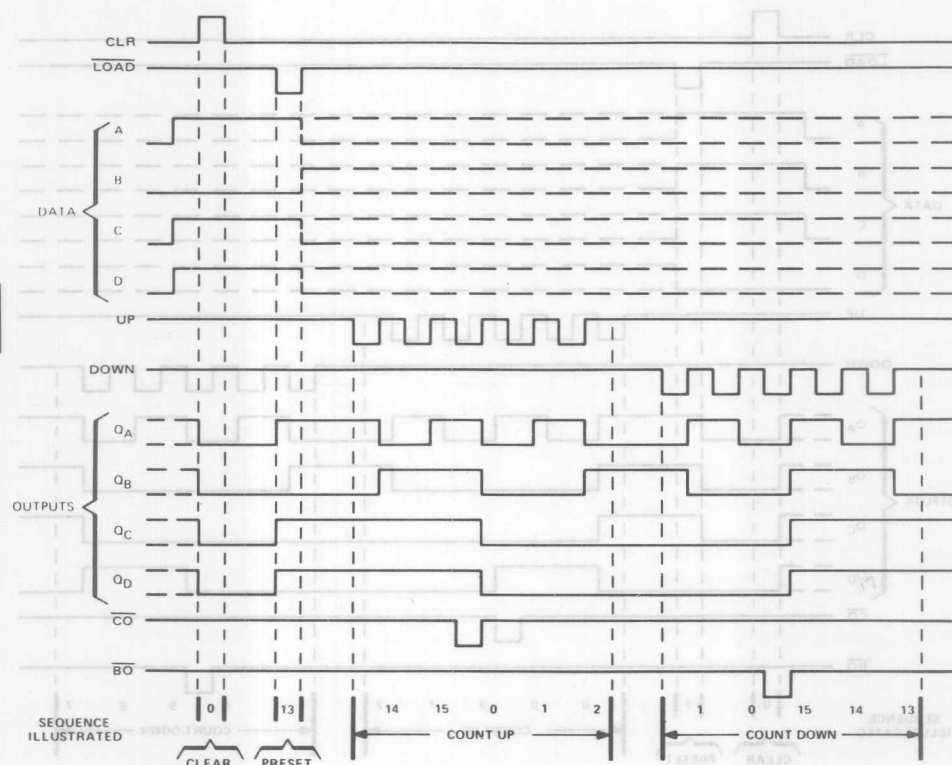
typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

3

TTL DEVICES



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

TYPES SN54192, SN54193, SN74192, SN74193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

recommended operating conditions

PARAMETER	DESCRIPTION	SN54192 SN54193			SN74192 SN74193			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			16			16	mA
f _{clock}	Clock frequency	0		25	0		25	MHz
t _w	Width of any input pulse	20			20			ns
t _{su}	Data setup time, (see Figure 1)	20			20			ns
t _h	Hold time			0			0	ns
				LOAD			3	
T _A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54192 SN54193			SN74192 SN74193			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
V _{IK}	Input clamp voltage			-1.5			-1.5	V
V _{OH}	High-level output voltage	2.4	3.4		2.4	3.4		V
V _{OL}	Low-level output voltage		0.2	0.4		0.2	0.4	V
I _I	Input current at maximum input voltage			1			1	mA
I _{IH}	High-level input current			40			40	µA
I _{IL}	Low-level input current			-1.6			-1.6	mA
I _{OS}	Short-circuit output current§	-20		-65	-18		-65	mA
I _{CC}	Supply current		65	89		65	102	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
t _{PLH}	UP	C ₀			17	26	ns
t _{PHL}					16	24	
t _{PLH}	DOWN	B ₀			16	24	ns
t _{PHL}					16	24	
t _{PLH}	UP OR DOWN	Q	C _L = 15 pF, R _L = 400 Ω, See Figures 1 and 2		25	38	ns
t _{PHL}					31	47	
t _{PLH}	LOAD	Q			27	40	ns
t _{PHL}					29	40	
t _{PHL}	CLR	Q			22	35	ns

¶ f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

3

TTL DEVICES

TYPES SN54LS192, SN54LS193, SN74LS192, SN74LS193
 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-400			-400	μ A
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Width of any input pulse	20			20			ns
t_{in}	Clear inactive-state setup time	15			15			ns
t_{su}	Load inactive-state setup time	15			15			ns
	Data setup time (see Figure 1)	20			20			ns
t_h	Data hold time	5			5			ns
T_A	Operating free-air temperature range	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu\text{A}$			2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$			0.25	0.4	0.15	0.4
		$I_{OL} = 8 \text{ mA}$					0.35	0.5
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1		0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		20	μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4		-0.4	mA
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$			-20	-100	-20	-100
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$			19	34	19	34

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

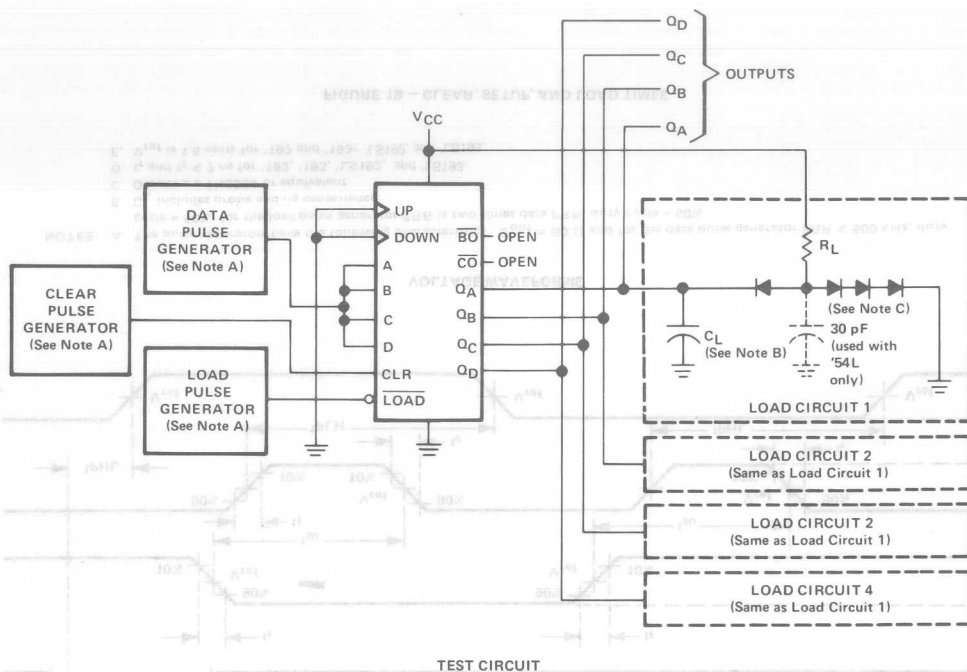
PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	32		MHz
t_{PLH}	UP	\overline{CO}		17	26		ns
t_{PHL}				18	24		
t_{PLH}	DOWN	\overline{BO}		16	24		ns
t_{PHL}				15	24		
t_{PLH}	UP OR DOWN	Q	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figures 1 and 2	27	38		ns
t_{PHL}				30	47		
t_{PLH}	LOAD	Q		24	40		ns
t_{PHL}				25	40		
t_{PHL}	CLR	Q		23	35		ns

3

TTL DEVICES

TYPES SN54192, SN54193, SN54LS192, SN54LS193
 SN74192, SN74LS193, SN74ALS192, SN74ALS193
 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. Diodes are 1N3064 or equivalent.
- D. t_r and $t_f \leq 7$ ns for '192, '193, 'LS192, and 'LS193.
- E. V_{ref} is 1.5 volts for '192 and '193; 'LS192, and 'LS193.

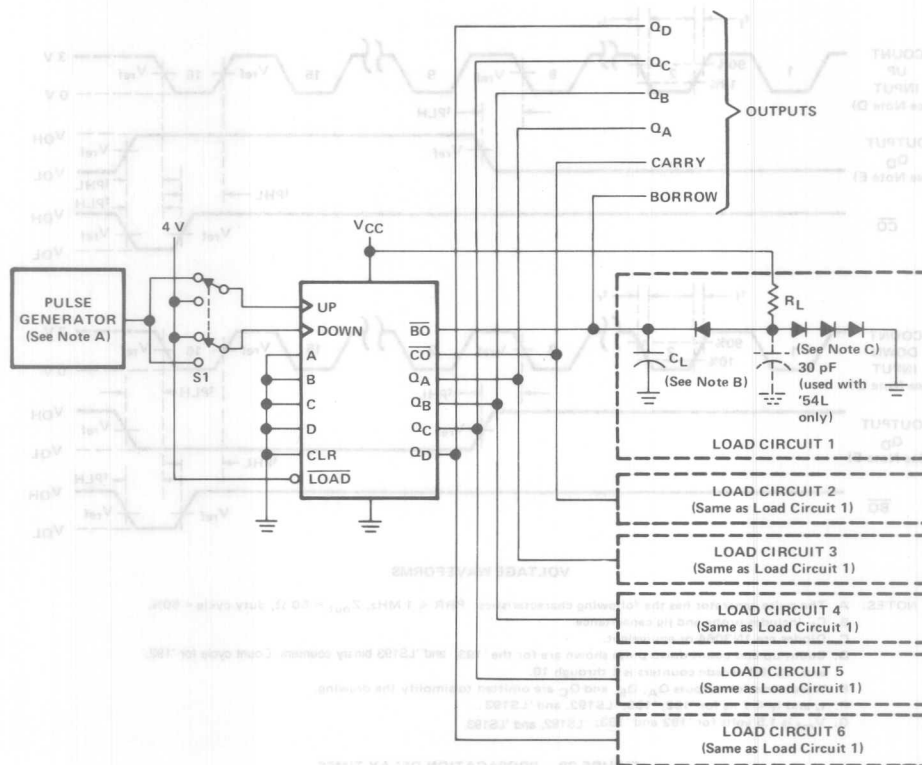
FIGURE 1A — CLEAR, SETUP AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

FIGURE 1B – CLEAR, SETUP, AND LOAD TIMES

**TYPES SN54192, SN54193, SN54LS192, SN54LS193
SN74192, SN74193, SN74LS192, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)**

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

- NOTES: A. The pulse generator has the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Count-up and count-down pulse shown are for the '193, and 'LS193 binary counters. Count cycle for '192, and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs Q_A , Q_B , and Q_C are omitted to simplify the drawing.
F. t_r and $t_f \leq 7 \text{ ns}$ for '192, '193, 'LS192, and 'LS193.
G. V_{ref} is 1.5 volts for '192 and '193; 'LS192, and 'LS193.

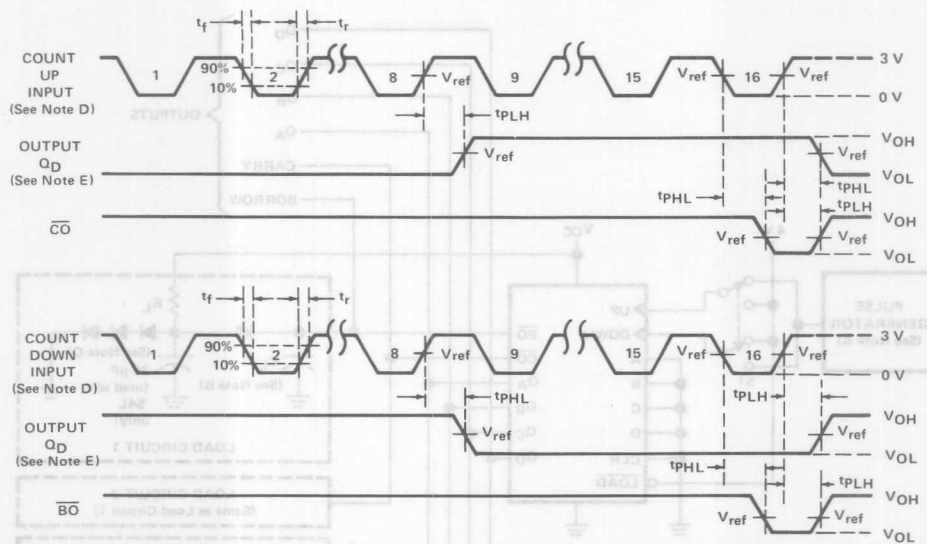
FIGURE 2A – PROPAGATION DELAY TIMES

3

TTL DEVICES

**TYPES SN54192, SN54193, SN54LS192, SN54LS193
SN74192, SN74193, SN74LS192, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)**

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Count-up and count-down pulse shown are for the '193, and 'LS193 binary counters. Count cycle for '192, and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs Q_A , Q_B , and Q_C are omitted to simplify the drawing.
F. t_r and $t_f \leq 7 \text{ ns}$ for '192, '193, 'LS192, and 'LS193.
G. V_{ref} is 1.5 volts for '192 and '193; 'LS192, and 'LS193.

FIGURE 2B – PROPAGATION DELAY TIMES

3

TTL DEVICES

TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

MARCH 1974—REVISED APRIL 1985

- Parallel Inputs and Outputs

- Four Operating Modes:

Synchronous Parallel Load
Right Shift
Left Shift
Do Nothing

- Positive Edge-Triggered Clocking

- Direct Overriding Clear

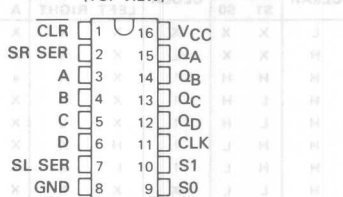
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

SN54194, SN54LS194A, SN54S194 ... J OR W PACKAGE

SN74194 ... J OR N PACKAGE

SN74LS194A, SN74S194 ... D, J OR N PACKAGE

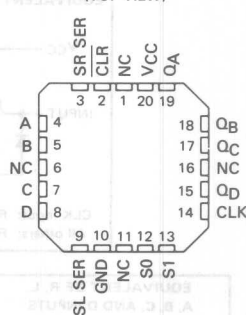
(TOP VIEW)



SN54LS194A, SN54S194 ... FK PACKAGE

SN74LS194A, SN74S194

(TOP VIEW)



NC - No internal connection

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Inhibit clock (do nothing)
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

PRODUCTION DATA

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TEXAS
INSTRUMENTS

3-645

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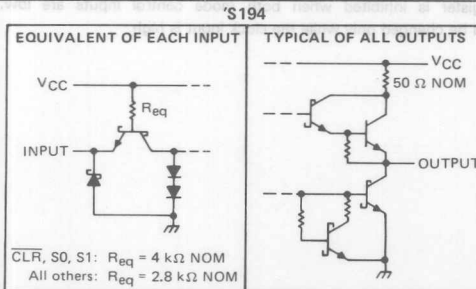
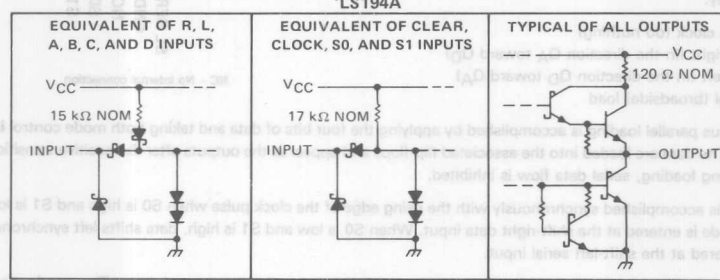
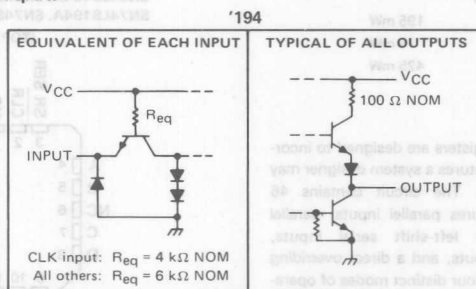
TTL DEVICES

**TYPES SN54194, SN54LS194A, SN54S194,
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

FUNCTION TABLE											
INPUTS			OUTPUTS								
CLEAR	MODE		CLOCK		SERIAL		PARALLEL				
	S1	S0			LEFT	RIGHT	A	B	C	D	
L	X	X	X	X	X	X	X	X	X	X	L
H	X	X	L	X	X	X	X	X	X	X	L
H	H	H	1	X	X	a	b	c	d		L
H	L	H	1	X	H	X	X	X	X	X	L
H	L	H	1	X	L	X	X	X	X	X	L
H	H	L	1	X	H	X	X	X	X	X	L
H	H	L	1	X	L	X	X	X	X	X	L
H	L	L	X	X	X	X	X	X	X	X	L

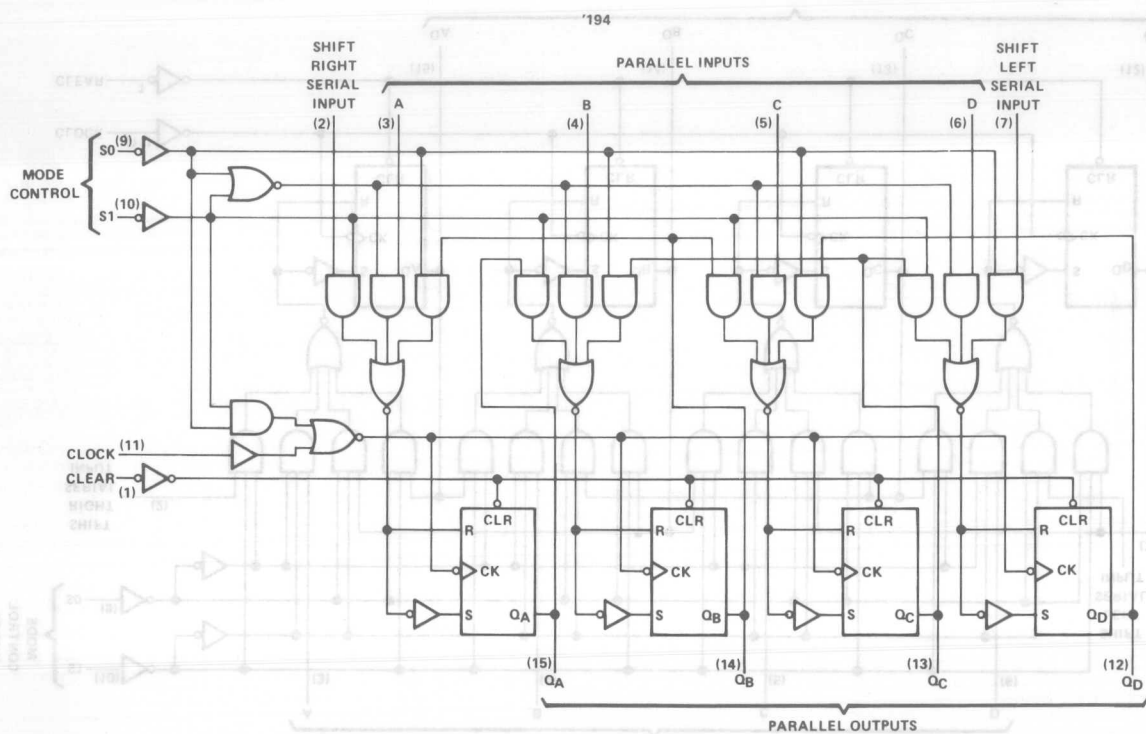
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
1 = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or $Q_D,$ respectively, before the indicated steady-state input conditions were established.
 $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ respectively, before the most recent 1 transition of the clock.

schematics of inputs and outputs



Logic diagrams

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS
TYPES SN54194, SN74194



Pin numbers shown on logic notation are for D, J or N packages.

TEXAS
INSTRUMENTS

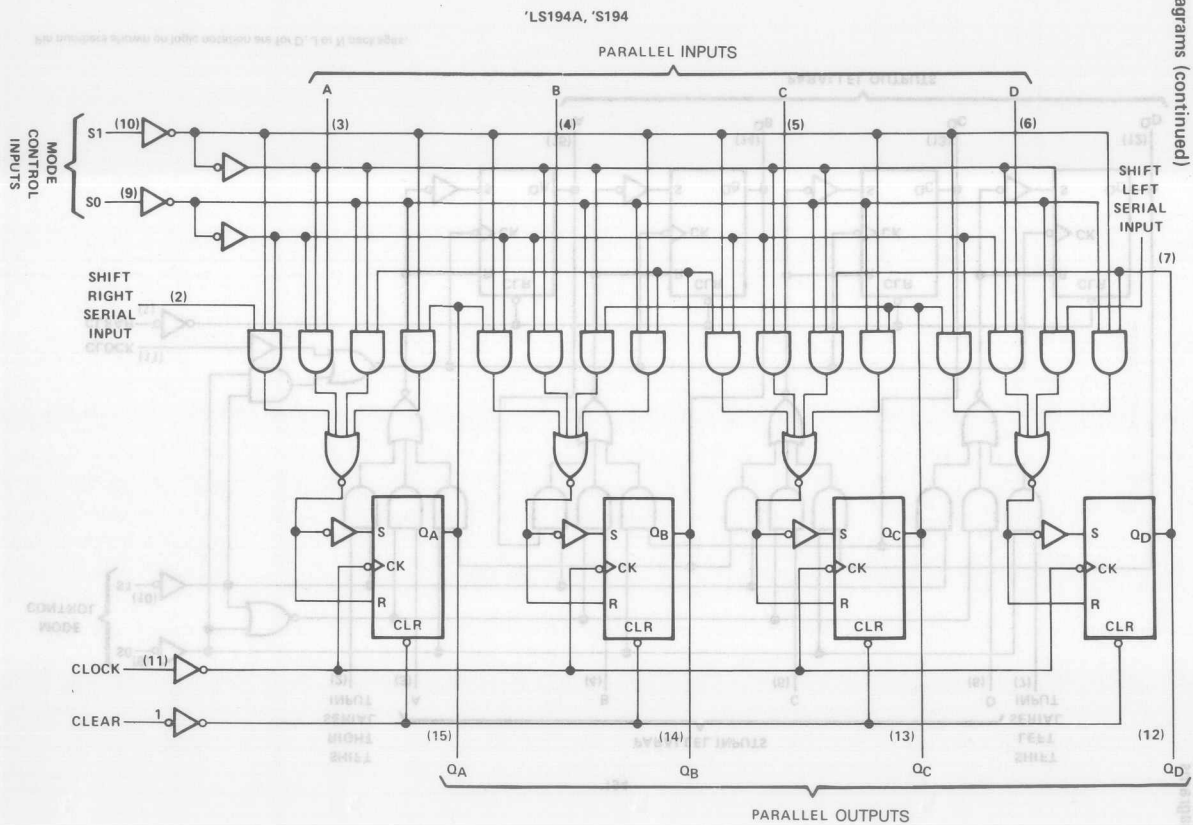
3-647

TTL DEVICES



TYPES SN54LS194A, SN54S194,
SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

Logic diagrams (continued)



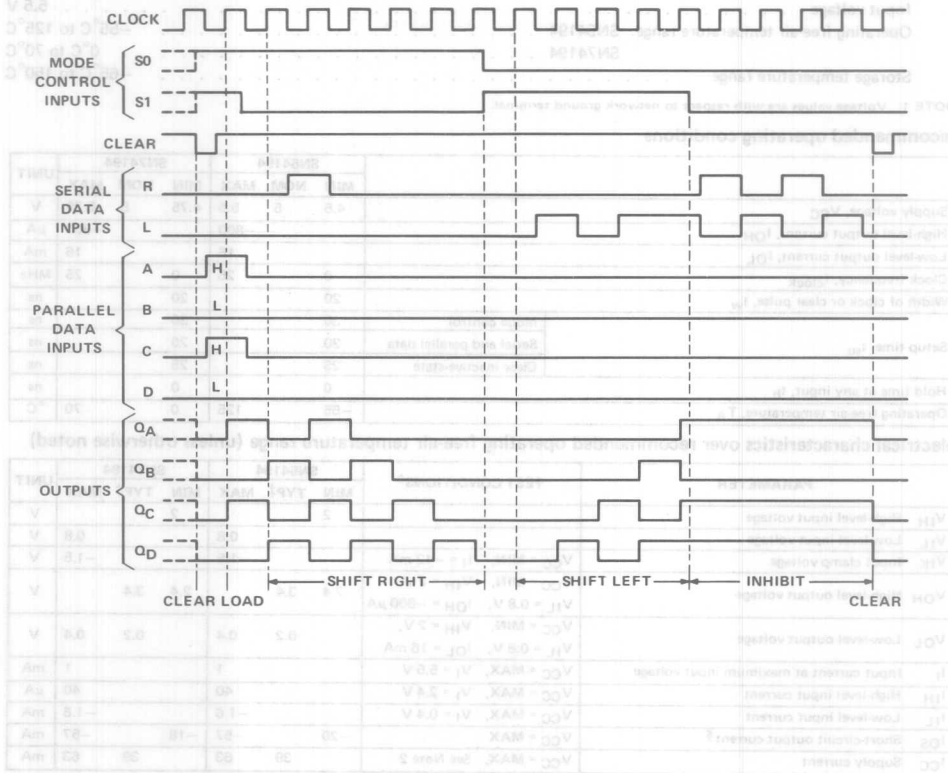
Pin numbers shown on logic notation are for D, J or N packages.

TTL DEVICES

3

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



3

TTL DEVICES

TYPES SN54194, SN74194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54194	-55°C to 125°C
SN74194	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54194			SN74194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_W		20			20			ns
Setup time, t_{SU}	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_H		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54194			SN74194			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	39		63	39		63	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1		19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns

TYPES SN54LS194A, SN74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS194A	-55°C to 125°C
SN74LS194A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS194A			SN74LS194A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w			20			20	ns
Setup time, t_{su}	Mode control			30			ns
	Serial and parallel data			20			ns
	Clear inactive-state			25			ns
Hold time at any input, t_h			0			0	ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS194A			SN74LS194A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		15	23		15	23	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	36		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF},$		19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clear	$R_L = 2 \text{ k}\Omega,$		14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	See Figure 1		17	26	ns

TYPES SN54S194, SN74S194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S194	-55°C to 125°C
SN74S194	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S194			SN74S194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Clock frequency, f_{clock}	0		70	0		70	MHz
Width of clock pulse, $t_{w(clock)}$	7			7			ns
Width of clear pulse, $t_{w(clear)}$	12			12			ns
Setup time, t_{SU}	Mode control			11			ns
	Serial and parallel data			5			ns
	Clear inactive-state			9			ns
Hold time at any input, t_H	3			3			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54S194			SN74S194			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		85	135		85	135	μA
	$V_{CC} = \text{MAX}, T_A = 125^\circ \text{C}, \text{ W package}$			110				mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applies to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

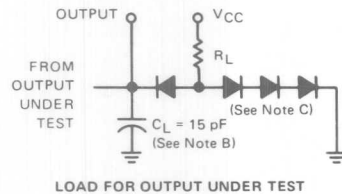
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		70	105		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$		12.5	18.5	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Figure 1	4	8	12	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock		4	11	16.5	ns

3

TTL DEVICES

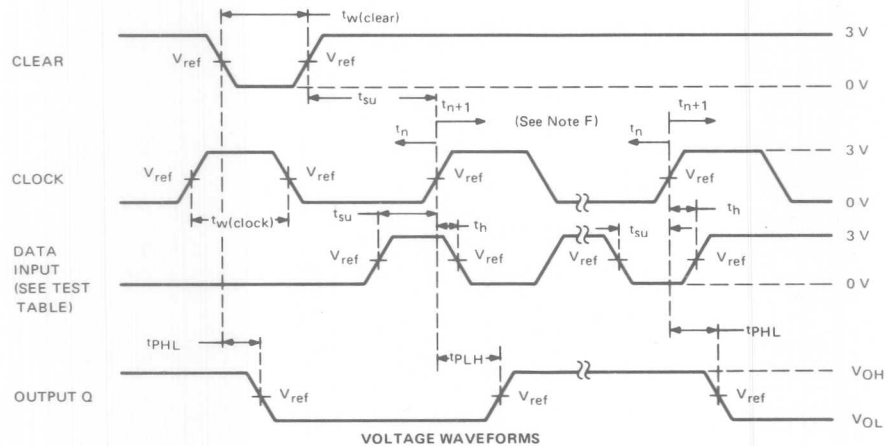
TYPES SN54194, SN54LS194A, SN54S194,
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	QA at t_{n+1}
B	4.5 V	4.5 V	QB at t_{n+1}
C	4.5 V	4.5 V	QC at t_{n+1}
D	4.5 V	4.5 V	QD at t_{n+1}
L Serial Input	4.5 V	0 V	QA at t_{n+4}
R Serial Input	0 V	4.5 V	QD at t_{n+4}



- NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$. For '194, $t_r \leq 7 \text{ ns}$ and $t_f \leq 7 \text{ ns}$. For 'LS194A, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. For 'S194, $t_r \leq 2.5 \text{ ns}$ and $t_f \leq 2.5 \text{ ns}$. When testing t_{max} , vary PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. A clear pulse is applied prior to each test.
- E. For '194 and 'S194, $V_{ref} = 1.5 \text{ V}$; for 'LS194A, $V_{ref} = 1.3 \text{ V}$.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

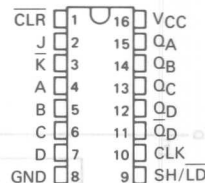
TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

MARCH 1974—REVISED APRIL 1985

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and K Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance:
Accumulators/Processors
Serial-to-Parallel, Parallel-to-Serial
Converters

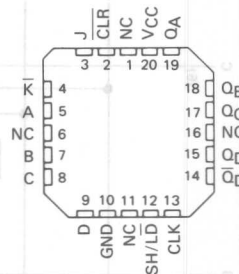
SN54195, SN54LS195A, SN54S195 ... J OR W PACKAGE
SN74195 ... J OR N PACKAGE
SN74LS195A, SN74S195 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS195, SN54S195 ... FK PACKAGE
SN74LS195, SN74S195

(TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'S195	105 MHz	350 mW

description

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

FUNCTION TABLE

		INPUTS				OUTPUTS				
		SHIFT/ LOAD	CLOCK	SERIAL	PARALLEL	Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
CLEAR				J	\bar{K}	A	B	C	D	
L	X	X	X	X	X	X	X	X	X	H
H	L	↑	X	X	a	b	c	d	\bar{a}	\bar{d}
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{D0}
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q_{An}
H	H	↑	H	H	X	X	X	X	H	Q_{An}
H	H	↑	H	L	X	X	X	X	\bar{Q}_{An}	Q_{Cn}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of Q_A, Q_B, Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established
 Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B , or Q_C , respectively, before the most-recent transition of the clock

PRODUCTION DATA

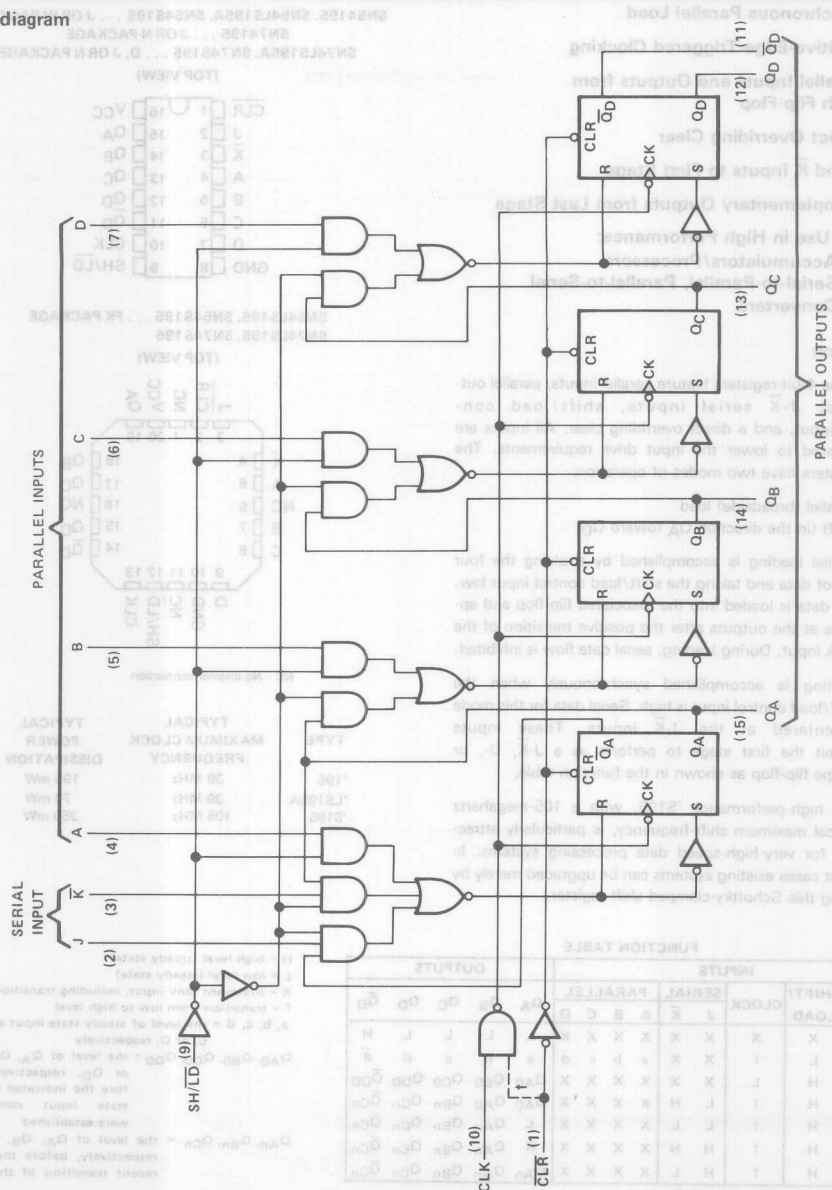
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3

TTL DEVICES

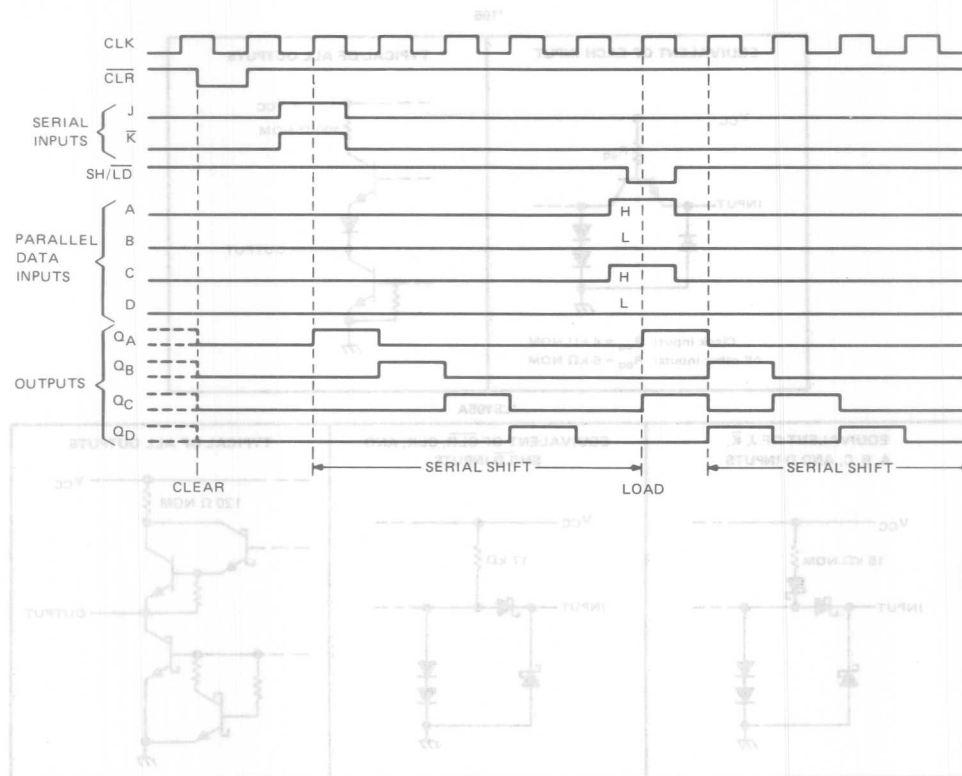
logic diagram



^fThis connection is made on '195 only.
Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

typical clear, shift, and load sequences



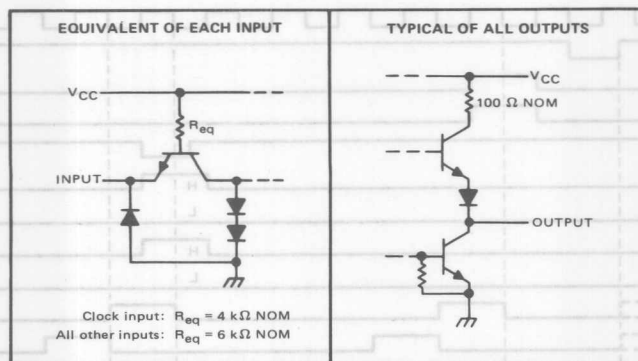
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TTL DEVICES

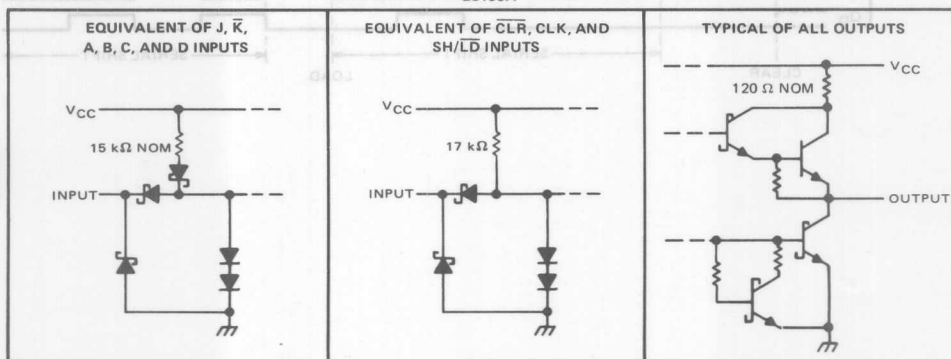
TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

schematics of inputs and outputs

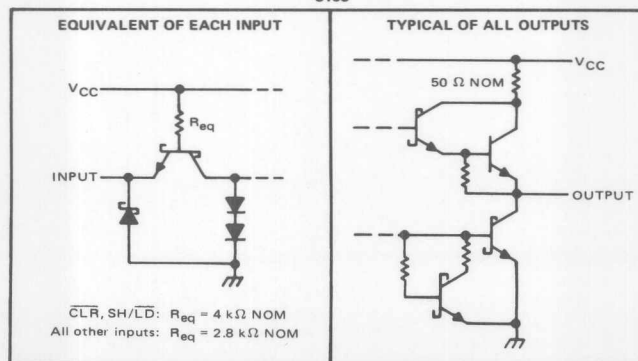
'195



'LS195A



'S195



3

TTL DEVICES

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54195	-55°C to 125°C
SN74195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54195			SN74195			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V _{CC}			4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I _{OH}			-800			-800			μA	
Low-level output current, I _{OL}			16			16			mA	
Clock frequency, f _{clock}			0	30		0	30		MHz	
Width of clock input pulse, t _{w(clock)}			16			16			ns	
Width of clear input pulse, t _{w(clear)}			12			12			ns	
Setup time, t _{su} (see Figure 1)	Shift/load		25			25			ns	
	Serial and parallel data		20			20				
	Clear inactive-state		25			25				
Shift/load release time, t _{release} (see Figure 1)			20			10			ns	
Serial and parallel data hold time, t _h (see Figure 1)			0			0			ns	
Operating free-air temperature, T _A			-55			125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54195 -20		57	mA
		SN74195 -18		57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2		.39	.63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF},$		19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	$R_L = 400 \Omega,$		14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	See Figure 1		17	26	ns

TYPES SN54LS195A, SN74LS195A 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

V_{CC} Supply voltage, V_{CC} (see Note 1)	7 V
V_{IH} Input voltage	7 V
Operating free-air temperature range: SN54LS195A	–55°C to 125°C
SN74LS195A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS195A			SN74LS195A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}					–400			–400	μA
Low-level output current, I _{OL}					4			8	mA
Clock frequency, f _{clock}			0		30	0		30	MHz
Width of clock or clear pulse, t _W (clock)			16			16			ns
Width of clear input pulse, t _W (clear)			12			12			ns
Setup time, t _{su} (see Figure 1)	Shift/load		25			25			ns
	Serial and parallel data		15			15			
	Clear inactive-state		25			25			
Shift/load release time, t _{release} (see Figure 1)					20			20	ns
Serial and parallel data hold time, t _h (see Figure 1)			0			0			ns
Operating free-air temperature, T _A			–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS195A			SN74LS195A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \text{ μA}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–0.4			–0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	14		21	14		21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$	30	39		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$R_L = 2 \text{ k}\Omega$		19	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Figure 1		14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			17	26	ns

TYPES SN54S195, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S195	-55°C to 125°C
SN74S195	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54S195			SN74S195			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					-1			-1	mA
Low-level output current, I_{OL}					20			20	mA
Clock frequency, f_{clock}			0		70	0		70	MHz
Width of clock input pulse, $t_w(\text{clock})$			7			7			ns
Width of clear input pulse, $t_w(\text{clear})$			12			12			ns
Setup time, t_{su} (see Figure 1)			Shift/load			11			ns
			Serial and parallel data			5			
			Clear inactive-state			9			
Shift/load release time, $t_{release}$ (see Figure 1)					6			6	ns
Serial and parallel data hold time, t_h (see Figure 1)			3			3			ns
Operating free-air temperature, T_A			-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54S195	70	99	mA
		SN74S195	70	109	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

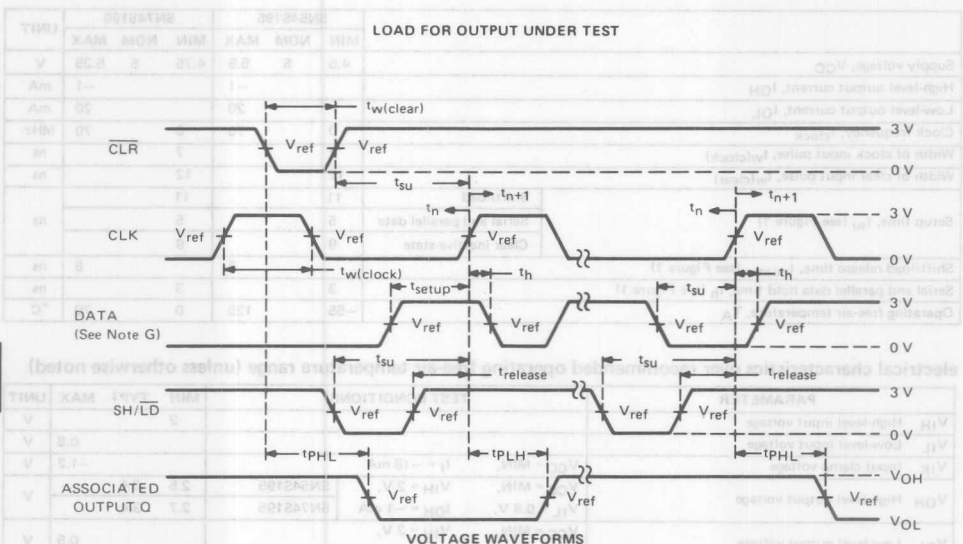
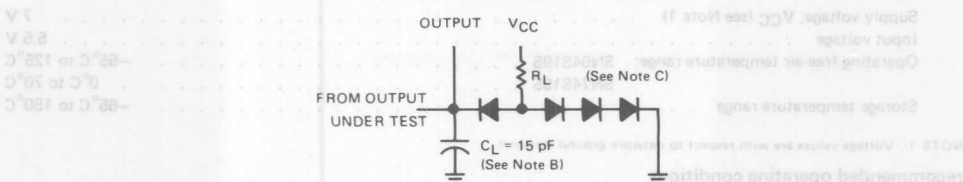
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$ $R_L = 280 \Omega,$ See Figure 1	70	105		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			11	16.5	ns

**TYPES SN54195, SN54LS195A, SN54S195,
SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

PARAMETER MEASUREMENT INFORMATION



- NOTES:** A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$. For '195, $t_r \leq 7 \text{ ns}$ and $t_f \leq 7 \text{ ns}$. For 'LS195A, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. For 'S195, $t_r = 2.5 \text{ ns}$ and $t_f = 2.5 \text{ ns}$. When testing f_{max} , vary the clock PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. A clear pulse is applied prior to each test.
- E. For '195 and 'S195, $V_{ref} = 1.5 \text{ V}$; for 'LS195A, $V_{ref} = 1.3 \text{ V}$.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
- H. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock frequency		10			MHz
Propagation delay time, low-level output from clock	$C_L = 15 \text{ pF}$	10	15	20	ns
Propagation delay time, high-level output from clock	$C_L = 15 \text{ pF}$	10	15	20	ns
Propagation delay time, low-level output from data	$C_L = 15 \text{ pF}$	10	15	20	ns
Propagation delay time, high-level output from data	$C_L = 15 \text{ pF}$	10	15	20	ns

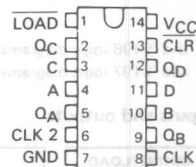
TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197, SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197 50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

OCTOBER 1976 - REVISED APRIL 1985

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output QA Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

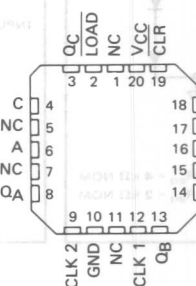
SN54196, SN54LS196, SN54S196
SN54197, SN54LS197, SN54S197 ... J OR W PACKAGE
SN74196, SN74197 ... J OR N PACKAGE
SN74LS196, SN74S196, SN74LS197, SN74S197 ... D, J OR N PACKAGE

(TOP VIEW)



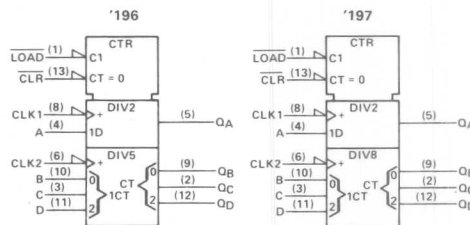
SN54LS196, SN54S196, SN54LS197, SN54S197, SN74LS196, SN74S196
SN74LS197, SN74S197 ... FK PACKAGE

(TOP VIEW)



NC - No internal connection

logic symbols†



†Pin numbers shown on logic notation are for D, J or N packages.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops, which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196, 'S196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197, 'S197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL logic families. Series 54, 54LS, and 54S circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, 74LS, and 74S circuits are characterized for operation from 0°C to 70°C.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-663

3

TTL DEVICES

**TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197,
SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES**

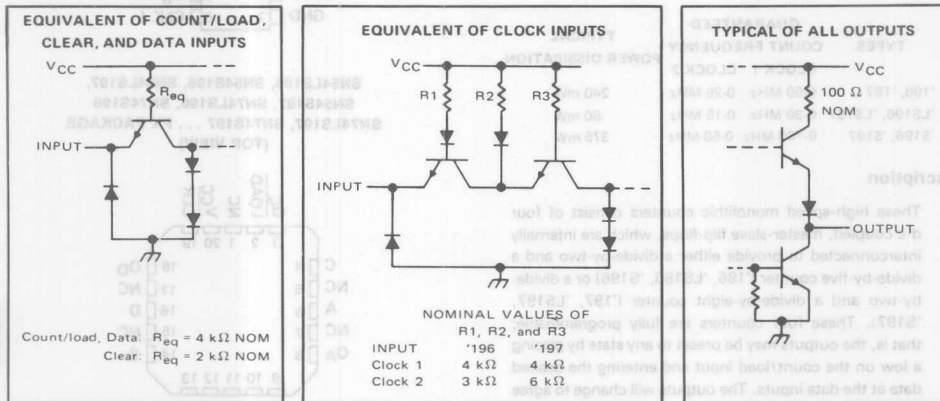
typical count configurations

'196, 'LS196, and 'S196 typical count configurations and function tables are the same as those for '176.
'197, 'LS197, and 'S197 typical count configurations and function tables are the same as those for '177.

logic diagrams

'196, 'LS196, and 'S196 logic diagrams are the same as those for '176.
'197, 'LS197, and 'S197 logic diagrams are the same as those for '177.

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54196, SN54197, SN74196, SN74197 50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits	-55°C to 125°C
SN74196, SN74197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		SN54196, SN54197			SN74196, SN74197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Count frequency	Clock-1 input	0		50	0		50	MHz
	Clock-2 input	0		25	0		25	
Pulse width, t_w	Clock-1 input	10			10			ns
	Clock-2 input	20			20			
	Clear	15			15			
	Load	20			20			
Input hold time, t_h	High-level data	$t_w(\text{load})$			$t_w(\text{load})$			ns
	Low-level data	$t_w(\text{load})$			$t_w(\text{load})$			
Input setup time, t_{su} (see Note 4)	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{en} (see Note 3)		20			20			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

NOTES: 3. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.
4. t_{su} is measured with respect to load input.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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TYPES SN54196, SN54197, SN74196, SN74197
50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54196, SN74196			SN54197, SN74197			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage			0.8			0.8		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA		-1.5			-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶	0.2	0.4		0.2	0.4		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	Data, count/load		40			40		µA
	Clear, clock 1	V _{CC} = MAX, V _I = 2.4 V				80		
	Clock 2					120		
I _{IL} Low-level input current	Data, count/load		-1.6			-1.6		mA
	Clear	V _{CC} = MAX, V _I = 0.4 V				-3.2		
	Clock 1					-4.8		
	Clock 2					-6.4		
I _{OS} Short-circuit output current §	V _{CC} = MAX	SN54'	-20	-57	-20	-57		mA
		SN74'	-18	-57	-18	-57		
I _{CC} Supply current	V _{CC} = MAX, See Note 5		48	59		48	59	mA

NOTE 5: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25° C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54196 SN74196			SN54197 SN74197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Clock 1	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 6	50	70		50	70		MHz
t _{PLH}	Clock 1	Q _A		7	12		7	12		ns
t _{PHL}				10	15		10	15		
t _{PLH}	Clock 2	Q _B		12	18		12	18		ns
t _{PHL}				14	21		14	21		
t _{PLH}	Clock 2	Q _C		24	36		24	36		ns
t _{PHL}				28	42		28	42		
t _{PLH}	Clock 2	Q _D		14	21		36	54		ns
t _{PHL}				12	18		42	63		
t _{PLH}	A, B, C, D	Q _A , Q _B , Q _C , Q _D		16	24		16	24		ns
t _{PHL}				25	38		25	38		
t _{PLH}	Load	Any		22	33		22	33		ns
t _{PHL}				24	36		24	36		
t _{PHL}	Clear	Any		25	37		25	37		ns

◇f_{max} = maximum count frequency.

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

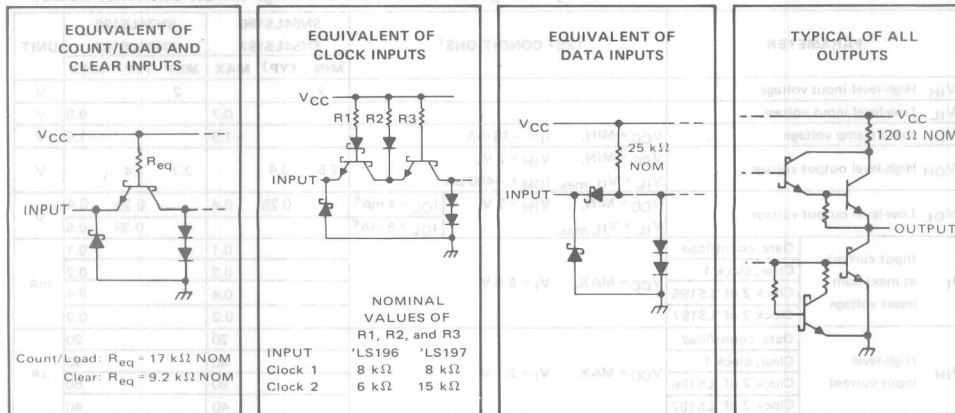
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that testing f_{max}, V_{IL} = 0.3 V.

3

TTL DEVICES

TYPES SN54LS196, SN54LS197, SN74LS196, SN74LS197 30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54LS196, SN54LS197 Circuits	-55°C to 125°C
SN74LS196, SN74LS197 Circuits	0°C to 70°C
Storage temperature range	65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

TIME	TEST CONDITIONS	UNIT	SN54LS196, SN54LS197			SN74LS196, SN74LS197			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current				-400			-400	μA
I _{OL}	Low-level output current				4			8	mA
	Count frequency	Clock-1 input	0	30	0	30	MHz		
		Clock-2 input	0	15	0	15			
t _w	Pulse width	Clock-1 input	20		20	ns			
		Clock-2 input	30		30				
		Clear	15		15				
		Load	20		20				
t _h	Input hold time	High-level data	10		10	ns			
		Low-level data	10		10				
t _{su}	Input setup time	High-level data	10		10	ns			
		Low-level data	15		15				
t _{enable}	Count enable time (see Note 3)	Clock 1	30		30	ns			
		Clock 2	50		50				
T _A	Operating free-air temperature		-55	125	0	70	°C		

NOTE 3: Minimum count enable time is the interval immediately preceding the negative going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

TYPES SN54LS196, SN54LS197, SN74LS196, SN74LS197
30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS196 SN54LS197			SN74LS196 SN74LS197			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}^{\S}, I_{OL} = 8 \text{ mA}^{\S}$	0.25	0.4		0.25	0.4	0.35 0.5	V
I_I Input current at maximum input voltage	Data, count/load			0.1			0.1	mA
	Clear, clock 1			0.2			0.2	
	Clock 2 of 'LS196			0.4			0.4	
	Clock 2 of 'LS197			0.2			0.2	
I_{IH} High-level input current	Data, count/load			20			20	μA
	Clear, clock 1			40			40	
	Clock 2 of 'LS196			80			80	
	Clock 2 of 'LS197			40			40	
I_{IL} Low-level input current	Data, count/load			-0.4			-0.4	mA
	Clear			-0.8			-0.8	
	Clock 1			-2.4			-2.4	
	Clock 2 of 'LS196			-2.8			-2.8	
	Clock 2 of 'LS197			-1.3			-1.3	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 4	16	27		16	27		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock 2 input. This permits driving the clock 2 input while maintaining full fan-out capability.

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS196 SN74LS196			SN54LS197 SN74LS197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 5	30	40		30	40		MHz
t_{PLH}	Clock 1	Q_A		8	15		8	15		ns
t_{PHL}				13	20		14	21		
t_{PLH}	Clock 2	Q_B		16	24		12	19		ns
t_{PHL}				22	33		23	35		
t_{PLH}	Clock 2	Q_C		38	57		34	51		ns
t_{PHL}				41	62		42	63		
t_{PLH}	Clock 2	Q_D		12	18		55	78		ns
t_{PHL}				30	45		63	95		
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		20	30		18	27		ns
t_{PHL}				29	44		29	44		
t_{PLH}	Load	Any		27	41		26	39		ns
t_{PHL}				30	45		30	45		
t_{PHL}	Clear	Any	34	51		34	51		ns	

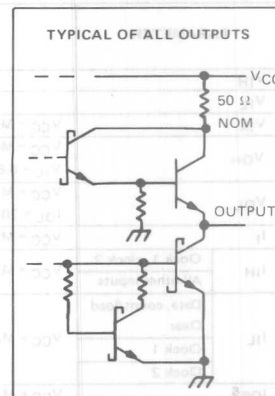
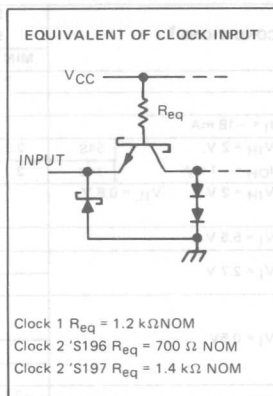
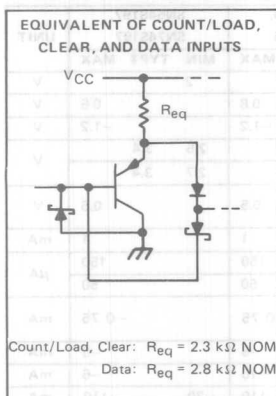
† f_{max} = maximum count frequency

‡ t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output

NOTE 5: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that $t_r \leq 15 \text{ ns}, t_f \leq 6 \text{ ns}$, and $V_{\text{ref}} = 1.3 \text{ V}$ (as opposed to 1.5 V)

TYPES SN54S196, SN54S197, SN74S196, SN74S197 100-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S196, SN54S197 Circuits	-55°C to 125°C
SN74S196, SN74S197 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S196, SN54S197			SN74S196, SN74S197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency	Clock-1 input	0		100	0		100	MHz
	Clock-2 input	0		50	0		50	
Pulse width, t_W	Clock-1 input	5			5			
	Clock-2 input	10			10			
	Clear	30			30			ns
	Load	5			5			
Input hold time, t_H	High-level data	3↑			3↑			ns
	Low-level data	3↑			3↑			
Input setup time, t_{SU} (see Note 6)	High-level data	6↑			6↑			ns
	Low-level data	6↑			6↑			
Count enable time, t_{EN} (see Note 2)		12			12			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

NOTES: 2. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs are both high to permit counting.

6. t_{SU} is measured with respect to load input.

TYPES SN54S196, SN54S197, SN74S196, SN74S197
100-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S196, SN74S196			SN54S197, SN74S197			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IH}		2			2			V
V _{IL}				0.8			0.8	V
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	54S 2.5	3.4		54S 2.5	3.4		V
V _{OL}	V _{CC} = MIN, I _{OL} = 20 mA, V _{IH} = 2 V, V _{IL} = 0.8 V	74S 2.7	3.4		74S 2.7	3.4		V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	Clock 1, clock 2			150			150	µA
	All other inputs			50			50	µA
I _{IL}	Data, count/load Clear			-0.75			-0.75	mA
	Clock 1			-8			-8	mA
	Clock 2			-10			-6	mA
I _{OS} §	V _{CC} = MAX			-30			-110	mA
I _{CC}	V _{CC} = MAX, See Note 3	54S 75	110		54S 75	110		mA
		74S 75	120		74S 75	120		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Q_A outputs are tested at I_{OL} = 20 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54S/74S loads.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with all inputs grounded and all outputs open.

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TTL DEVICES

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	(FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S196, SN74S196			SN54S197, SN74S197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Clock 1	Q _A		100	140		100	140		MHz
t _{PLH}	Clock 1	Q _A		5	10		5	10		ns
t _{PHL}	Clock 1	Q _A		6	10		6	10		ns
t _{PLH}	Clock 2	Q _B		5	10		5	10		ns
t _{PHL}	Clock 2	Q _B		8	12		8	12		ns
t _{PLH}	Clock 2	Q _C		12	18		12	18		ns
t _{PHL}	Clock 2	Q _C		16	24		15	22		ns
t _{PLH}	Clock 2	Q _D		5	10		18	27		ns
t _{PHL}	Clock 2	Q _D		8	12		22	33		ns
t _{PLH}	A,B,C,D	Q _A ,Q _B ,Q _C ,Q _D		7	12		7	12		ns
t _{PHL}	A,B,C,D	Q _A ,Q _B ,Q _C ,Q _D		12	18		12	18		ns
t _{PLH}	Load	Any		10	18		10	18		ns
t _{PHL}	Load	Any		12	18		12	18		ns
t _{PHL}	Clear	Any		26	37		26	37		ns

◊ f_{max} = maximum input county frequency.

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TYPES SN54198, SN54199, SN74198, SN74199 8-BIT SHIFT REGISTERS

DECEMBER 1972—REVISED DECEMBER 1983

description

These 8-bit shift registers are compatible with most other TTL and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 devices are characterized for operation from 0°C to 70°C .

SN54198 and SN74198

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Inhibit Clock (Do nothing)
- Shift Right (In the direction Q_A toward Q_H)
- Shift Left (In the direction Q_H toward Q_A)
- Parallel (Broadside) Load

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1 , high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

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FUNCTION TABLE

CLEAR	INPUTS					OUTPUTS			
	MODE		CLOCK	SERIAL		PARALLEL	Q_A	Q_B ... Q_G	Q_H
	S_1	S_0		LEFT	RIGHT				
L	X	X	X	X	X	X	L	L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	H	H	↑	X	X	a ... h	a	b	g h
H	L	H	↑	X	H	X	H	Q_{An}	Q_{Fn} Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}	Q_{Fn} Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn} Q_{Cn}	Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn} Q_{Cn}	Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0} Q_{B0}	Q_{G0} Q_{H0}	

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a ... h = the level of steady-state input at inputs A thru H, respectively.

Q_{A0} , Q_{B0} , Q_{G0} , Q_{H0} = the level of Q_A , Q_B , Q_G , or Q_H , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , etc. = the level of Q_A , Q_B , etc., respectively, before the most-recent ↑ transition of the clock.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-671

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TTL DEVICES

TYPES SN54199, SN54198, SN74198, SN74199 8-BIT SHIFT REGISTERS

SN54199 and SN74199

These registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

- Inhibit Clock (Do nothing)
- Shift (In the direction Q_A toward Q_H)
- Parallel (Broadside) Load

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

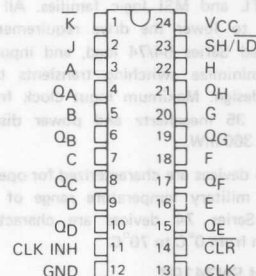
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-K inputs. See the function table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

SN54199 . . . J OR W PACKAGE SN74199 . . . J OR N PACKAGE

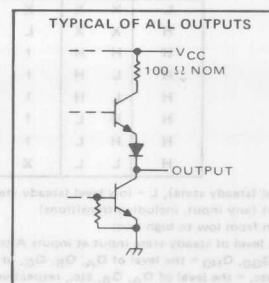
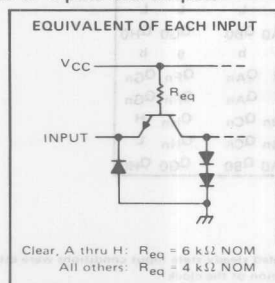
(TOP VIEW)



FUNCTION TABLE

INPUTS						OUTPUTS			
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL J K	PARALLEL A . . . H	Q_A	Q_B	Q_C	Q_H
L	X	X	X	X X	X	L	L	L	L
H	X	L	L	X X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}
H	L	L	L	X X	a . . . h	a	b	c	h
H	H	L	L	L H	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Gn}
H	H	L	L	L L	X	L	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	L	H H	X	H	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	L	H L	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}
H	X	H	L	X X	X	Q_{A0}	Q_{B0}	Q_{B0}	Q_{H0}

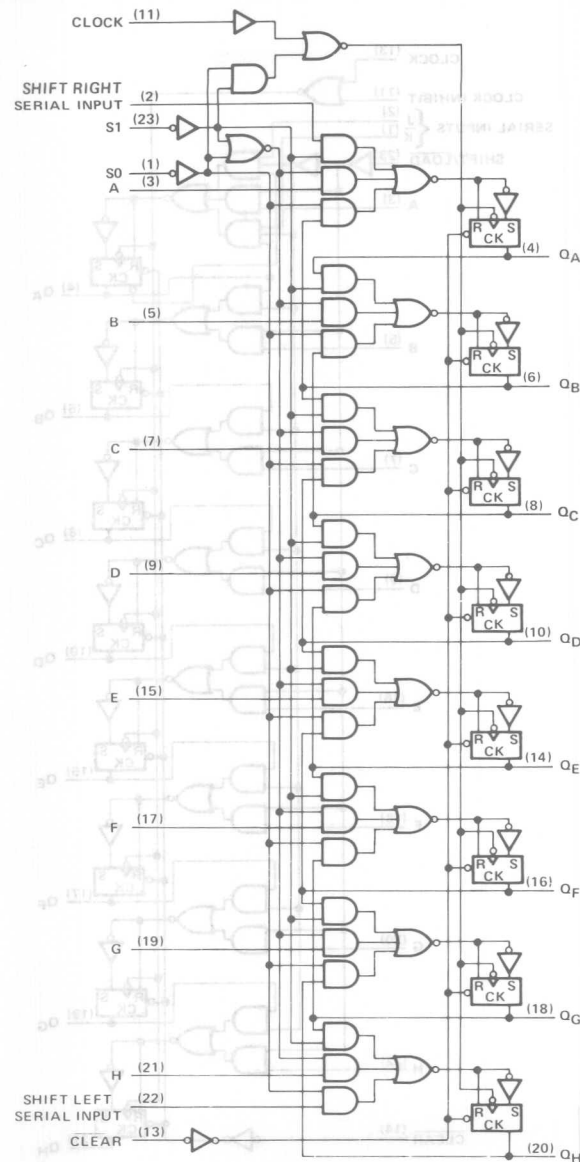
schematics of inputs and outputs



TYPES SN54198, SN74198
8-BIT SHIFT REGISTERS

logic diagram

'198



Pin numbers shown on logic notation are for J or N packages.

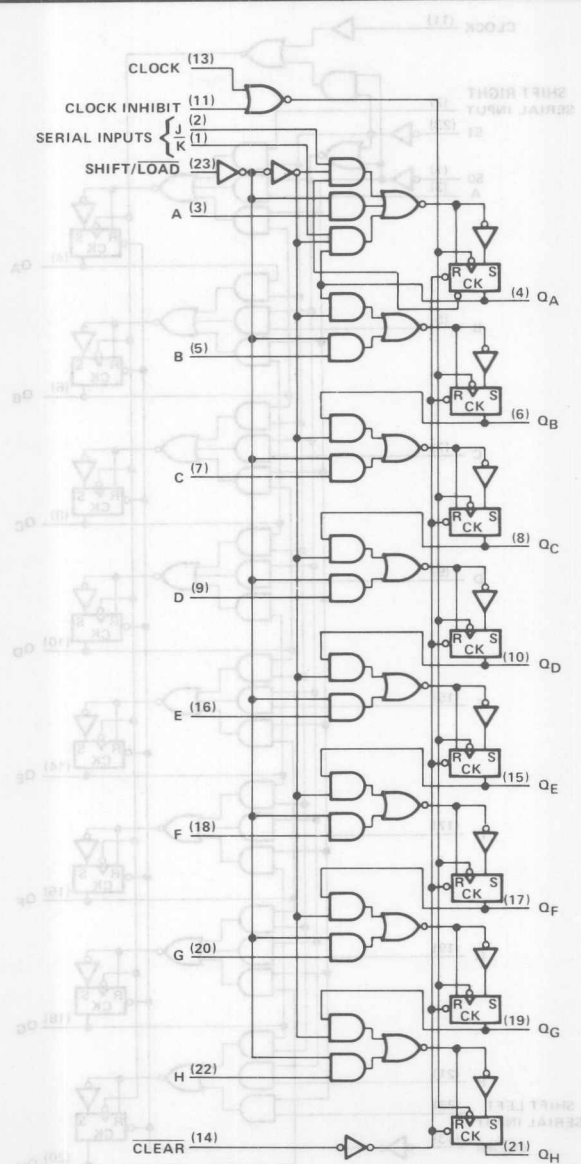
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TTL DEVICES

TYPES SN54199, SN74199 8-BIT SHIFT REGISTERS

logic diagram

'199



Pin numbers shown on logic notation are for J or N packages.

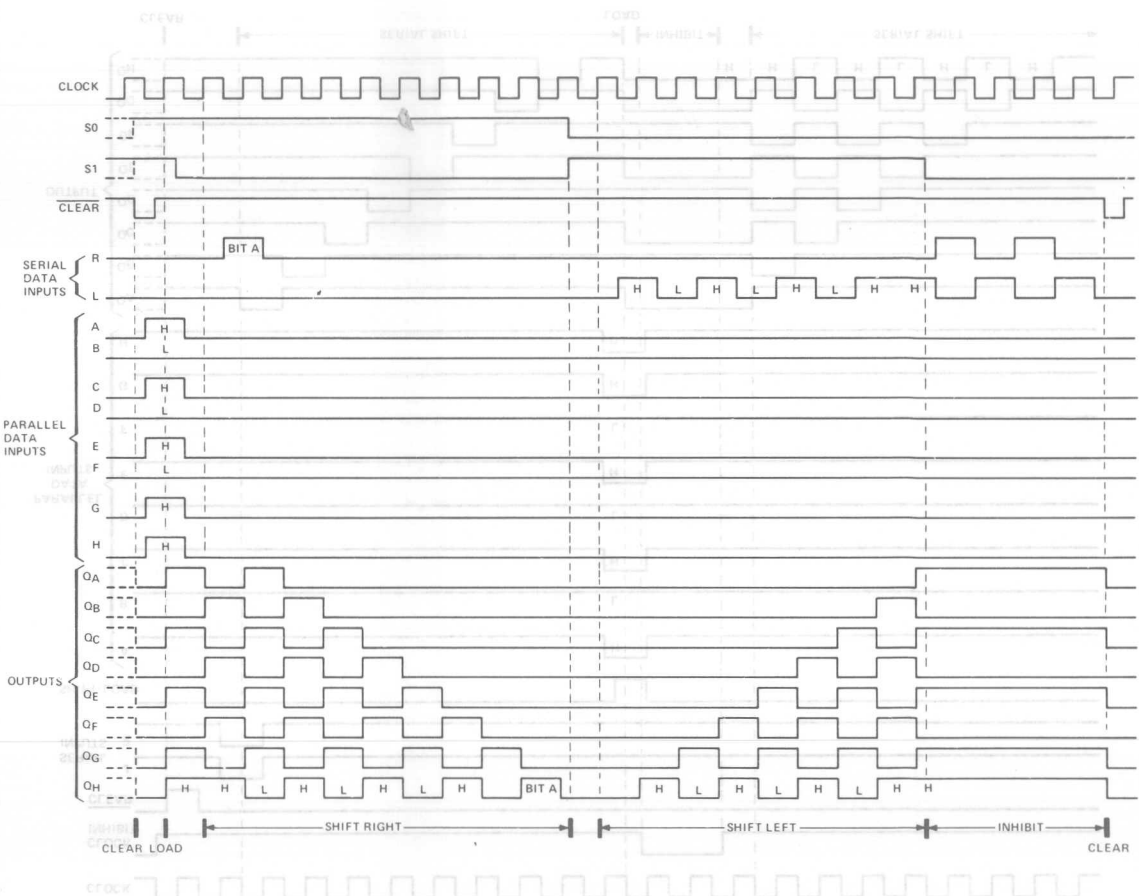
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TTL DEVICES

**TYPES SN54198, SN74198
8-BIT SHIFT REGISTERS**

SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



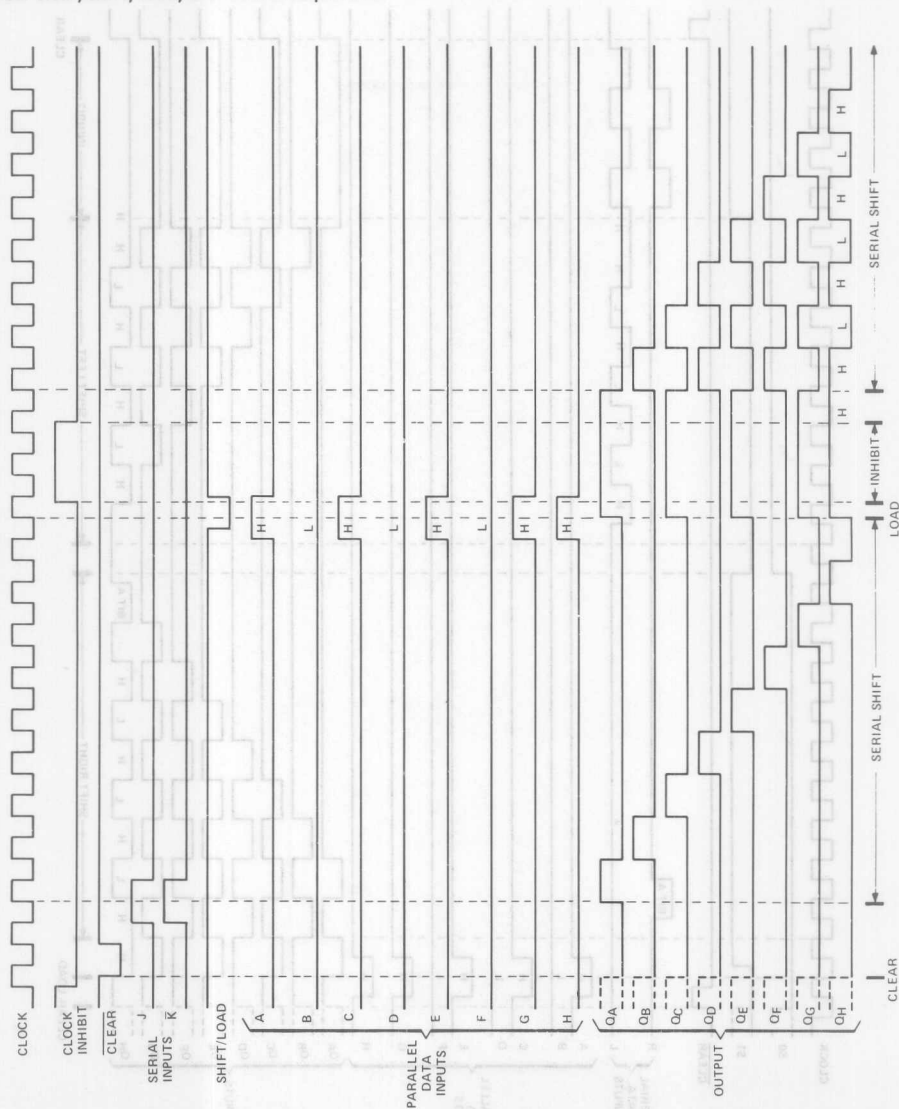
TTL DEVICES

3

TYPES SN54199, SN74199 8-BIT SHIFT REGISTERS

SN54199, SN74199

typical clear, shift, load, and inhibit sequences



3

TTL DEVICES

TYPES SN54198, SN54199, SN74198, SN74199 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54198 SN54199			SN74198 SN74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W (see Figure 1)	20			20			ns
Mode-control setup time, t_{SU}	30			30			ns
Data setup time, t_{SU} (see Figure 1)	20			20			ns
Hold time at any input, t_H (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54198 SN54199			SN74198 SN74199			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Table Below	90		127	90		127	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN)

TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54198, SN74198	Serial Input, S_0, S_1	Clock	Clear, Inputs A thru H
SN54199, SN74199	J, K, Inputs A thru H	Clock	Clock inhibit, Clear, Shift/Load

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max}	Maximum clock frequency		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1		23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	26	ns

TTL DEVICES

TYPES SN54198, SN54199, SN74198, SN74199 8-BIT SHIFT REGISTERS

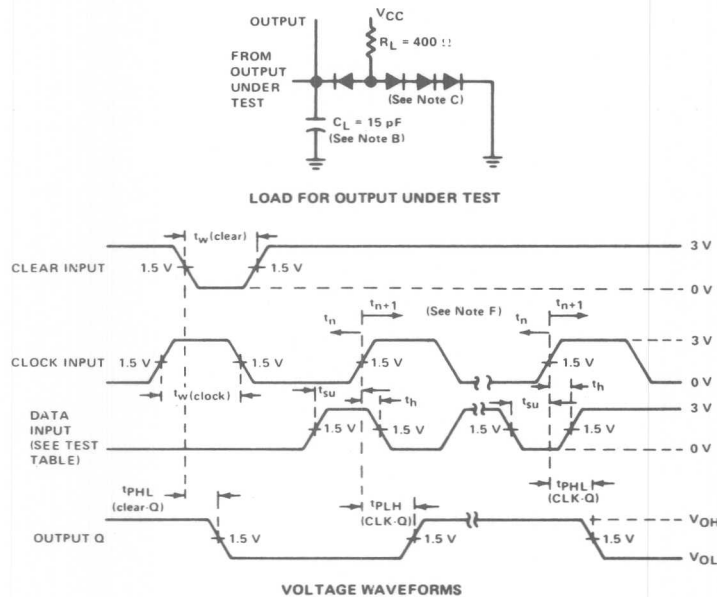
PARAMETER MEASUREMENT INFORMATION

SN54198, SN74198
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

SN54199, SN74199
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and \bar{K}	4.5 V	Q_H at t_{n+8}



- NOTES: A. The clock pulse has the following characteristics: $t_w(\text{clock}) \geq 20$ ns and $\text{PRR} = 1$ MHz. The clear pulse has the following characteristics: $t_w(\text{clear}) \geq 20$ ns and $t_{\text{hold}} = 0$ ns. When testing f_{max} , vary the clock PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064.
- D. A clear pulse is applied prior to each test.
- E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+8} with a functional test.
- F. t_n = bit time before clocking transition
 t_{n+1} = bit time after one clocking transition
 t_{n+8} = bit time after eight clocking transitions

FIGURE 1

TYPES SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

REVISED DECEMBER 1983

- **SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip**

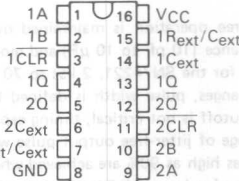
- **SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots**

- **Pin-Out Is Identical to the SN54123, SN74123, SN54LS123, SN74LS123**

- **Overriding Clear Terminates Output Pulse**

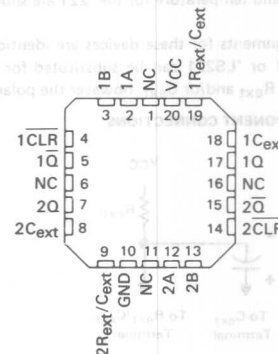
SN54221, SN54LS221 ... J OR W PACKAGE
SN74221 ... J OR N PACKAGE
SN74LS221 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS221 ... FK PACKAGE
SN74LS221

(TOP VIEW)



description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to VCC noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With $R_{ext} = 2 \text{ k}\Omega$ and $C_{ext} = 0$, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

FUNCTION TABLE
(EACH MONOSTABLE)

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌋	⌋
H	↑	H	⌋	⌋
↑ *	L	H	⌋	⌋

Also see description and switching characteristics

* This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logical "1" state prior to CLR going high. This latch is conditioned by taking either A high or B low which CLR is in the inactive state.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

description (continued)

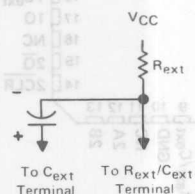
Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54221, 2 k Ω to 40 k Ω for the SN74221, 2 k Ω to 70 k Ω for the SN54LS221, and 2 k Ω to 100 k Ω for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_w(out) = C_{ext}R_{ext} \ln 2 \approx 0.7 C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

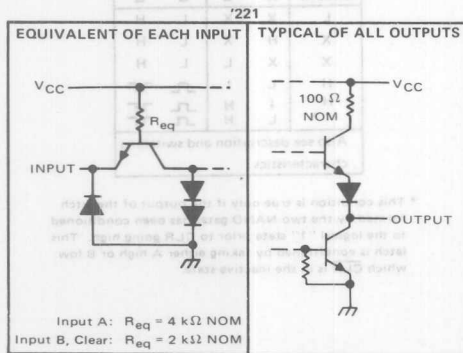
Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} , however the polarity of the capacitor will have to be changed.

TIMING COMPONENT CONNECTIONS

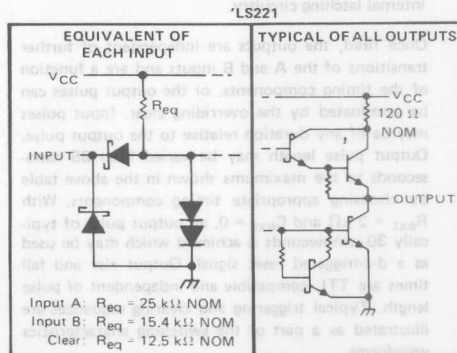
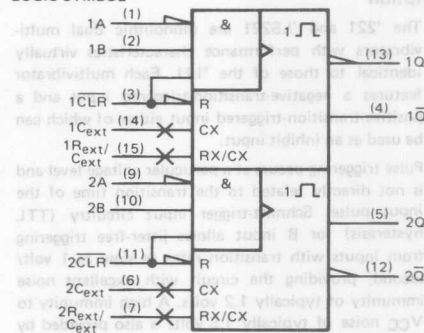


NOTE: Due to the internal circuit, the R_{ext}/C_{ext} pin will never be more positive than the C_{ext} pin.
Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



LOGIC SYMBOL



ISS TYPES SN54221, SN74221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/ μ s
Input pulse width	A or B, $t_{W(in)}$	50			50			ns
	Clear, $t_{W(clear)}$	20			20			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		30	1.4		40	k Ω
External timing capacitance, C_{ext}		0		1000	0		1000	μ F
Output duty cycle	$R_{ext} = 2 \text{ k}\Omega$			67			67	%
	$R_{ext} = \text{MAX } R_{ext}$			90			90	
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	$V_{CC} = \text{MIN}$			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	$V_{CC} = \text{MIN}$		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	$V_{CC} = \text{MIN}$			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	$V_{CC} = \text{MIN}$		0.8	1.35		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -800 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$	Input A			40	μ A
			Input B, Clear			80	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	Input A			-1.6	mA
			Input B, Clear			-3.2	
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54221	-20		-55	mA
			SN74221	-18		-55	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$	Quiescent		26	50	mA
			Triggered		46	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1 and Note 2	$C_{ext} = 80 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$		45	70	ns
	B	Q				35	55	
t_{PHL}	A	\bar{Q}				50	80	ns
	B	\bar{Q}				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	\bar{Q}					40	ns
$t_{W(out)}$	A or B	Q or \bar{Q}		$C_{ext} = 80 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$	70	110	150	ns
				$C_{ext} = 0$, $R_{ext} = 2 \text{ k}\Omega$	20	30	50	
				$C_{ext} = 100 \text{ pF}$, $R_{ext} = 10 \text{ k}\Omega$	650	700	750	
				$C_{ext} = 1 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	6.5	7	7.5	ms

¶ t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

$t_{W(out)}$ = Output pulse width

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μ A
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/ μ s
Input pulse width	A or B, $t_{W(in)}$	50			50			ns
	Clear, $t_{W(clear)}$	40			40			ns
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	k Ω
External timing capacitance, C_{ext}		0		1000	0		1000	μ F
Output duty cycle	$R_T = 2\text{ k}\Omega$			50			50	%
	$R_T = \text{MAX } R_{ext}$			90			90	%
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS221			SN74LS221			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{T+}	Positive-going threshold voltage at A input	V _{CC} = MIN		1.0	2		1.0	2	V	
V _{T-}	Negative-going threshold voltage at A input	V _{CC} = MIN	0.7	1.0		0.8	1.0		V	
V _{T+}	Positive-going threshold voltage at B input	V _{CC} = MIN		1.0	2		1.0	2	V	
V _{T-}	Negative-going threshold voltage at B input	V _{CC} = MIN	0.7	0.9		0.8	0.9		V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN, I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN	I _{OL} = 4 mA			0.25			0.4	V
			I _{OL} = 8 mA			0.35			0.5	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	μA	
I _{IL}	Low-level input current	Input A			-0.4			-0.4	mA	
		Input B			-0.8			-0.8		
		Clear			-0.8			-0.8		
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	-20		-100	-20		-100	mA	
I _{CC}	Supply current	V _{CC} = MAX	Quiescent		4.7	11	4.7		11	mA
			Triggered		19	27	19		27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

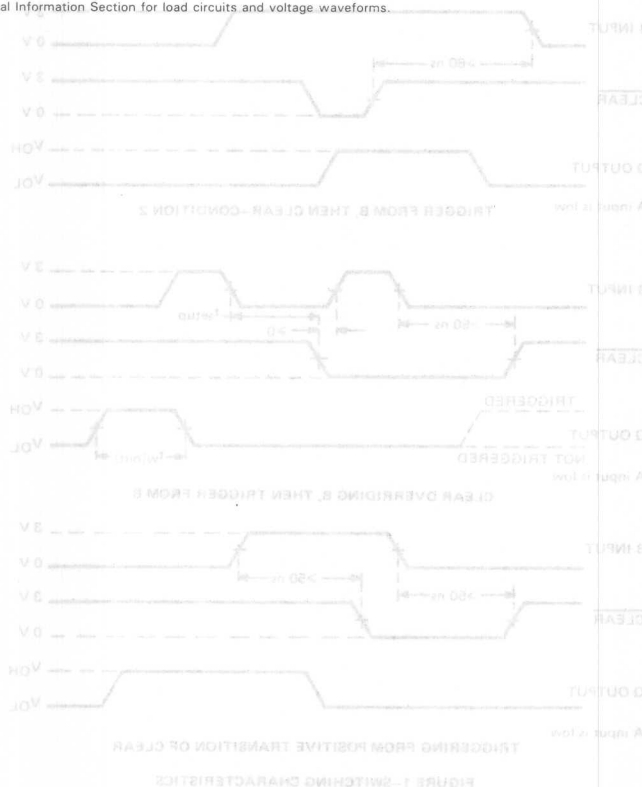
PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figure 1 and Note 3	45	70	ns	
	B	Q					
t_{PHL}	A	\bar{Q}		50	80	ns	
	B	\bar{Q}					
t_{PHL}	Clear	Q		35	55	ns	
t_{PLH}	Clear	\bar{Q}		44	65	ns	
$t_{w(out)}$	A or B	Q or \bar{Q}	$C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$	70	120	150	ns
			$C_{ext} = 0$, $R_{ext} = 2\text{ k}\Omega$	20	47	70	
			$C_{ext} = 100\text{ pF}$, $R_{ext} = 10\text{ k}\Omega$	670	740	810	
			$C_{ext} = 1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$	6	6.9	7.5	ms

[†] t_{PLH} \equiv Propagation delay time, low-to-high-level output

t_{PHL} \equiv Propagation delay time, high-to-low-level output

$t_{w(out)}$ \equiv Output pulse width

NOTE 3: See General Information Section for load circuits and voltage waveforms.



TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

PARAMETER MEASUREMENT INFORMATION

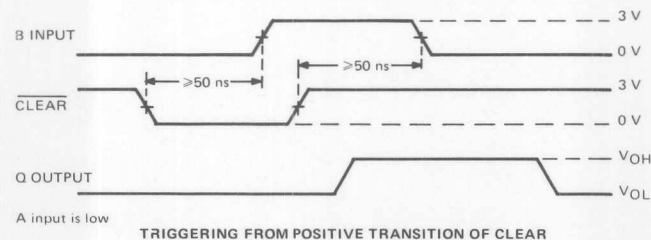
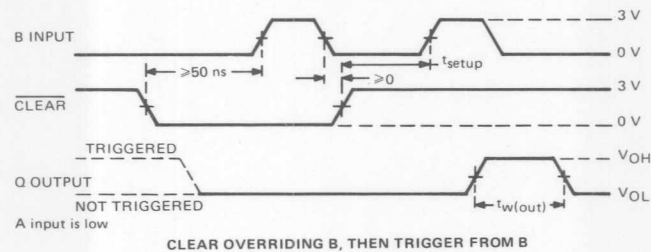
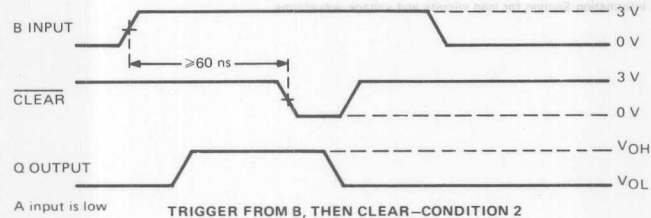
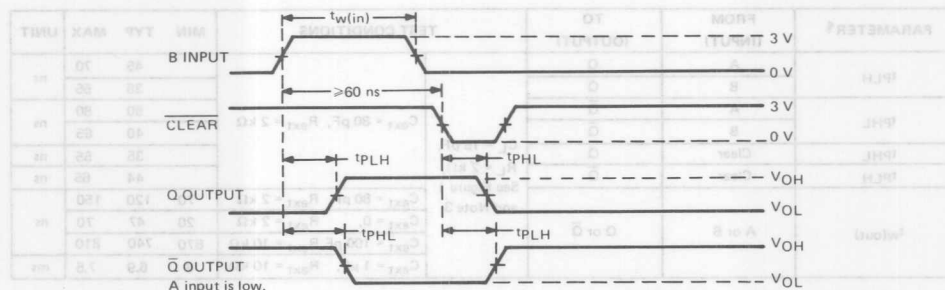


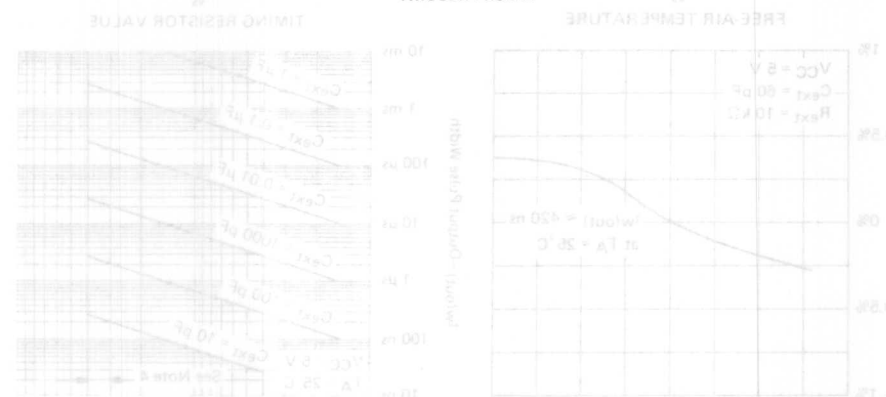
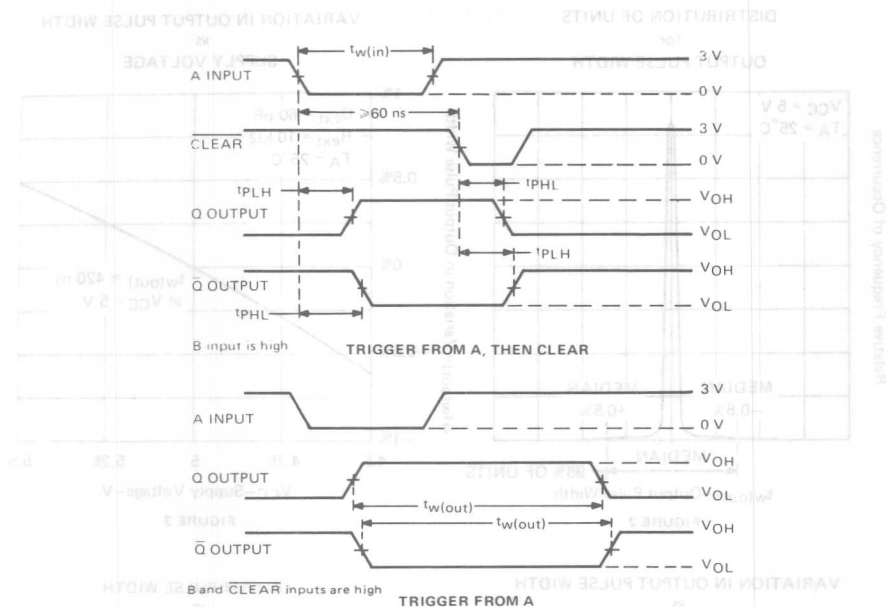
FIGURE 1—SWITCHING CHARACTERISTICS

3

TTL DEVICES

TYPES SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} = 50 \Omega$; for '221, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for 'LS221, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

FIGURE 1—SWITCHING CHARACTERISTICS (CONTINUED)

TYPES SN54221, SN74221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

TYPICAL CHARACTERISTICS ('221 ONLY)†

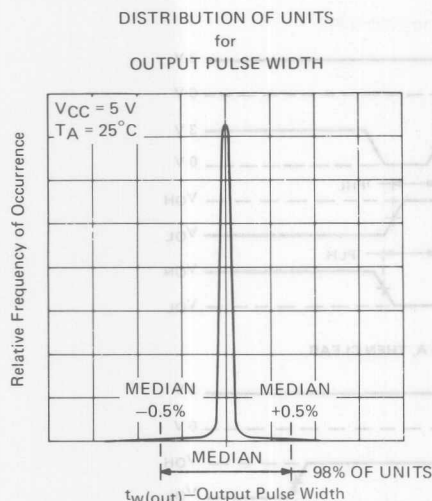


FIGURE 2

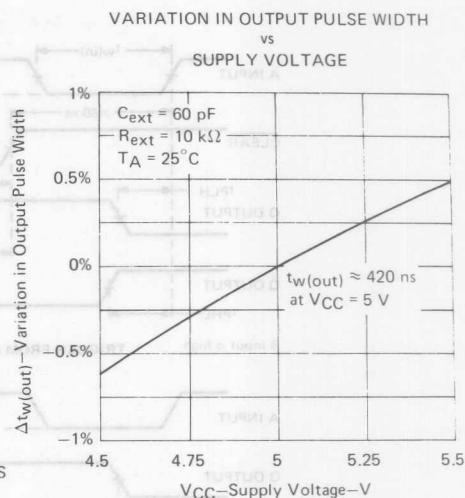


FIGURE 3

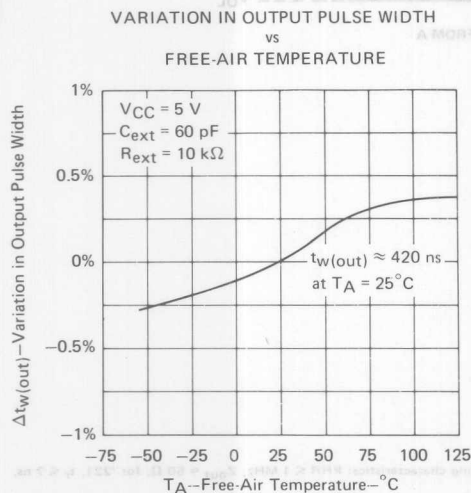


FIGURE 4

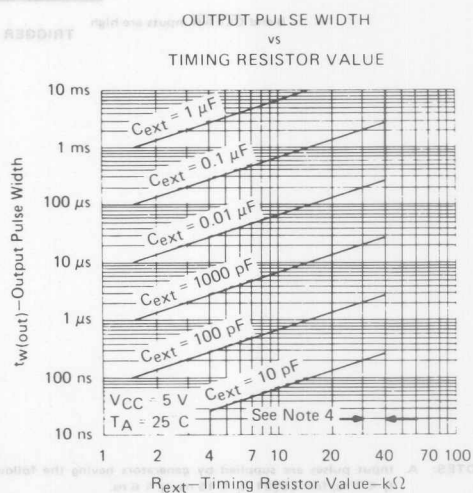


FIGURE 5

NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221

† Data for temperatures below 0°C and above 70°C , and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.

3

TTL DEVICES

TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

REVISED APRIL 1985

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

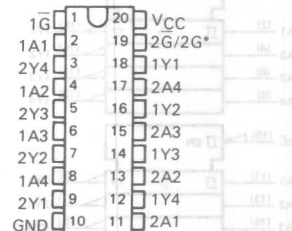
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical \bar{G} (active-low output control) inputs, and complementary G and \bar{G} inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

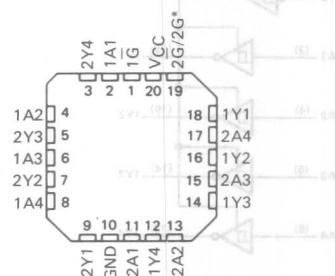
SN54LS', SN54S' ... J PACKAGE
SN74LS', SN74S' ... DW, J OR N PACKAGE

(TOP VIEW)



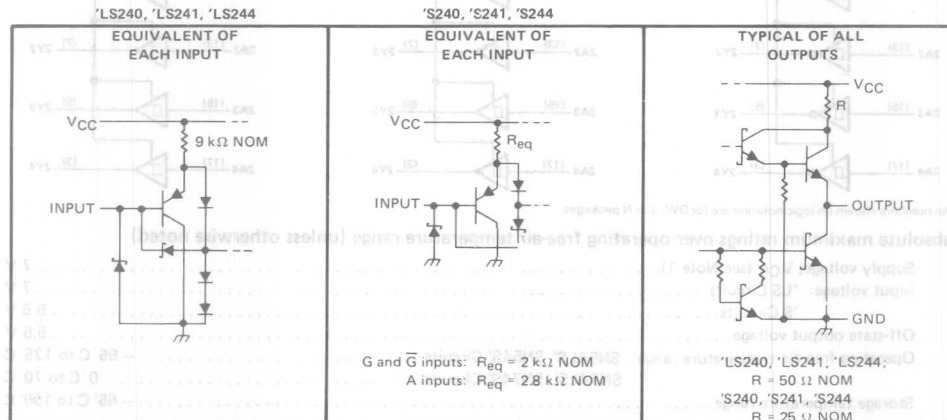
SN54LS', SN54S' ... FK PACKAGE
SN74LS', SN74S'

(TOP VIEW)



*2G for 'LS241 and 'S241 or 2G for all other drivers.

schematics of inputs and outputs



PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

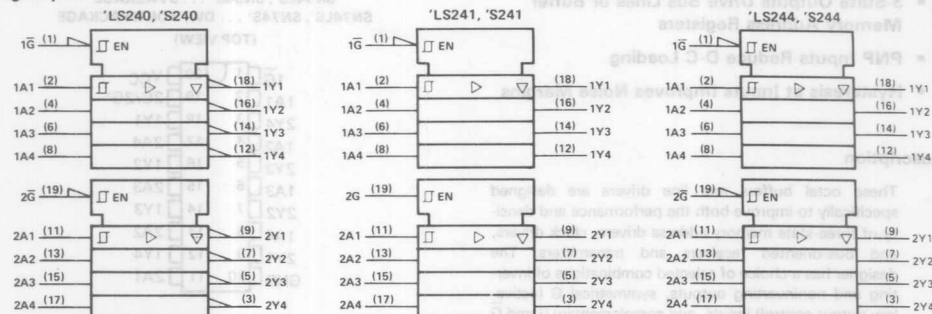
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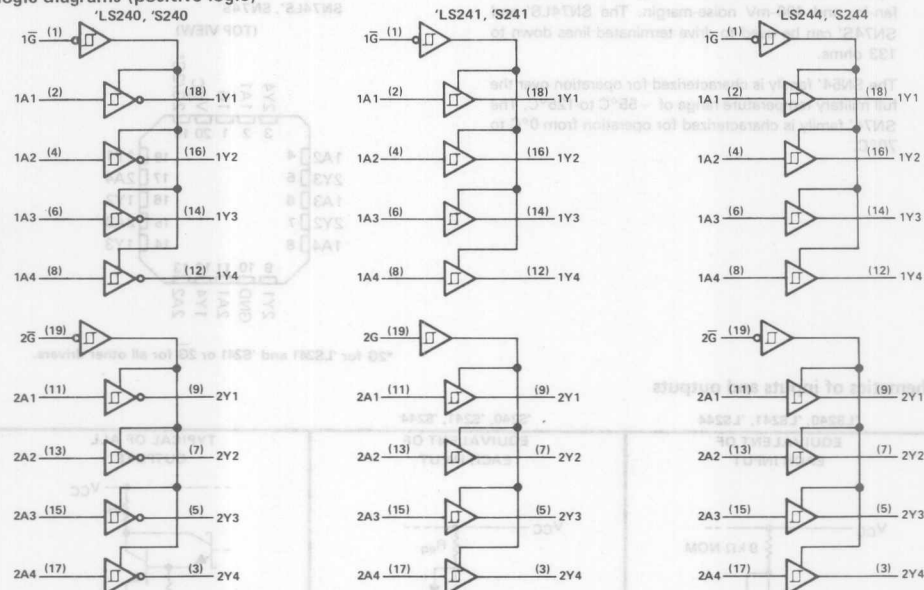
TTL DEVICES

**TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244,
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244**
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbols



logic diagrams (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1).	7 V
Input voltage: 'LS Circuits.	7 V
'S Circuits.	5.5 V
Off-state output voltage.	5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits	-55°C to 125°C
SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54LS240, SN54LS241, SN54LS244, SN74LS240, SN74LS241, SN74LS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54LS [†]			SN74LS [†]			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-12			-15	mA
I _{OL} Low-level output current			12			24	mA
T _A Operating free-air temperature	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		SN54LS [†]			SN74LS [†]			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN		0.2	0.4		0.2	0.4		V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -3 mA		2.4	3.4		2.4	3.4		V
	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.5 V, I _{OH} = MAX		2			2			V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 12 mA				0.4			0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 24 mA							0.5	V
I _{OZH}	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V				20			20	μA
I _{OZL}	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V				-20			-20	μA
I _I	V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V				-0.2			-0.2	mA
I _{OS} [§]	V _{CC} = MAX		-40		-225	-40		-225	mA
I _{CC}	Outputs high	All		17	27		17	27	mA
	Outputs low	'LS240		26	44		26	44	mA
		'LS241, 'LS244		27	46		27	46	mA
	All outputs disabled	'LS240		29	50		29	50	mA
		'LS241, 'LS244		32	54		32	54	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	R _L = 667 Ω, C _L = 45 pF, See Note 2		9	14		12	18		ns
t _{PHL}			12	18		12	18		ns
t _{PZL}			20	30		20	30		ns
t _{PZH}	R _L = 667 Ω, C _L = 5 pF, See Note 2		15	23		15	23		ns
t _{PLZ}			10	20		10	20		ns
t _{PHZ}			15	25		15	25		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3 TTL DEVICES

PARAMETER	SN54S'*			SN74S'*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage, (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-12			-15	mA
I _{OL} Low-level output current			48			64	mA
External resistance between any input and V _{CC} or ground			40			40	k Ω
T _A Operating free-air temperature (see Note 3)	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54S'			SN74S'			UNIT		
					MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IK}		V _{CC} = MIN,	I _I = - 18 mA			- 1.2			- 1.2			V	
Hysteresis (V _{T+} - V _{T-})		V _{CC} = MIN				0.2	0.4		0.2	0.4		V	
V _{OH}		V _{CC} = MIN, I _{OH} = - 1 mA	V _{IH} = 2 V, V _{IL} = 0.8 V,			2.7						V	
		V _{CC} = MIN, I _{OH} = - 3 mA	V _{IH} = 2 V, V _{IL} = 0.8 V,			2.4	3.4		2.4	3.4	V		
		V _{CC} = MIN, I _{OH} = MAX	V _{IH} = 2 V, V _{IL} = 0.5 V,			2			2				
V _{OL}		V _{CC} = MIN, I _{OL} = MAX	V _{IH} = 2 V, V _{IL} = 0.8 V,			0.55			0.55			V	
I _{OZH}		V _{CC} = MAX, V _{IL} = 0.8 V,	V _{IH} = 2 V,	V _O = 2.4 V	50			50			μA		
I _{OZL}		V _{IL} = 0.8 V,		V _O = 0.5 V	- 50			- 50					
I _I		V _{CC} = MAX, V _I = 5.5 V				1			1			mA	
I _{IH}		V _{CC} = MAX, V _I = 2.7 V				50			50			μA	
I _{IL}	Any A	V _{CC} = MAX, V _I = 0.5 V				- 400			- 400			μA	
	Any G					- 2			- 2			mA	
I _{OS} §		V _{CC} = MAX				- 50	- 225		- 50	- 225		mA	
I _{CC}	Outputs high	V _{CC} = MAX,	Outputs open	'S240	80	123		80	135		mA		
				'S241, 'S244	95	147		95	160				
	Outputs low			'S240	100	145		100	150				
				'S241, 'S244	120	170		120	180				
	Outputs disabled			'S240	100	145		100	150				
				'S241, 'S244	120	170		120	180				

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

TYPES SN54S240, SN54S241, SN54S244, SN74S240, SN74S241, SN74S244

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

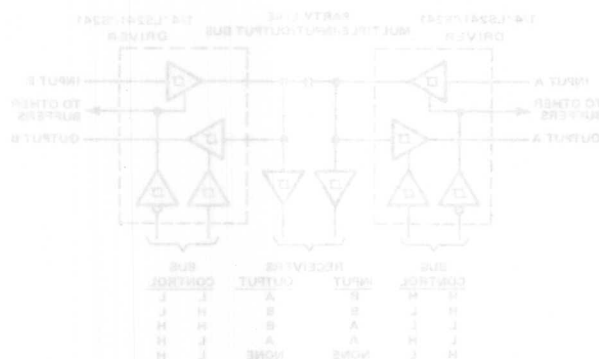
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	'S240			'S241, 'S244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 90\ \Omega$, See Note 4	4.5		7	6		9	ns
t_{PHL}		4.5		7	6		9	ns
t_{PZL}		10		15	10		15	ns
t_{PZH}	$R_L = 90\ \Omega$, See Note 4	6.5		10	8		12	ns
t_{PLZ}		10		15	10		15	ns
t_{PHZ}		6		9	6		9	ns

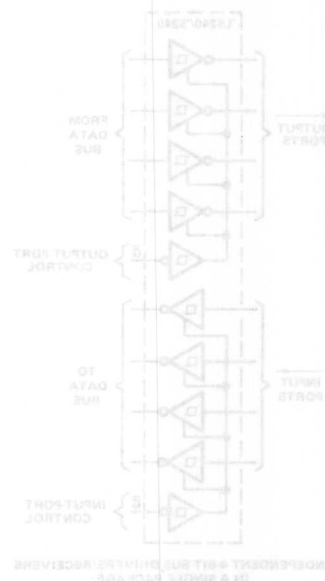
NOTE 4: See General Information Section for load circuits and voltage waveforms.



SYSTEM AND/OR MEMORY ADDRESS BUS
ADDRESS NEEDS SYSTEM AND/OR MEMORY BUS DRIVER—A BIT
ORGANIZATION CAN BE APPLIED TO 8-BIT BINARY OR BCD



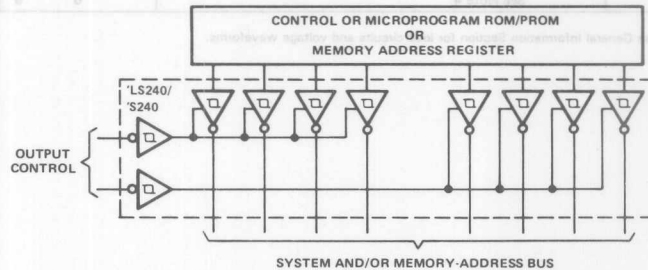
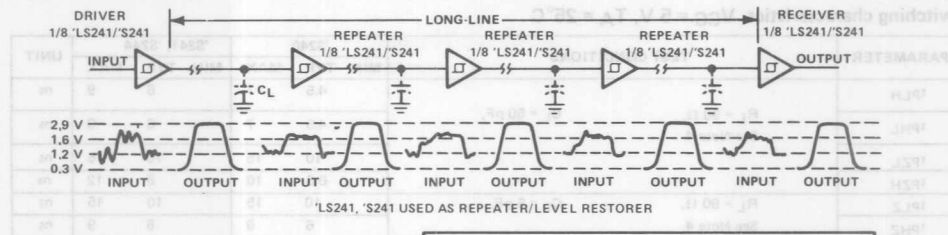
PARITY-TYPE BUS SYSTEM
WITH MULTIPLE INPUTS AND RECEIVERS



3

TTL DEVICES

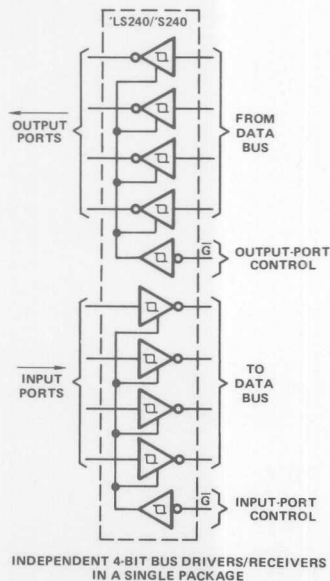
TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



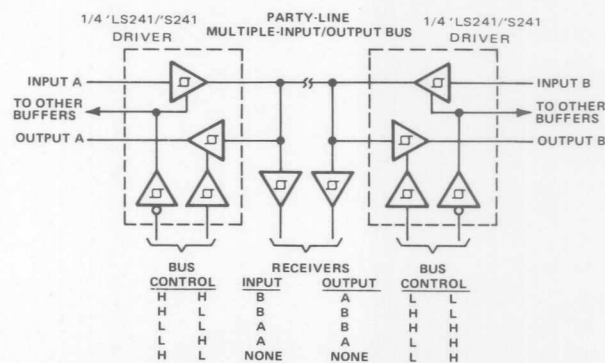
'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD

3

TTL DEVICES



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TYPES SN54LS242, SN54LS243, SN74LS242, SN74LS243 QUADRUPLE BUS TRANSCEIVERS

REVISED APRIL 1985

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

description

These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74LS' can be used to drive terminated lines down to 133 ohms.

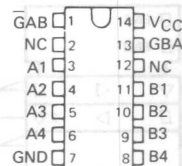
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

FUNCTION TABLE (EACH TRANSCEIVER)

INPUTS		'LS242	'LS243
$\overline{\text{GAB}}$	GBA		
L	L	$\overline{\text{A}}$ to B	A to B
H	H	$\overline{\text{B}}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($\text{A} = \overline{\text{B}}$)	Latch A and B ($\text{A} = \text{B}$)

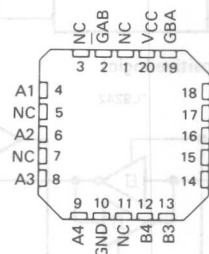
SN54LS242, SN54LS243 ... J OR W PACKAGE
SN74LS242, SN74LS243 ... D, J OR N PACKAGE

(TOP VIEW)



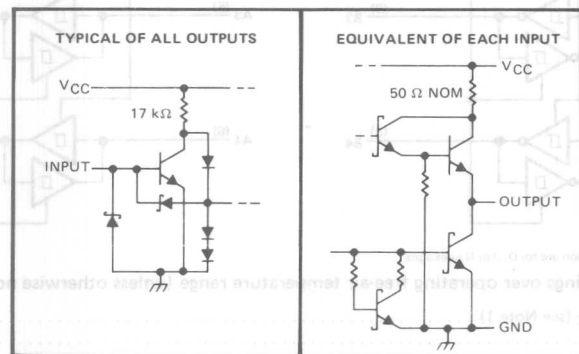
SN54LS242, SN54LS243 ... FK PACKAGE
SN74LS242, SN74LS243

(TOP VIEW)



NC-No internal connection

schematics of inputs and outputs



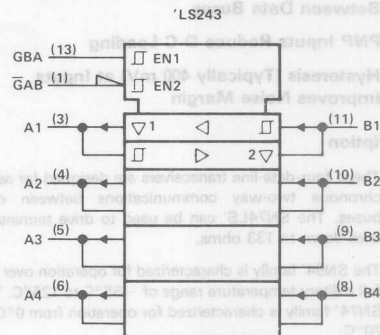
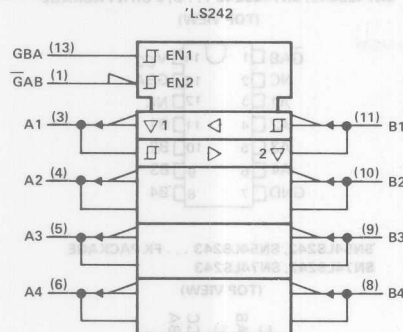
PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

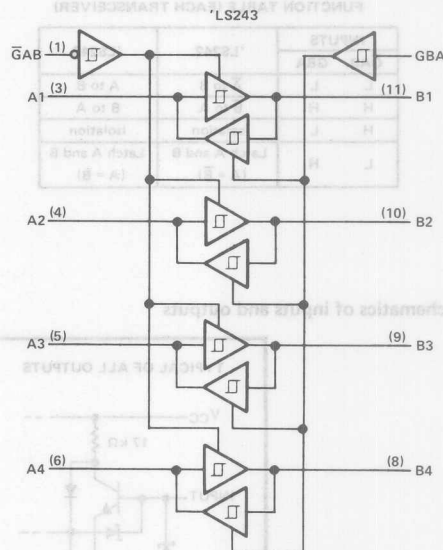
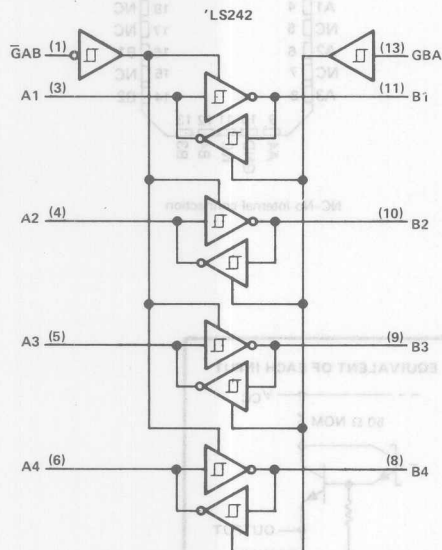
3-695

TYPES SN54LS242, SN54LS243, SN74LS242, SN74LS243 QUADRUPLE BUS TRANSCEIVERS

logic symbols



logic diagrams (positive logic)



Pin numbers shown on logic notation are for D, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS242, SN54LS243, SN74LS242, SN74LS243 QUADRUPLE BUS TRANSCEIVERS

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage, (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	A or B	V _{CC} = MIN, I _I = − 18 mA				− 1.5			− 1.5	V
Hysteresis (V _{T+} − V _{T−})		V _{CC} = MIN		0.2	0.4		0.2	0.4		V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = − 3 mA		2.4	3.1		2.4	3.1		V
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.5 V, I _{OH} = MAX		2			2			V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I _{OL} = 24 mA					0.35	0.5	V
I _{OZH}		V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX	V _O = 2.7 V			40			40	μA
I _{OZL}			V _O = 0.4 V			− 200			− 200	μA
I _I	A or B	V _{CC} = MAX,	V _I = 5.5 V			0.1			0.1	mA
	GAB or GBA		V _I = 7 V			0.1		0.1	mA	
I _{IH}		V _{CC} = MAX, V _I = 2.7 V				20			20	μA
I _{IL}	A inputs	V _{CC} = MAX, V _I = 0.4 V, GAB and GBA at 0 V				− 0.2			− 0.2	mA
	B inputs	V _{CC} = MAX, V _I = 0.4 V, GAB and GBA at 4.5 V				− 0.2			− 0.2	mA
	GAB or GBA	V _{CC} = MAX, V _I = 0.4 V				− 0.2			− 0.2	mA
I _{OS} §		V _{CC} = MAX		− 40		− 225	− 40		− 225	mA
I _{CC}	Outputs high	V _{CC} = MAX, Outputs open, See Note 2	'LS242, 'LS243		22	38		22	38	mA
	Outputs low		'LS242, 'LS243		29	50		29	50	
	All outputs disabled		'LS242		29	50		29	50	
			'LS243		32	54		32	54	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	'LS242			'LS243			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 667 \Omega$ See Note 3		9	14		12	18	ns
t_{PHL}			12	18		12	18	ns
t_{PZL}			20	30		20	30	ns
t_{PZH}	$R_L = 667 \Omega,$ See Note 3		15	23		15	23	ns
t_{PLZ}			10	20		10	20	ns
t_{PHZ}			15	25		15	25	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage	0.7			V
I_{OH}	High-level output current	-13			mA
I_{OL}	Low-level output current	13			mA
T_A	Operating free-air temperature	-55	125	0	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	A or B				V
Propagation delay (t_{PLH} , t_{PLL})	$V_{CC} = \text{MIN}$, $V_I = -1.5 \text{ V}$	0.3	0.4	0.5	nS
V_{OH}	$V_{CC} = \text{MIN}$, $V_I = -1.5 \text{ V}$, $I_{OH} = -13 \text{ mA}$	2.4	2.1	2.4	V
V_{OL}	$V_{CC} = \text{MAX}$, $V_I = 1.5 \text{ V}$, $I_{OL} = 13 \text{ mA}$	0.3	0.4	0.5	V
t_{RST}	$V_{CC} = \text{MAX}$, $V_I = 1.5 \text{ V}$, $I_{OL} = 13 \text{ mA}$	0.3	0.4	0.5	nS
t_{FST}	$V_{CC} = \text{MAX}$, $V_I = 1.5 \text{ V}$, $I_{OL} = 13 \text{ mA}$	0.3	0.4	0.5	nS
I_{CC1}	A or B				mA
I_{CC2}	A or B				mA
I_{CC3}	A or B				mA
I_{CC4}	A or B				mA
I_{CC5}	A or B				mA
I_{CC6}	A or B				mA
I_{CC7}	A or B				mA
I_{CC8}	A or B				mA
I_{CC9}	A or B				mA
I_{CC10}	A or B				mA
I_{CC11}	A or B				mA
I_{CC12}	A or B				mA
I_{CC13}	A or B				mA
I_{CC14}	A or B				mA
I_{CC15}	A or B				mA
I_{CC16}	A or B				mA
I_{CC17}	A or B				mA
I_{CC18}	A or B				mA
I_{CC19}	A or B				mA
I_{CC20}	A or B				mA
I_{CC21}	A or B				mA
I_{CC22}	A or B				mA
I_{CC23}	A or B				mA
I_{CC24}	A or B				mA
I_{CC25}	A or B				mA
I_{CC26}	A or B				mA
I_{CC27}	A or B				mA
I_{CC28}	A or B				mA
I_{CC29}	A or B				mA
I_{CC30}	A or B				mA
I_{CC31}	A or B				mA
I_{CC32}	A or B				mA
I_{CC33}	A or B				mA
I_{CC34}	A or B				mA
I_{CC35}	A or B				mA
I_{CC36}	A or B				mA
I_{CC37}	A or B				mA
I_{CC38}	A or B				mA
I_{CC39}	A or B				mA
I_{CC40}	A or B				mA
I_{CC41}	A or B				mA
I_{CC42}	A or B				mA
I_{CC43}	A or B				mA
I_{CC44}	A or B				mA
I_{CC45}	A or B				mA
I_{CC46}	A or B				mA
I_{CC47}	A or B				mA
I_{CC48}	A or B				mA
I_{CC49}	A or B				mA
I_{CC50}	A or B				mA
I_{CC51}	A or B				mA
I_{CC52}	A or B				mA
I_{CC53}	A or B				mA
I_{CC54}	A or B				mA
I_{CC55}	A or B				mA
I_{CC56}	A or B				mA
I_{CC57}	A or B				mA
I_{CC58}	A or B				mA
I_{CC59}	A or B				mA
I_{CC60}	A or B				mA
I_{CC61}	A or B				mA
I_{CC62}	A or B				mA
I_{CC63}	A or B				mA
I_{CC64}	A or B				mA
I_{CC65}	A or B				mA
I_{CC66}	A or B				mA
I_{CC67}	A or B				mA
I_{CC68}	A or B				mA
I_{CC69}	A or B				mA
I_{CC70}	A or B				mA
I_{CC71}	A or B				mA
I_{CC72}	A or B				mA
I_{CC73}	A or B				mA
I_{CC74}	A or B				mA
I_{CC75}	A or B				mA
I_{CC76}	A or B				mA
I_{CC77}	A or B				mA
I_{CC78}	A or B				mA
I_{CC79}	A or B				mA
I_{CC80}	A or B				mA
I_{CC81}	A or B				mA
I_{CC82}	A or B				mA
I_{CC83}	A or B				mA
I_{CC84}	A or B				mA
I_{CC85}	A or B				mA
I_{CC86}	A or B				mA
I_{CC87}	A or B				mA
I_{CC88}	A or B				mA
I_{CC89}	A or B				mA
I_{CC90}	A or B				mA
I_{CC91}	A or B				mA
I_{CC92}	A or B				mA
I_{CC93}	A or B				mA
I_{CC94}	A or B				mA
I_{CC95}	A or B				mA
I_{CC96}	A or B				mA
I_{CC97}	A or B				mA
I_{CC98}	A or B				mA
I_{CC99}	A or B				mA
I_{CC100}	A or B				mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
3. Not more than one output should be asserted at a time, and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with transceivers enabled in one direction only, in which transceivers drawing.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FHL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF}$	12	14	16	nS
t_{FSL}	$R_L = 80 \Omega$ $C_L = 40 \text{ pF$				

TYPES SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTOBER 1976—REVISED APRIL 1985

- Bi-directional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times, Port-to-Port . . . 8 ns

TYPE	I _{OL} (SINK CURRENT)	I _{OH} (SOURCE CURRENT)
SN54LS245	12 mA	-12 mA
SN74LS245	24 mA	-15 mA

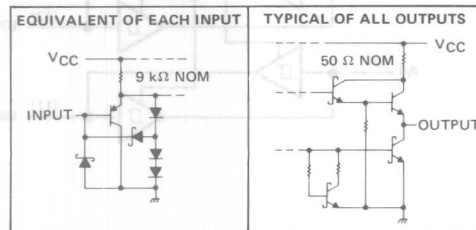
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

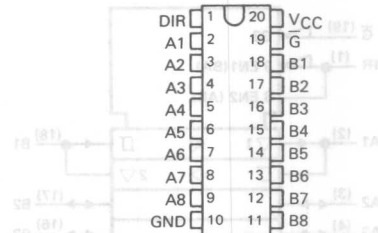
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

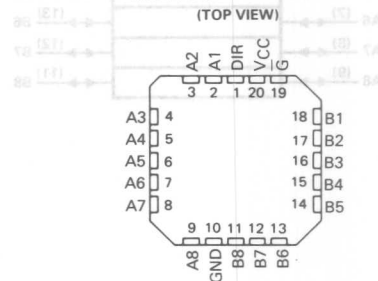
schematics of inputs and outputs



SN54LS245 . . . J PACKAGE
SN74LS245 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS245 . . . FK PACKAGE
SN74LS245
(TOP VIEW)



FUNCTION TABLE

ENABLE \bar{G}	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

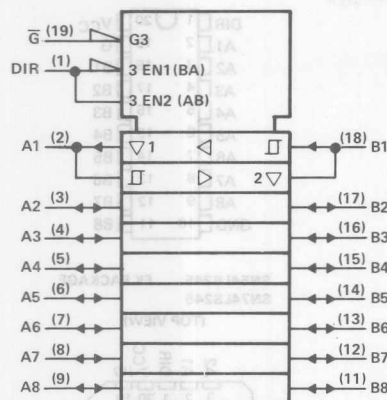
H = high level, L = low level, X = irrelevant

PRODUCTION DATA

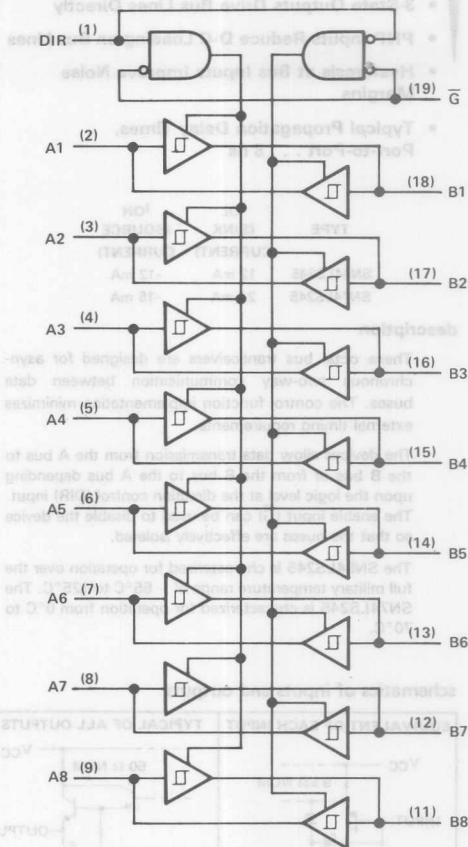
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TYPES SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol



logic diagram (positive logic)



3

TTL DEVICES

ENABLE	DIRECTION	OPERATION
H	DIR	B data to A bus
L	DIR	A data to B bus
X	DIR	Isolation

Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54LS245			SN74LS245			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS245			SN74LS245			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage			0.7			0.8			V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V
Hysteresis (V _{T+} - V _{T-}) A or B input			V _{CC} = MIN	0.2	0.4		0.2	0.4		V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OH} = -3 mA	2.4	3.4		2.4	3.4	V
			I _{OH} = MAX	2		2				
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OL} = 12 mA	0.4			0.4		V
			I _{OL} = 24 mA				0.5			
I _{OZH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, \bar{G} at 2 V	V _O = 2.7 V	20			20		µA
I _{OZL}	Off-state output current, low-level voltage applied			V _O = 0.4 V	-200			-200		
I _I	Input current at maximum input voltage	A or B DIR or \bar{G}	V _{CC} = MAX,	V _I = 5.5 V	0.1			0.1		mA
		V _I = 7 V		0.1			0.1			
I _{IH}	High-level input current		V _{CC} = MAX, V _{IH} = 2.7 V	20				20		µA
I _{IL}	Low-level input current		V _{CC} = MAX, V _{IL} = 0.4 V	-0.2				-0.2		mA
I _{OS}	Short-circuit output current¶		V _{CC} = MAX	-40		-225	-40	-225		mA
I _{CC}	Supply current	Total, outputs high	V _{CC} = MAX, Outputs open	48		70	48	70		mA
		62		90	62	90				
		64		95	64	95				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

¶ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$C_L = 45 \text{ pF}, R_L = 667 \Omega, \text{ See Note 2}$	8	12	ns
t_{PZL}	Output enable time to low level		27	40	ns
t_{PZH}	Output enable time to high level		25	40	ns
t_{PLZ}	Output disable time from low level	$C_L = 5 \text{ pF}, R_L = 667 \Omega, \text{ See Note 2}$	15	25	ns
t_{PHZ}	Output disable time from high level		15	28	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

OCAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS TYPICAL CHARACTERISTICS

recommended operating conditions

PARAMETER	SN7ALS245	
	MIN	MAX
Supply voltage, V_{CC}	4.5	5.5
High-level output current, I_{OH}	-15	-15
Low-level output current, I_{OL}	15	15
Operating free-air temperature, T_A	-55	125

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		UNIT
	MIN	MAX	
V_{IH} High-level input voltage	2	2	V
V_{IL} Low-level input voltage	0.7	0.7	V
V_{IK} Input clamp voltage	-1.8	-1.8	V
Hysteresis ($V_{TH} - V_{TL}$) at 8 mV	0.2	0.4	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$	2.4	V
	$I_{OH} = -3 \text{ mA}$	2.4	
	$V_{IH} = 2 \text{ V}$	2.4	
	$V_{IL} = 0.7 \text{ V}$	2.4	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$	0.4	V
	$I_{OL} = 3 \text{ mA}$	0.4	
	$V_{IH} = 2 \text{ V}$	0.4	
	$V_{IL} = 0.7 \text{ V}$	0.4	
I_{OZH} On-state output current high-level voltage applied	$V_{CC} = \text{MAX}$	30	mA
	$V_O = 2.5 \text{ V}$	30	
I_{OLZ} On-state output current low-level voltage applied	$V_{CC} = \text{MAX}$	-300	mA
	$V_O = 0.4 \text{ V}$	-300	
I_I Input current at 0 or 1	$V_{CC} = \text{MAX}$	0.1	mA
	$V_I = 2.5 \text{ V}$	0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$	30	mA
	$V_{IH} = 2.5 \text{ V}$	30	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$	-30	mA
	$V_{IL} = 0.4 \text{ V}$	-30	
I_{OS} Short-circuit output current	$V_{CC} = \text{MAX}$	-40	mA
	$V_O = 0.4 \text{ V}$	-40	
I_{CC} Supply current	Total, on high	45	mA
	Total, on low	80	
	Output open	80	

For conditions shown as MIN or MAX, use the appropriate value specified unless recommended operating conditions are noted.
All values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
Test time may vary; output should be tested at a time, and duration of the above circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		UNIT
	MIN	MAX	
t_{PLH} Propagation delay time low-to-high level output	8	15	ns
t_{PLZ} Propagation delay time high-to-low level output	8	15	ns
t_{PZL} Propagation delay time low-to-low level output	30	40	ns
t_{PZH} Propagation delay time high-to-high level output	30	40	ns
t_{PZS} Output disable time from low level	15	30	ns
t_{PHS} Output disable time from high level	15	30	ns

NOTE 1: See General Information Section for load circuit and timing waveform.

3 TTL DEVICES

TYPES SN54247, SN54LS247 THRU SN54LS249 SN74247, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

MARCH 1974—REVISED DECEMBER 1983

'247, 'LS247 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'LS248 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'LS249 feature

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54247	low	open-collector	40 mA	15 V	320 mW	J, W
SN54LS247	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS248	high	2-k Ω pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS249	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN74247	low	open-collector	40 mA	15 V	320 mW	J, N
SN74LS247	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS248	high	2-k Ω pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS249	high	open-collector	8 mA	5.5 V	40 mW	J, N

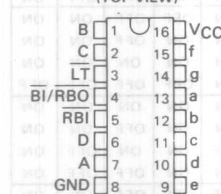
SN54247

SN54LS247 THRU SN54LS249 ... J OR W PACKAGE

SN74247 ... J OR N PACKAGE

SN74LS247 THRU SN74LS249 ... D, J OR N PACKAGE

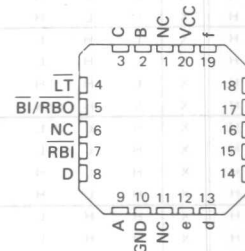
(TOP VIEW)



SN54LS247 THRU SN54LS249 ... FK PACKAGE



SN74LS247 THRU SN74LS249

(TOP VIEW)



NC - No internal connection

description

The '247 is electrically and functionally identical to the SN5447A/SN7447A, and has the same pin assignment. Also the 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The 'LS249 is the 16-pin versions of the 14-pin SN54LS49/SN74LS49. Included in the 'LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the 'LS49 circuits. The '46A, '47A, '48, '49, 'LS47, 'LS48, and 'LS49 compose the  and the  without tails and the '247, 'LS247, 'LS248, and 'LS249

PRODUCTION DATA

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TEXAS
INSTRUMENTS

3-703

3

TTL DEVICES

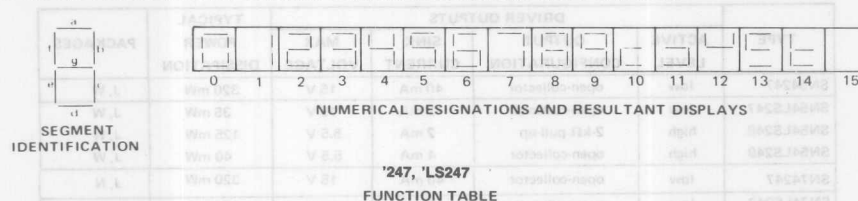
TYPES SN54247, SN54LS247 THRU SN54LS249, SN74247, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

description (continued)

compose the 5 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the 'LS248, and 'LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{\text{RBI}}$ and $\overline{\text{RBO}}$). Lamp test ($\overline{\text{LT}}$) of these types may be performed at any time when the $\overline{\text{BI/RBO}}$ node is at a high level. All types contain an overriding blanking input ($\overline{\text{BI}}$) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C .



DECIMAL OR FUNCTION	INPUTS						$\overline{\text{BI/RBO}}^{\dagger}$	OUTPUTS							NOTE
	LT	$\overline{\text{RBI}}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
$\overline{\text{LT}}$	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a low level (response condition).

4. When the blanking input/ripple blanking output ($\overline{\text{BI/RBO}}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

$^{\dagger}\overline{\text{BI/RBO}}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$).

3

TTL DEVICES

**TYPES SN54248, SN54LS249
SN74LS248, SN74LS249
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

**'LS248, 'LS249
FUNCTION TABLE**

DECIMAL OR FUNCTION	INPUTS						BI/RBO [†]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	1
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	2
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	3
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	4
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

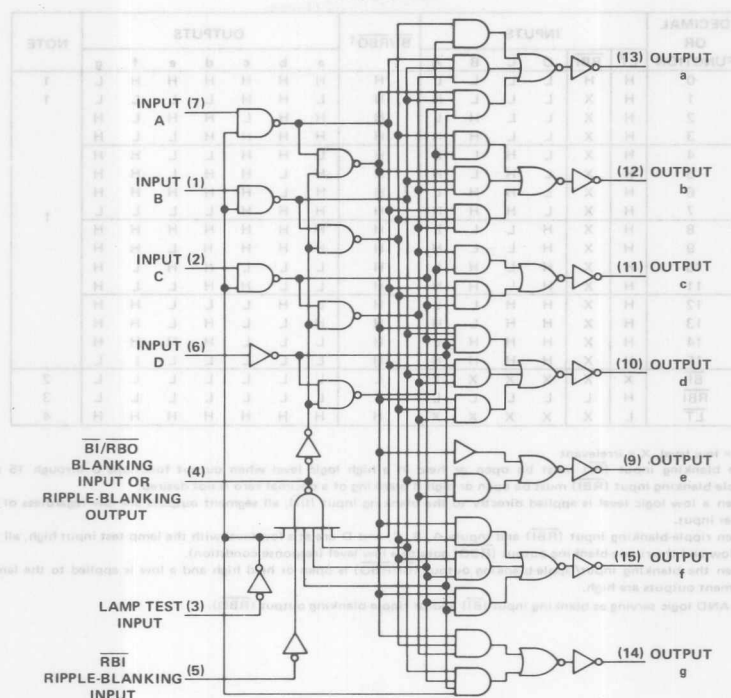
[†] BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

3

TTL DEVICES

**TYPES SN54247, SN54LS247
SN74247, SN74LS247
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

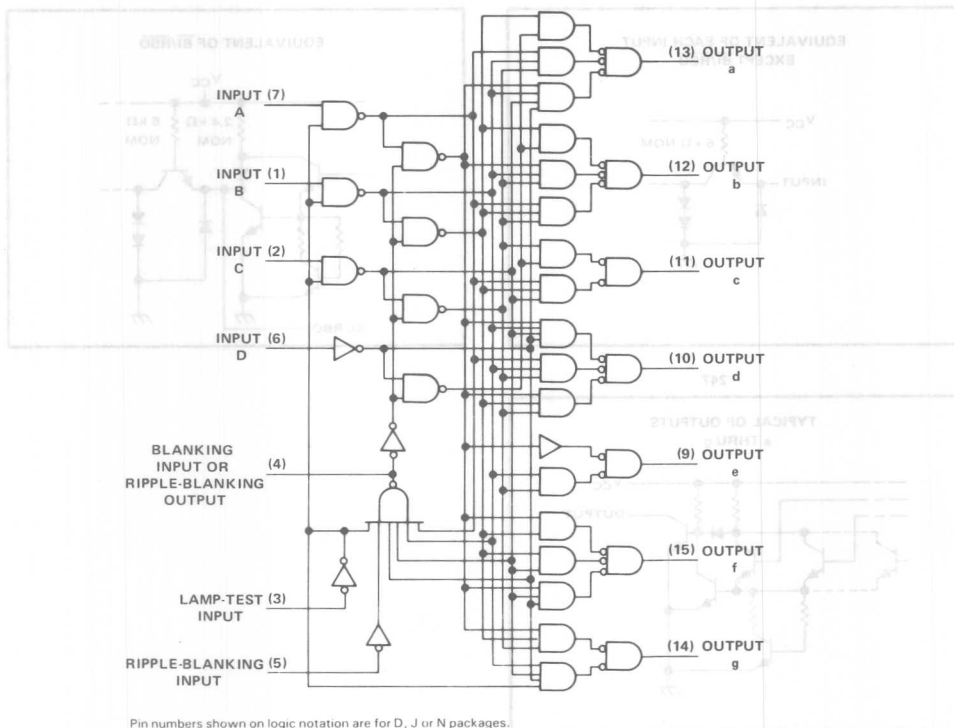
3

TTL DEVICES

**TYPES SN54LS248, SN54LS249
SN74LS248, SN74LS249
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

logic diagrams

'LS248, 'LS249



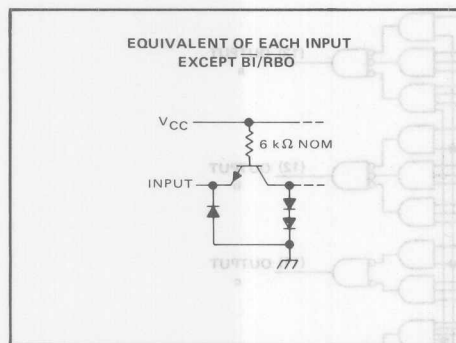
3

TTL DEVICES

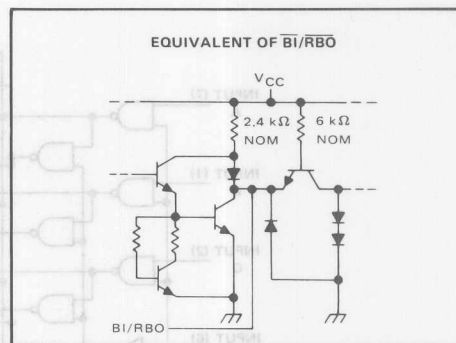
TYPES SN54247, SN74247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

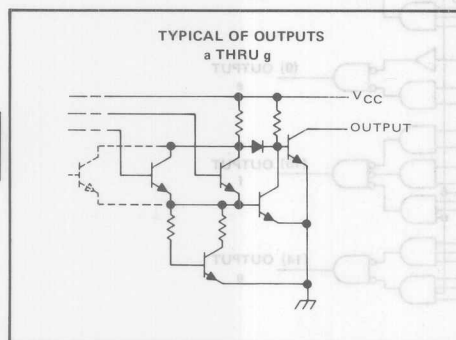
'247



'247



'247



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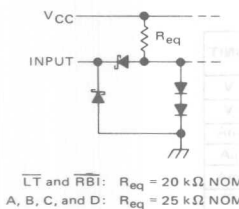
TTL DEVICES

TYPES SN54LS247 THRU SN54LS249, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

schematics of inputs and outputs

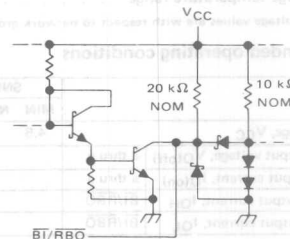
'LS247, 'LS248, 'LS249

EQUIVALENT OF EACH INPUT
EXCEPT BI/RBO



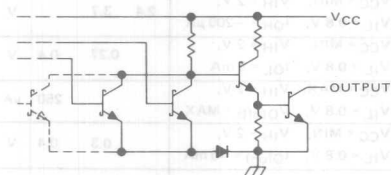
'LS247, 'LS248, 'LS249

EQUIVALENT OF BI/RBO



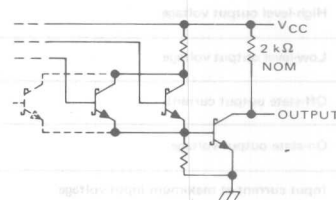
'LS247

TYPICAL OF OUTPUTS
a THRU g



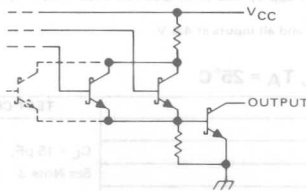
'LS248

TYPICAL OF OUTPUTS
a THRU g



'LS249

TYPICAL OF OUTPUTS
a THRU g



3

TTL DEVICES

TYPES SN54247, SN74247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54247	-55°C to 125°C
SN74247	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54247			SN74247			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$ a thru g			15			15	V
On-state output current, $I_{O(on)}$ a thru g			40			40	mA
High-level output current, I_{OH} BI/RBO			-200			-200	μ A
Low-level output current, I_{OL} BI/RBO			8			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				1.5	V
V_{OH}	High-level output voltage	BI/RBO $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -200 \mu\text{A}$	2.4	3.7			V
V_{OL}	Low-level output voltage	BI/RBO $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 8 \text{ mA}$	0.27	0.4			V
$I_{O(off)}$	Off-state output current	a thru g $V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $V_{O(off)} = \text{MAX}$				250	μ A
$V_{O(on)}$	On-state output voltage	a thru g $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{O(on)} = 40 \text{ mA}$	0.3	0.4			V
I_I	Input current at maximum input voltage	Any input except BI/RBO $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Any input except BI/RBO $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$				40	μ A
I_{IL}	Low-level input current	Any input except BI/RBO $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$				-1.6	mA
I_{OS}	Short-circuit output current	BI/RBO $V_{CC} = \text{MAX}$				-4	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 2	64	103			mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input					100	ns
t_{on}	Turn-on time from A input	$C_L = 15 \text{ pF}$, $R_L = 120 \Omega$, See Note 3				100	ns
t_{off}	Turn-off time from RBI input					100	ns
t_{on}	Turn-on time from RBI input					100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS247, SN74LS247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_W \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS247	-55°C to 125°C
SN74LS247	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS247			SN74LS247			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			15			15	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	$\overline{BI}/R\overline{BO}$			-50			-50	μA
Low-level output current, I_{OL}	$\overline{BI}/R\overline{BO}$			1.6			3.2	mA
Operating free-air temperature, T_A		-55		125	0		70	$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS247		SN74LS247		UNIT		
				MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IH}	High-level input voltage			2			2	V		
V _{IL}	Low-level input voltage					0.7		0.8 V		
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5 V		
V _{OH}	High-level output voltage	$\overline{BI}/R\overline{BO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -50 μA	2.4	4.2		2.4	4.2	V	
V _{OL}	Low-level output voltage	$\overline{BI}/R\overline{BO}$	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 1.6 mA		0.25	0.4	0.25	0.4	V
				I _{OL} = 3.2 mA				0.35	0.5	
I _{O(off)}	Off-state output current	a thru g	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _{O(off)} = 15 V			250		250	μA	
V _{O(on)}	On-state output voltage	a thru g	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{O(on)} = 12 mA		0.25	0.4	0.25	0.4	V
				I _{O(on)} = 24 mA				0.35	0.5	
I _I ⁴	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA	
I _{IH} ⁴	High-level input current		V _{CC} = MAX, V _I = 2.7 V			20		20	μA	
I _{IL}	Low-level input current	Any input except $\overline{BI}/R\overline{BO}$	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA	
		$\overline{BI}/R\overline{BO}$				-1.2		-1.2		
I _{OS}	Short-circuit output current	$\overline{BI}/R\overline{BO}$	V _{CC} = MAX	-0.3		-2	-0.3		-2 mA	
I _{CC}	Supply current		V _{CC} = MAX, See Note 2	7		13	7		13 mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input			100	ns
t_{on}	Turn-on time from A input	$C_L = 15 \text{ pF}, R_L = 665 \Omega,$		100	ns
t_{off}	Turn-off time from \overline{RBI} input	See Note 3		100	ns
t_{on}	Turn-on time from \overline{RBI} input			100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

NOTE 4: Any input except $\overline{BI}/R\overline{BO}$

TYPES SN54LS248, SN74LS248 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS248	-55°C to 125°C
SN74LS248	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS248			SN74LS248			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			-100			-100	μ A
	\overline{BI}/RBO			-50			-50	
Low-level output current, I_{OL}	a thru g			2			6	mA
	\overline{BI}/RBO			1.6			3.2	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS248			SN74LS248			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage				0.7			0.8		V
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH}	High-level output voltage	a thru g and \overline{BI}/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.4	4.2		2.4	4.2		V
I_O	Output current	a thru g	$V_{CC} = \text{MIN}, V_O = 0.85 \text{ V},$ Input conditions as for V_{OH}	-1.3	-2		-1.3	-2		mA
V_{OL}	Low-level output voltage	a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	0.25	0.4		0.25	0.4		V
			$I_{OL} = 2 \text{ mA}$							
	\overline{BI}/RBO		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	0.25	0.4		0.25	0.4		V
			$I_{OL} = 3.2 \text{ mA}$							
I_I	Input current at maximum input voltage	Any input except \overline{BI}/RBO	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH}	High-level input current	Any input except \overline{BI}/RBO	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μ A
I_{IL}	Low-level input current	Any input except \overline{BI}/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
		\overline{BI}/RBO			-1.2			-1.2		
I_{OS}	Short-circuit output current	\overline{BI}/RBO	$V_{CC} = \text{MAX}$	-0.3	-2		-0.3	-2		mA
I_{CC}	Supply current		$V_{CC} = \text{MAX},$ See Note 2	25	38		25	38		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS			UNIT
tPHL	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 4 \text{ k}\Omega,$			
		See Note 3			100 ns
tPLH	Propagation delay time, low-to-high-level output from A input				100
tPHL	Propagation delay time, high-to-low-level output from \overline{RBI} input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega,$			100 ns
		See Note 3			

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS249, SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the offstate	1 mA
Operating free-air temperature range: SN54LS249	-55°C to 125°C
SN74LS249	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS249			SN74LS249			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	a thru g			5.5			5.5	V
High-level output current, I_{OH}	$\overline{BI}/\overline{RBO}$			-50			-50	μ A
Low-level output current, I_{OL}	a thru g			4			8	mA
	$\overline{BI}/\overline{RBO}$			1.6			3.2	
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS249			SN74LS249			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -50 \mu\text{A}$	2.4	4.2		2.4	4.2		V
I_{OH}	High-level output current	a thru g $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			250			250	μ A
V_{OL}	Low-level output voltage	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 1.6 \text{ mA}$		0.25	0.4		0.25	0.4	V
							0.35	0.5	
		a thru g $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
							0.35	0.5	
I_I	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	High-level input current	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL}	Low-level input current	Any input except $\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
		$\overline{BI}/\overline{RBO}$			-1.2			-1.2	
I_{OS}	Short-circuit output current	$\overline{BI}/\overline{RBO}$ $V_{CC} = \text{MAX}$	-0.3		-2	-0.3		-2	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	8	15		8	15		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input	See Note 3				100	
t_{PHL}	Propagation delay time, high-to-low-level output from \overline{RBI} input	$C_L = 15 \text{ pF}, R_L = 6 \text{ k}\Omega,$				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from \overline{RBI} input	See Note 3				100	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

BCD-TO-SEVEN-SEGMENT DECODER/DRIVERS

TYPES SN74LS249, SN74ALS249

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the offstate	1 mA
Operating free-air temperature range: SN74LS249	-55°C to 125°C
Operating free-air temperature range: SN74ALS249	-55°C to 150°C
Storage temperature range	-65°C to 180°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN74LS249		SN74ALS249		UNIT
		MIN	TYP	MIN	MAX	
Operating free-air temperature, T_A		-55		-55	125	°C
Low-level output current, I_{OL}	0.3 mA	1.6		1.6	3.2	mA
High-level output current, I_{OH}	0.3 mA	1.6		1.6	3.2	mA
High-level output voltage, V_{OH}	0.3 mA	2.8		2.8	2.8	V
Low-level output voltage, V_{OL}	0.3 mA	0.4		0.4	0.4	V
Supply voltage, V_{CC}		4.5	5	4.5	5	V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74LS249		SN74ALS249		UNIT
		MIN	TYP	MIN	MAX	
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}		0.7		0.7		V
Input clamp voltage, V_{IK}		-1.5		-1.5		V
High-level output voltage, V_{OH}	0.3 mA, $V_{CC} = 5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.7$ V, max, $I_{OH} = -0.3$ mA, $V_{CC} = 5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.7$ V, max, $V_{OH} = 2.8$ V	2.8	4.2	2.8	4.2	V
High-level output current, I_{OH}	0.3 mA, $V_{CC} = 5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.7$ V, max, $V_{OH} = 2.8$ V	1.6		1.6		mA
Low-level output voltage, V_{OL}	0.3 mA, $V_{CC} = 5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.7$ V, max, $V_{OL} = 0.4$ V	0.4	0.52	0.4	0.52	V
Low-level output current, I_{OL}	0.3 mA, $V_{CC} = 5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.7$ V, max, $V_{OL} = 0.4$ V	1.6		1.6		mA
Input current at maximum input voltage, except B1A80	$V_{CC} = 5$ V, $V_I = 2$ V	0.1		0.1		mA
Input current at high-level input voltage, except B1A80	$V_{CC} = 5$ V, $V_I = 2$ V	0.1		0.1		mA
Input current at low-level input voltage, except B1A80	$V_{CC} = 5$ V, $V_I = 0.7$ V	0.1		0.1		mA
Short-circuit output current, I_{SC}	$V_{CC} = 5$ V, $V_O = 0$ V	-5		-5		mA
Supply current, I_{CC}	$V_{CC} = 5$ V, $V_I = 0$ V	8		8		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

1. All values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and inputs at 0 V.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	SN74LS249		SN74ALS249		UNIT
		MIN	TYP	MIN	MAX	
Propagation delay time, low-to-high-level output from A input	$C_L = 15$ pF, $R_L = 2$ k Ω	100		100		ns
Propagation delay time, high-to-low-level output from A input	See Note 3	100		100		ns
Propagation delay time, high-to-low-level output from B1 input	$C_L = 15$ pF, $R_L = 2$ k Ω	100		100		ns
Propagation delay time, low-to-high-level output from B1 input	See Note 3	100		100		ns

NOTE 3: See General Information section for load circuit and waveform.

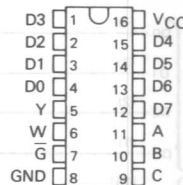


TYPES SN54251, SN54LS251, SN54S251, SN74251, SN74LS251 (TIM9905), SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

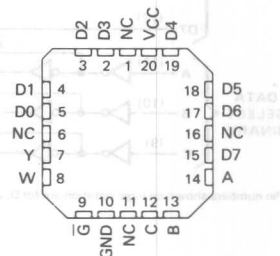
DECEMBER 1972—REVISED APRIL 1985

- Three-State Versions of '151, 'LS151, 'S151
- Three-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Permit Multiplexing from N-lines to One Line
- Complementary Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL Circuits

SN54251, SN54LS251, SN54S251 ... J OR W PACKAGE
SN74251 ... J OR N PACKAGE
SN74LS251, SN74S251 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS251, SN54S251 ... FK PACKAGE
SN74LS251, SN74S251
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT	ENABLE			Y	W
C	B	A	G		
X	X	X	H	Z	Z
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 ... D7 = the level of the respective D input

TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL AVG PROP DELAY TIME (D TO Y)	TYPICAL POWER DISSIPATION
SN54251	49	17 ns	250 mW
SN74251	129	17 ns	250 mW
SN54LS251	49	17 ns	35 mW
SN74LS251	129	17 ns	35 mW
SN54S251	39	8 ns	275 mW
SN74S251	129	8 ns	275 mW

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

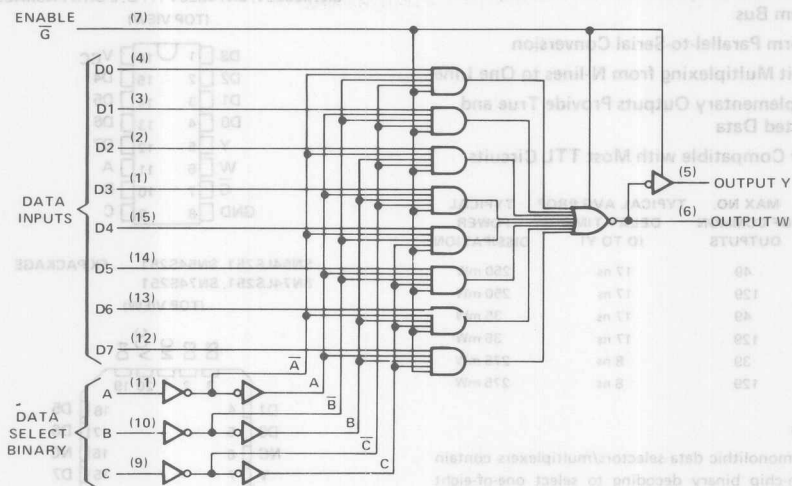
TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN54251, SN54LS251, SN54S251, SN74251, SN74LS251 (TIM9905), SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

FUNCTION TABLE

DATA SELECT BINARY	A	B	C	SELECT		ENABLE	Y	W
				D0	D1			
00	0	0	0	D0	D1	0	0	0
01	0	0	1	D0	D1	0	0	0
10	0	1	0	D0	D1	0	0	0
11	0	1	1	D0	D1	0	0	0
00	1	0	0	D0	D1	0	0	0
01	1	0	1	D0	D1	0	0	0
10	1	1	0	D0	D1	0	0	0
11	1	1	1	D0	D1	0	0	0

H = high logic level, L = low logic level
X = impedance, S = high impedance (off)
00, 01, 10, 11 = the level of the respective D inputs

3

TTL DEVICES

TYPES SN54251, SN74251

DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54251	-55°C to 125°C
SN74251	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54251			SN74251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-5.2	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.2		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_{OZ}	Off-state (high-impedance-state) output current	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}$	$V_O = 2.4 \text{ V}$ $V_O = 0.4 \text{ V}$		40 -40	μA
V_O	Output clamp voltage	$V_{CC} = \text{MAX}, V_{IH} = 4.5 \text{ V}$	$I_O = -12 \text{ mA}$ $I_O = 12 \text{ mA}$		-1.5 $V_{CC} + 1.5$	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-18	-55	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{All inputs at } 4.5 \text{ V}, \text{All outputs open}$		38	62	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

3

TTL DEVICES

TYPES SN54251, SN74251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	$C_L = 50\text{ pF}$, $R_L = 400\ \Omega$, See Note 2	29	45	ns	
t_{PHL}				28	45		
t_{PLH}	A, B, or C (3 levels)	W		20	33	ns	
t_{PHL}				21	33		
t_{PLH}	Any D	Y		17	28	ns	
t_{PHL}				18	28		
t_{PLH}	Any D	W		10	15	ns	
t_{PHL}				9	15		
t_{PZH}	\bar{G}	Y	17	27	ns		
t_{PZL}	\bar{G}	Y	26	40			
t_{PZH}	\bar{G}	W	17	27	ns		
t_{PZL}	\bar{G}	W	24	40			
t_{PHZ}	\bar{G}	Y	$C_L = 5\text{ pF}$, $R_L = 400\ \Omega$, See Note 2	5	8	ns	
t_{PLZ}	\bar{G}	Y		15	23		
t_{PHZ}	\bar{G}	W		5	8	ns	
t_{PLZ}				15	23		

[¶] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

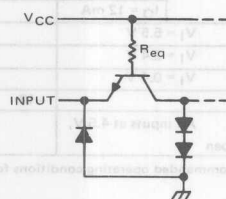
t_{PLZ} = Output disable time from low level

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

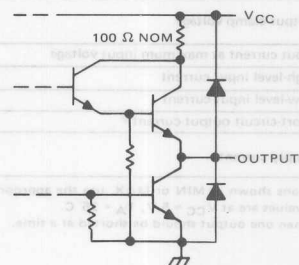
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Select: $R_{eq} = 6\text{ k}\Omega\text{ NOM}$
Other inputs: $R_{eq} = 4\text{ k}\Omega\text{ NOM}$

TYPICAL OF BOTH OUTPUTS



TTL DEVICES

TYPES SN54LS251, SN74LS251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS251	55°C to 125°C
SN74LS251	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS251			SN74LS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS251		SN74LS251		UNIT
				MIN	TYP ‡ MAX	MIN	TYP‡ MAX	
V _{IK}		V _{CC} = MIN, I _I = − 18 mA	− 1.5		− 1.5		V	
V _{OH}		V _{CC} = MIN, I _{OH} = MAX, V _{IH} = 2 V, V _{IL} = MAX	2.4	3.4	2.4	3.1	V	
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA		0.25	0.4	V	
		I _{OL} = 8 mA		0.35 0.5				
I _{OZ}		V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.7 V		20	20	μA	
			V _O = 0.4 V		− 20	− 20		
I _I		V _{CC} = MAX, V _I = 7 V			0.1	0.1	mA	
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20	20	μA	
I _{IL}	Enable G	V _{CC} = MAX, V _I = 0.4			− 0.2	− 0.2	mA	
	All other				− 0.4	− 0.4		
I _{OS} §		V _{CC} = MAX	− 30	− 130	− 30	− 130	mA	
I _{CC}		V _{CC} = MAX, See Note 3	Condition A	6.1	10	6.1	10	mA
			Condition B	7.1	12	7.1	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the outputs open and all data and select inputs at 4.5 V under the following conditions:

- A. Enable grounded.
- B. Strobe at 4.5 V.

3

TTL DEVICES

TYPES SN54LS251, SN74LS251 (TIM9905) DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	A, B, or C (4 levels)	Y	CL = 5 pF, RL = 2 kΩ, See Note 2	29	45	ns	
tPHL				28	45		
tPLH	A, B, or C (3 levels)	W		20	33	ns	
tPHL				21	33		
tPLH	Any D	Y		17	28	ns	
tPHL				18	28		
tPLH	Any D	W		10	15	ns	
tPHL				9	15		
tPZH	G	Y		30	45	ns	
tPZL				26	40		
tPZH	G	W		17	27	ns	
tPZL				24	40		
tPHZ	G	Y	CL = 15 pF, RL = 2 kΩ, See Note 2	30	45	ns	
tPLZ				15	25		
tPHZ	G	W		37	55	ns	
tPLZ				15	25		

[†] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

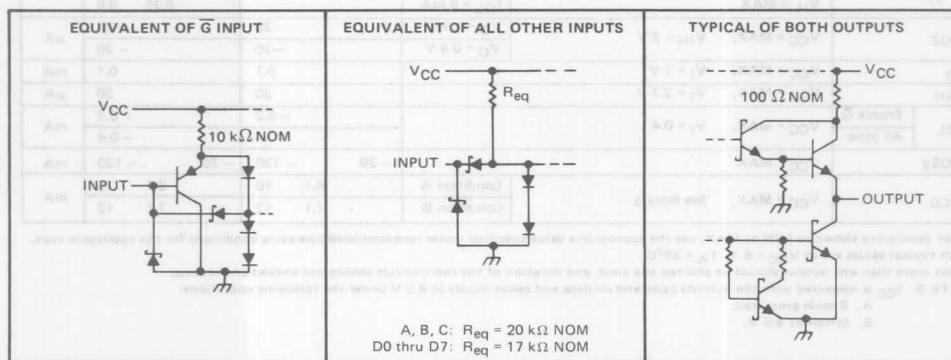
t_{PLZ} = Output disable time from low level

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

schematics of inputs and outputs

TTL DEVICES



TYPES SN54S251, SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S251	-55°C to 125°C
SN74S251	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S251			SN74S251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = \text{MAX}$	SN54S [§]	2.4	3.4	V
		SN74S [§]	2.4	3.2	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.5	V
I_{OZ} Off-state (high-impedance-state) output current	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$	$V_O = 2.4 \text{ V}$		50	μA
		$V_O = 0.5 \text{ V}$		50	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			50	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$			2	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$		40	100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, All inputs at 4.5 V, All outputs open		55	95	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

3

TTL DEVICES

TYPES SN54S251, SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	A, B, or C (4 levels)	Y	CL = 15 pF, RL = 280 Ω, See Note 2	12	18	ns	
tPHL				13	19.5		
tPLH	A, B, or C (3 levels)	W		10	15	ns	
tPHL				9	13.5		
tPLH	Any D	Y		8	12	ns	
tPHL				8	12		
tPLH	Any D	W		4.5	7	ns	
tPHL				4.5	7		
tPZH	G̅	Y	CL = 50 pF, RL = 280 Ω, See Note 2	13	19.5	ns	
tPZL				14	21		
tPZH	G̅	W		13	19.5	ns	
tPZL				14	21		
tPHZ	G̅	Y		5.5	8.5	ns	
tPLZ				9	14		
tPHZ	G̅	W		5.5	8.5	ns	
tPLZ				9	14		

[†] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

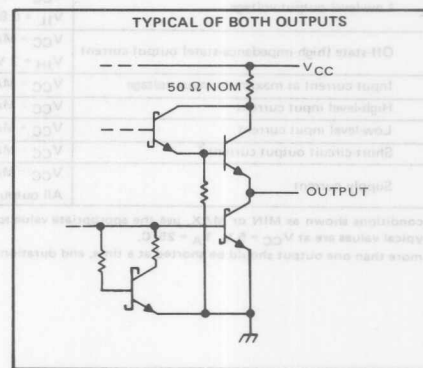
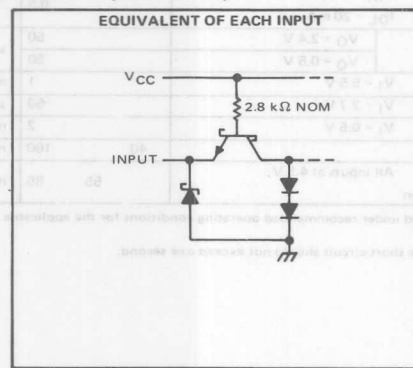
t_{PLZ} = Output disable time from low level

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

schematics of inputs and outputs



TYPES SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SEPTEMBER 1972 — REVISED DECEMBER 1983

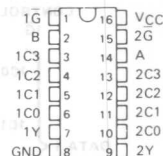
- Three-State Version of SN54/74LS153, SN54/74S153

SN54LS253, SN54S253 . . . J OR W PACKAGE
SN74LS253, SN74S253 . . . D, J OR N PACKAGE

- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Fully Compatible with Most TTL Circuits
- Low Power Dissipation

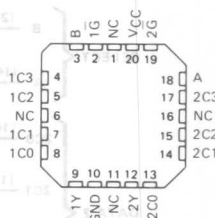
'LS253 . . . 35 mW Typical
'S253 . . . 225 mW Typical

(TOP VIEW)



SN54LS253, SN54S253 . . . FK PACKAGE
SN74LS253, SN74S253

(TOP VIEW)



NC No internal connection

description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	X	Z
L	L	L	X	X	X	H	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS253	7 V
'S253	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS253, SN54S253	-55°C to 125°C
SN74LS253, SN74S253	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

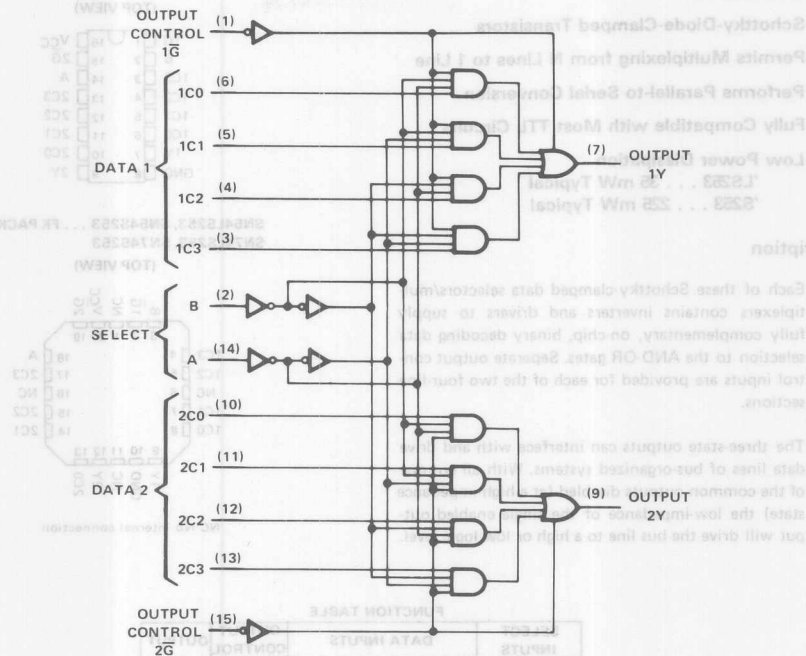
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TEXAS
INSTRUMENTS

3-723

TYPES SN54LS253, SN54S253, SN74LS253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

DATA INPUTS	CONTROL	OUTPUT
B	A	Y
X	X	X
L	L	L
L	H	X
L	X	X
L	H	X
L	X	X
H	L	X
H	X	X
H	L	X
H	X	X
H	H	X

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS253	7 V
'S253	8.8 V
Off-state output voltage	8.8 V
Operating free-air temperature range: SN54LS253, SN54S253	-55°C to 125°C
SN74LS253, SN74S253	0°C to 70°C
Storage temperature range	-55°C to 150°C

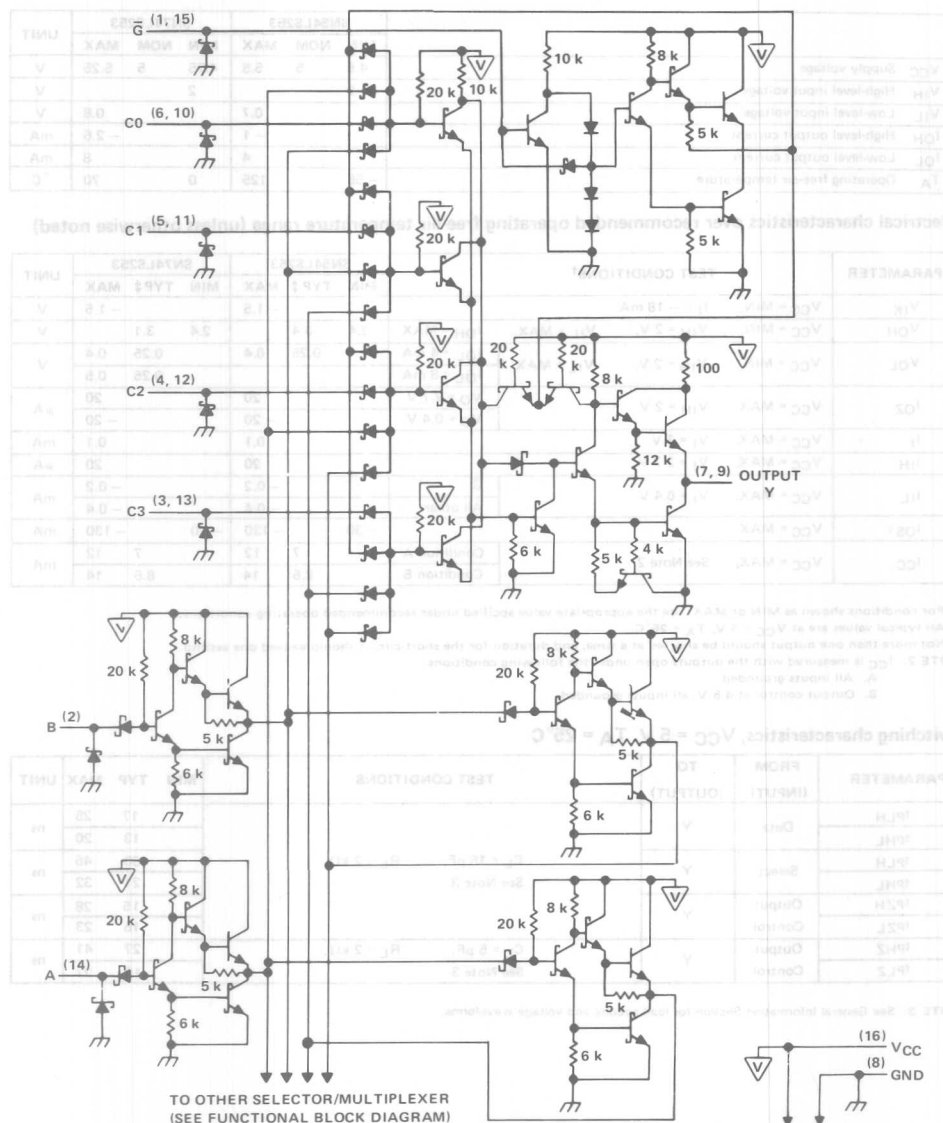
NOTE 1: Voltage values are with respect to network ground terminal.

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TEXAS
INSTRUMENTS

TYPES SN54LS253, SN74LS253, DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

schematic (each selector/multiplexer, and the common select section)



3

TTL DEVICES

TYPES SN54LS253, SN74LS253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54LS253			SN74LS253			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-1			-2.6	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS253			SN74LS253			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.4	3.1		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 8 mA					0.25	0.5	
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.7 V			20			20	µA
		V _O = 0.4 V			-20			-20	
I _I	V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				20			20	µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	G			-0.2			-0.2	mA
		All other			-0.4			-0.4	
I _{OS} §	V _{CC} = MAX		-30		-130	-30		-130	mA
I _{CC}	V _{CC} = MAX, See Note 2	Condition A		7	12		7	12	mA
		Condition B		8.5	14		8.5	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration for the short-circuit should exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	$C_L = 15\text{ pF}, \quad R_L = 2\text{ k}\Omega,$ See Note 3		17	25	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			30	45	ns
t_{PHL}					21	32	
t_{PZH}	Output	Y	$C_L = 5\text{ pF}, \quad R_L = 2\text{ k}\Omega,$ See Note 3		15	28	ns
t_{PZL}	Control				15	23	
t_{PHZ}	Output	Y			27	41	ns
t_{PLZ}	Control				18	27	

NOTE 3: See General Information Section for load circuits and voltage waveforms.



TO OTHER SELECTOR/MULTIPLEXER
(SEE FUNCTIONAL BLOCK DIAGRAM)

3

TTL DEVICES

TYPES SN54S253, SN74S253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54S253			SN74S253			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-2			-6.5	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.2	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	Series 54S	2.5	3.4		V
		Series 74S	2.7	3.4		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA				0.5	V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.4 V			50	μA
		V _O = 0.5 V			-50	
I _I	V _{CC} = MAX, V _I = 5.5 V				1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				50	μA
I _{IL}	V _{CC} = MAX, V _I = 0.5 V	\bar{G} = 0.8 V,			-2	mA
		\bar{G} = 2 V			-0.25	
I _{OS§}	V _{CC} = MAX		-40		-100	mA
I _{CC}	V _{CC} = MAX, See Note 2	Condition A		45	70	mA
		Condition B		65	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
¹ PLH	Data	Y	R _L = 280 Ω, See Note 3	C _L = 15 pF		6	9	ns
¹ PHL						6	9	
¹ PLH	Select	Y				11.5	18	ns
¹ PHL						12	18	
¹ PZH	Output	Y				11	16.5	ns
¹ PZL	Control					12	18	
¹ PHZ	Output	Y	R _L = 280 Ω, See Note 3	C _L = 5 pF		6.5	9.5	ns
¹ PLZ	Control					10	15	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS257B, SN54LS258B, SN54S257, SN54S258, SN74LS257B, SN74LS258B, SN74S257, SN74S258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

OCTOBER 1976 — REVISED DECEMBER 1983

- Three-State Outputs Interface Directly with System Bus
- 'LS257B and 'LS258B Offer Three Times the Sink-Current Capability of the Original 'LS257 and 'LS258
- Same Pin Assignments as SN54LS157, SN74LS157, SN54S157, SN74S157, and SN54LS158, SN74LS158, SN54S158, SN74S158
- Provides Bus Interface from Multiple Sources in High-Performance Systems

	AVERAGE PROPAGATION DELAY FROM DATA INPUT	TYPICAL POWER DISSIPATION†
'LS257B	9 ns	55 mW
'LS258B	9 ns	55 mW
'S257	4.8 ns	320 mW
'S258	4 ns	280 mW

† Off state (worst case)

description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin (\bar{G}) is at a high-logic level.

Series 54LS and 54S are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74LS and 74S are characterized for operation from 0°C to 70°C .

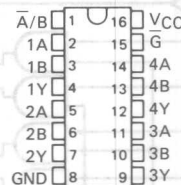
FUNCTION TABLE

OUTPUT CONTROL	INPUTS		OUTPUT Y		
	SELECT	A	B	'LS257B 'S257	'LS258B 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

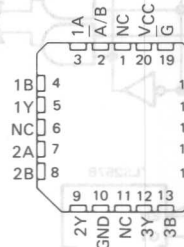
SN54LS257B, SN54S257, SN54LS258B, SN54S258 ... J OR W PACKAGE
SN74LS257B, SN74S257, SN74LS258B, SN74S258 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS257B, SN54S257, SN54LS258B, SN54S258, SN74LS257B, SN74S257, SN74LS258B, SN74S258 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection.

3

TTL DEVICES

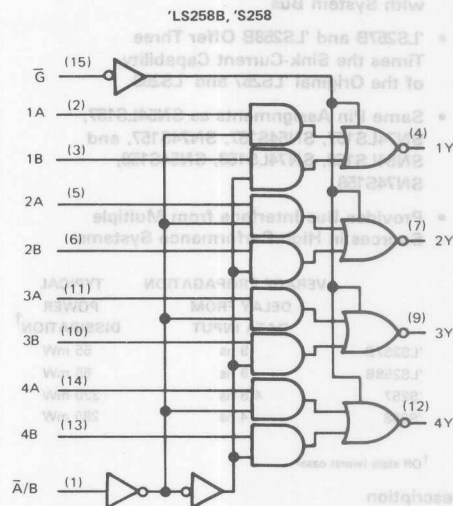
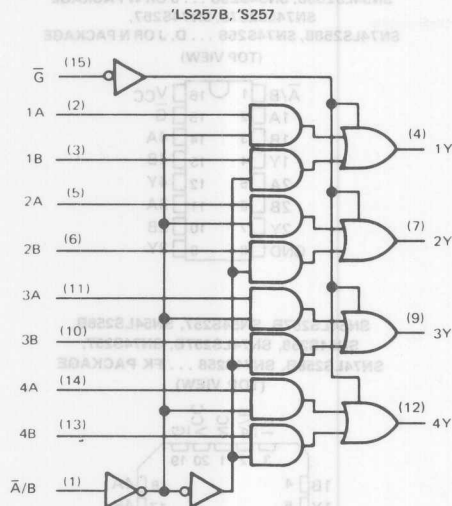
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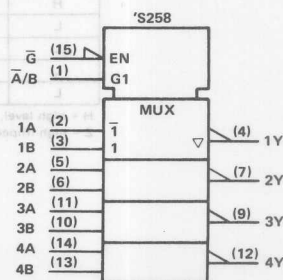
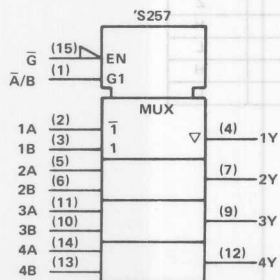
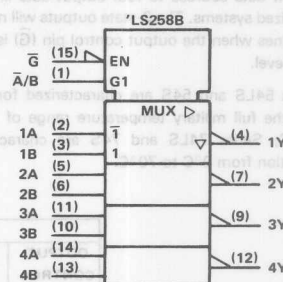
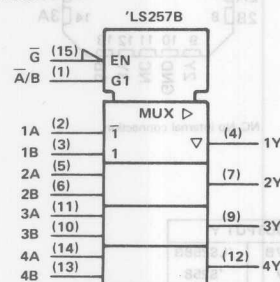
TEXAS
INSTRUMENTS

**TYPES SN54LS257B, SN54LS258B, SN54S257, SN54S258,
SN74LS257B, SN74LS258B, SN74S257, SN74S258
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

logic diagrams



logic symbol

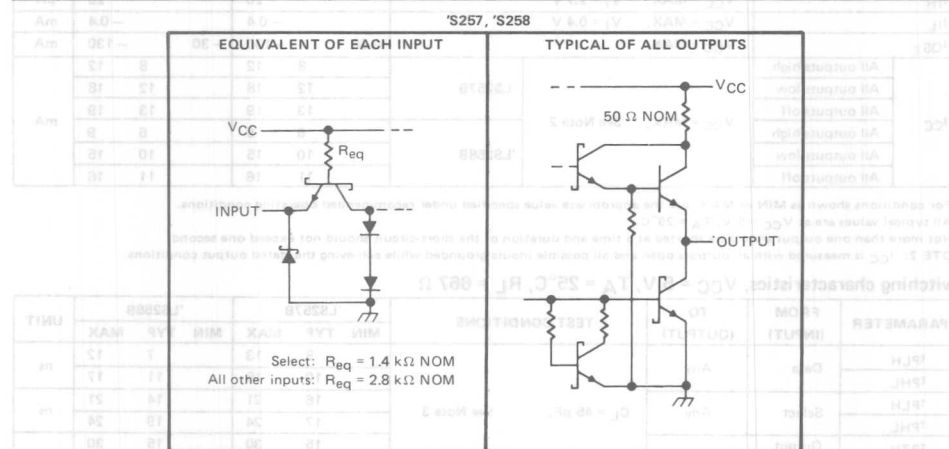
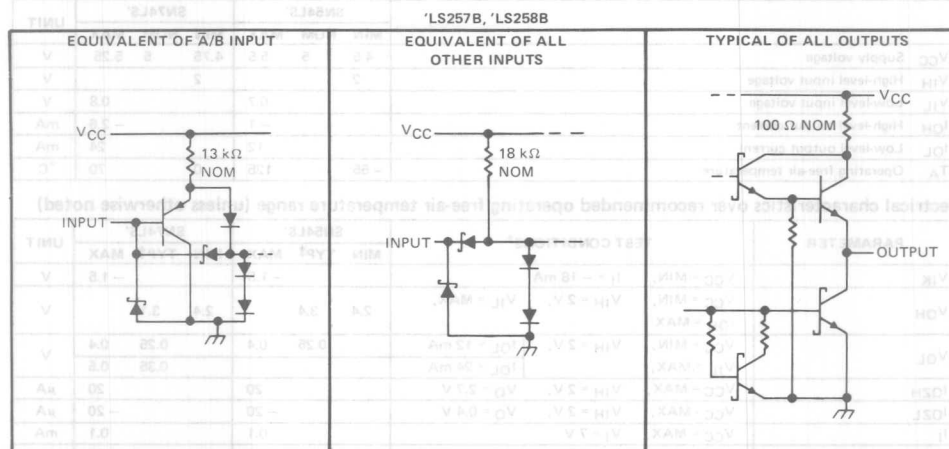


Pin numbers shown on logic notation are for D, J or N packages.

3 TTL DEVICES

TYPES SN54LS257B, SN54LS258B, SN54S257, SN54S258,
SN74LS257B, SN74LS258B, SN74S257, SN74S258
QUADRUPL 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS257B, 'LS258B Circuits	7 V
'S257, 'S258 Circuits	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits	-55°C to 125°C
SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS257B, SN54LS258B, SN74LS257B, SN74LS258B QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-1			-2.6	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.4	3.1		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 12 mA			0.25	0.4		0.25	0.4	V
			I _{OL} = 24 mA					0.35	0.5	
I _{OZH}		V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V				20			20	μA
I _{OZL}		V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V				-20			-20	μA
I _I		V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V				20			20	μA
I _{IL}		V _{CC} = MAX, V _I = 0.4 V				-0.4			-0.4	mA
I _{OS} §		V _{CC} = MAX,		-30		-130	-30		-130	mA
I _{CC}	All outputs high	V _{CC} = MAX, See Note 2	'LS257B		8	12		8	12	mA
	All outputs low				12	18		12	18	
	All outputs off				13	19		13	19	
	All outputs high		'LS258B		6	9		6	9	
	All outputs low				10	15		10	15	
	All outputs off				11	16		11	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS257B			'LS258B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Data	Any	C _L = 45 pF, See Note 3		8	13		7	12	ns
t _{PHL}					10	15		11	17	
t _{PLH}	Select	Any			16	21		14	21	ns
t _{PHL}					17	24		19	24	
t _{PZH}	Output	Any	C _L = 5 pF, See Note 3		15	30		15	30	ns
t _{PZL}	Control				19	30		20	30	
t _{PHZ}	Output	Any			18	30		18	30	ns
t _{PLZ}	Control				16	25		16	25	

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

NOTE 3: See General Information Section for load circuits and voltage waveforms.

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

TYPES SN54S257, SN54S258, SN74S257, SN74S258

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'S257			'S258			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage				2			2			V
V _{IL}	Low-level input voltage				0.8			0.8			V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = −1 mA	SN74S'	2.7		2.7		V		
				SN54S'	2.4	3.4	2.4	3.4			
			V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	SN74S'	2.4	3.2	2.4	3.2			
				SN54S'	2.4	3.2	2.4	3.2			
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA		0.5			0.5			V
I _{OZH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V		50			50			μA
I _{OZL}	Off-state output current, low-level voltage applied		V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V		−50			−50			μA
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 5.5 V		1			1			mA
I _{IH}	High-level input current	S input	V _{CC} = MAX, V _I = 2.7 V		100			100			μA
		Any other			50			50			
I _{IL}	Low-level input current	S input	V _{CC} = MAX V _I = 0.5 V		−4			−4			mA
		Any other			−2			−2			
I _{OS}	Short-circuit output current §		V _{CC} = MAX		−40 −100			−40 −100			mA
I _{CC}	Supply current	All outputs high	V _{CC} = MAX, See Note 2		44 68			36 56			mA
		All outputs low			60 93			52 81			
		All outputs off			64 99			56 87			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}, R_L = 280 \Omega$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S257			'S258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
[†] PLH	Data	Any	C _L = 15 pF, See Note 3		5	7.5		4	6	ns
[†] PHL					4.5	6.5		4	6	
[†] PLH	Select	Any			8.5	15		8	12	ns
[†] PHL					8.5	15		7.5	12	
[†] PZH	Output	Any			13	19.5		13	19.5	ns
[†] PZL	Control				14	21		14	21	
[†] PHZ	Output		Any	C _L = 5 pF, See Note 3		5.5	8.5		5.5	8.5
[†] PLZ	Control				9	14		9	14	

¶ f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 3: See General Information Section for load circuits and voltage waveforms.

QUADRUPEL 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLXERS

TYPES SN542257, SN542258, SN742257, SN742258

recommended operating conditions

PARAMETER	SN542257		SN742257		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	5	4.5	5	V
High-level output current, I_{OH}	-2		-2		mA
Low-level output current, I_{OL}	20		20		mA
Operating free-air temperature, T_A	-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹		SN542257		SN742257		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH} High-level input voltage			2		2		V
V_{IL} Low-level input voltage			0.8		0.8		V
V_{IC} Input clamp voltage			-1.5		-1.5		V
V_{OH} High-level output voltage			2.7	2.7	2.7	2.7	V
V_{OL} Low-level output voltage			0.8	0.8	0.8	0.8	V
I_{OZH} Off-state output current, high-level voltage applied			20	20	20	20	mA
I_{OLZ} Off-state output current, low-level voltage applied			-20	-20	-20	-20	mA
I_I Input current at maximum input voltage			1	1	1	1	mA
I_{IH} High-level input current			100	100	100	100	mA
I_{IL} Low-level input current			-4	-4	-4	-4	mA
I_{OZ} Short-circuit output current ²			-40	-40	-40	-40	mA
I_{CC} Supply current			64	64	64	64	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
² All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.
³ Input current at any other input voltage should be limited to a time and duration of the input voltage should not exceed the second.
⁴ I_{CC} is measured with all outputs high and all disabled inputs grounded while allowing the stated output conditions.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, $R_L = 280$ Ω

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	7503		2588		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Data	Any	$C_L = 15\text{ pF}$, See Note 3	4.5	8.5	4	8	ns
				4.5	8.5	4	8	
t_{PLH}	Data	Any		4.5	8.5	4	8	ns
				4.5	8.5	4	8	
t_{PHZ}	Output	Any		4.5	8.5	4	8	ns
				4.5	8.5	4	8	
t_{PLZ}	Output	Any		4.5	8.5	4	8	ns
				4.5	8.5	4	8	

¹ MAX = Maximum clock frequency.
² t_{PLH} = Propagation delay time, low-to-high input.
³ t_{PLH} = Propagation delay time, high-to-low input.
⁴ t_{PHZ} = Output enable time to high level.
⁵ t_{PLZ} = Output enable time to low level.

NOTE 3: See Timing Information section for load circuit and voltage waveform.

3 TTL DEVICES

TYPES SN54259, SN54LS259B, SN74259, SN74LS259B 8-BIT ADDRESSABLE LATCHES

REVISED DECEMBER 1983

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

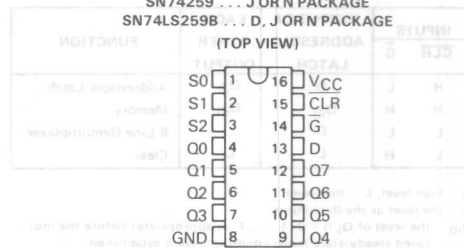
description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

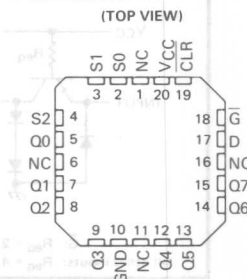
Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (G) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable G should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54259 and SN54LS259B are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74259 and SN74LS259B are characterized for operation from 0°C to 70°C .

SN54259, SN54LS259B ... J OR W PACKAGE
SN74259 ... J OR N PACKAGE
SN74LS259B ... D, J OR N PACKAGE

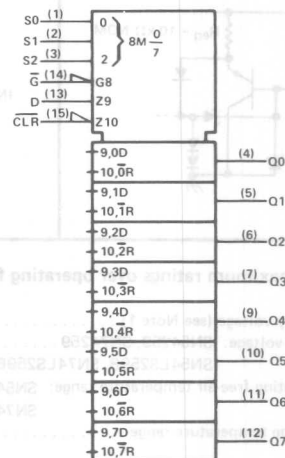


SN54LS259B ... FK PACKAGE
SN74LS259B



NC - No internal connection

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

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TEXAS
INSTRUMENTS

3-735

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TTL DEVICES

TYPES SN54259, SN54LS259B, SN74259, SN74LS259B 8-BIT ADDRESSABLE LATCHES

REVISED DECEMBER 1982

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLR	G			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

H = high level, L = low level

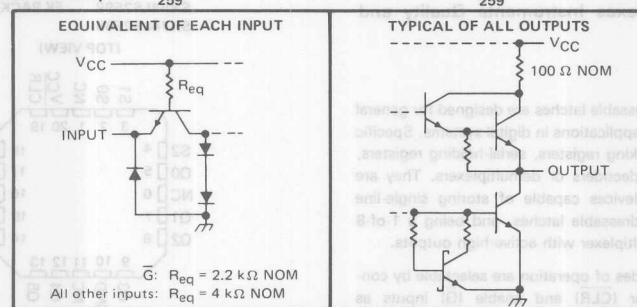
D = the level at the data input

Q_{i0} = the level of Q_i ($i = 0, 1, \dots, 7$, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

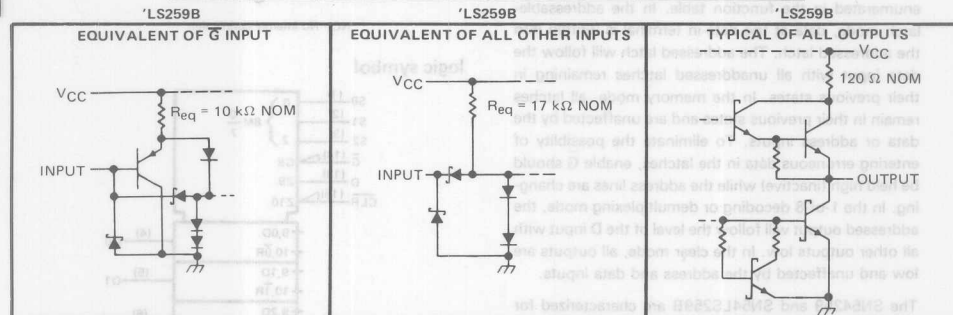
SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

schematic of inputs and outputs



3

TTL DEVICES



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: SN54259, SN74259	5.5 V
SN54LS259B, SN74LS259B	7 V
Operating free-air temperature range: SN54259, SN54LS259B	-55°C to 125°C
SN74259, SN74LS259B	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54259, SN74259 8-BIT ADDRESSABLE LATCHES

recommended operating conditions

		SN54259			SN74259			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Width of clear or enable pulse, t_w		15			15			ns
Setup time, t_{su}	Data	15 \uparrow			15 \uparrow			ns
	Address	5 \uparrow			5 \uparrow			ns
Hold time, t_h	Data	0 \uparrow			0 \uparrow			ns
	Address	20 \uparrow			20 \uparrow			ns
Operating free-air temperature, T_A		-55	125		0	70		$^{\circ}$ C

\uparrow The arrow indicates that the rising edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54259			SN74259			UNIT
			MIN	TYP \ddagger	MAX	MIN	TYP \ddagger	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = 12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		80			80		μ A
	Other inputs			40			40		μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-3.2			-3.2		mA
	Other inputs			-1.6			-1.6		mA
I_{OS}	Short-circuit output current \S	$V_{CC} = \text{MAX}$	-18		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	60	90		60	90		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

\ddagger All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

\S Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	CLR	Any Q	C _L = 15 pF, R _L = 400 Ω, See Note 3		16	25	ns
t _{PLH}	Data	Any Q			14	24	ns
t _{PHL}					11	20	
t _{PLH}	Address	Any Q			15	28	ns
t _{PHL}					17	28	
t _{PLH}	G	Any Q			12	20	ns
t _{PHL}					11	20	

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS259B, SN74LS259B 8-BIT ADDRESSABLE LATCHES

recommended operating conditions

				SN54LS259B			SN74LS259B			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
I _{OH}	High-level output current					−0.4			−0.4	mA
I _{OL}	Low-level output current					4			8	mA
t _w	Pulse duration	\overline{G} low		17			17			ns
		CLR low		10			10			
t _{su}	Set up time	Data before $\overline{G} \uparrow$		20			20			ns
		Address before $\overline{G} \uparrow$		17			17			
		Address before $\overline{G} \downarrow$		0			0			
t _h	Hold time	Data after $\overline{G} \uparrow$		0			0			ns
		Address after $\overline{G} \uparrow$		0			0			
T _A	Operating free-air temperature				−55		125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS259B			SN74LS259B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -0.4 mA	V _{IL} = MAX,	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 8 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V				-0.4			-0.4	mA
I _{OS} §	V _{CC} = MAX		-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, See Note 2			27	36		22	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PHL}	CLR	Any Q	C _L = 15 pF, See Note 3	R _L = 2 kΩ,		12	18	ns
t _{PLH}	Data	Any Q				19	30	ns
t _{PHL}					13	20		
t _{PLH}	Address	Any Q				17	27	ns
t _{PHL}					14	20		
t _{PLH}					15	24		
t _{PHL}	\overline{G}	Any Q				15	24	ns

t_{PLH} = propagation delay time, low-to-high level output

t_{PHL} = propagation delay time, high-to-low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S260, SN74S260 DUAL 5-INPUT POSITIVE -NOR GATES

REVISED DECEMBER 1983

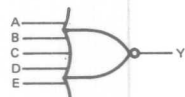
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 5-input positive -NOR gates. They perform the Boolean function $Y = A + B + C + D + E$ in positive logic.

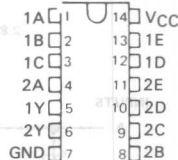
The SN54S260 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74S260 is characterized for operation from 0°C to 70°C .

logic diagram (each gate)



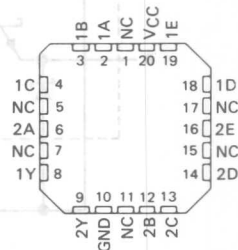
SN54S260 ... J OR W PACKAGE
SN74S260 ... D, J OR N PACKAGE

(TOP VIEW)



SN54S260 ... FK PACKAGE
SN74S260

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

PRODUCTION DATA

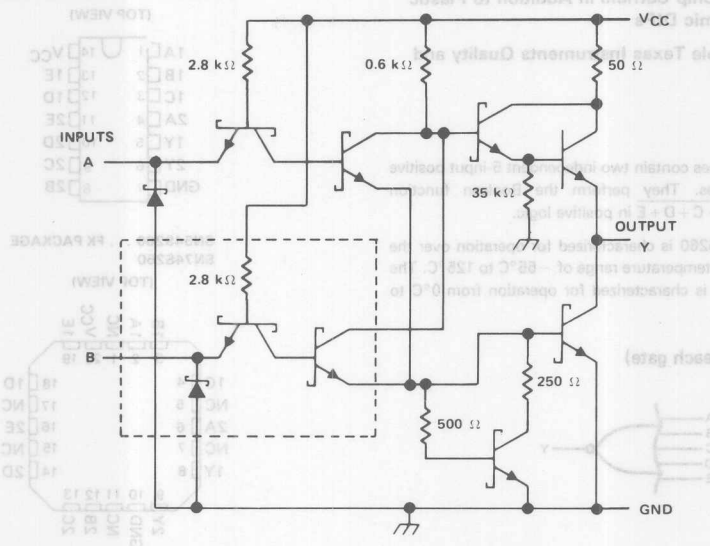
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TEXAS
INSTRUMENTS

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TYPES SN54S260, SN74S260 DUAL 5-INPUT POSITIVE -NOR GATES

schematic (each gate)



Resistor values shown are nominal.
The portion of the schematic within the dashed-line is repeated for each additional input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54S260, SN74S260 DUAL 5-INPUT POSITIVE -NOR GATES

recommended operating conditions

	SN54S260			SN74S260			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-1			-1	mA
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S260			SN74S260			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _{IH} = 2.7 V			50			50	μA
I _{IL}	V _{CC} = MAX, V _{IL} = 0.5 V			-2			-2	mA
I _{OS} §	V _{CC} = MAX	-40		-100	-40		-100	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		17	29		17	29	mA
I _{CCL}	V _{CC} = MAX, See Note 2		26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 280 Ω, C _L = 15 pF		4	5.5	ns
t _{PHL}					4	6	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

recommended operating conditions

UNIT	SN742580		SN542580	
	MIN	TYP	MAX	MIN
V _{CC} supply voltage	4.5	5	5.5	4.5
V _{OH} high-level output voltage	2			2
V _{OL} low-level output voltage	0.5			0.5
I _{OH} high-level output current	1			1
I _{OL} low-level output current	20			20
T _A operating free-air temperature	0		75	0

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

UNIT	SN742580		SN542580		TEST CONDITIONS	PARAMETER
	MIN	TYP	MAX	MIN		
V _{IK}	—	—	—	—	V _{CC} = MIN, I _I = —78 mA	V _{IK} = MIN
V _{OH}	2.5	3.4	5.0	2.5	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = —1 mA	V _{OH} = MIN
V _{OL}	0.5	0.5	0.5	0.5	V _{CC} = MIN, V _{IH} = 2.5 V, I _{OL} = 20 mA	V _{OL} = MIN
I _I	1			1	V _{CC} = MAX, V _I = 0.5 V	I _I = MAX
I _{IH}	80			80	V _{CC} = MAX, V _{IH} = 2.5 V	I _{IH} = MAX
I _{IL}	—2			—2	V _{CC} = MAX, V _{IL} = 0.5 V	I _{IL} = MAX
I _{IS}	—100			—100	V _{CC} = MAX	I _{IS} = MAX
I _{OCH}	15			15	V _{CC} = MAX, V _I = 0 V	I _{OCH} = MAX
I _{OCR}	20			20	V _{CC} = MAX, see Note 2	I _{OCR} = MAX

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2 All typical values are at V_{CC} = 5 V, T_A = 25°C.
3 Not more than one output should be driven at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 0.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

UNIT	MIN	TYP	MAX	TEST CONDITIONS	TO (OUTPUT)	FROM (INPUT)	PARAMETER
ns	4	5.5		R _L = 280 Ω, C _L = 15 pF	Y	Any	t _{PLH}
ns	4	5					t _{PLL}

NOTE 3: See General Information Section for load circuit and voltage waveform.

3

TTL DEVICES

TYPES SN54LS261, SN74LS261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLEXERS

MARCH 1974 — REVISED DECEMBER 1983

- Fast Multiplication . . . 5-Bit Product in 26 ns Typ
- Power Dissipation . . . 110 mW Typical
- Latch Outputs for Synchronous Operation
- Expandable for m-Bit-by-n-Bit Applications
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families
- Diode-Clamped Inputs Simplify System Design

description

These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

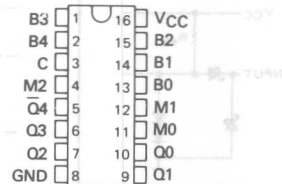
The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most-significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

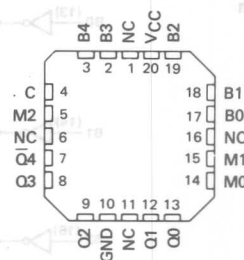
The SN54LS261 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS261 for operation from 0°C to 70°C .

SN54LS261 . . . J OR W PACKAGE
SN74LS261 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS261 . . . FK PACKAGE
SN74LS261

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

LATCH CONTROL C	INPUTS			OUTPUTS					
	MULTIPLIER			\bar{Q}_4	Q3	Q2	Q1	Q0	
	M2	M1	M0	\bar{Q}_4	Q3	Q2	Q1	Q0	
L	X	X	X	\bar{Q}_4	Q3	Q2	Q1	Q0	
H	L	L	L	H	L	L	L	L	
H	L	L	H	\bar{B}_4	B4	B3	B2	B1	
H	L	H	L	\bar{B}_4	B4	B3	B2	B1	
H	L	H	H	\bar{B}_4	B3	B2	B1	B0	
H	H	L	L	B4	\bar{B}_3	\bar{B}_2	\bar{B}_1	\bar{B}_0	
H	H	L	H	B4	\bar{B}_4	\bar{B}_3	\bar{B}_2	\bar{B}_1	
H	H	H	L	B4	\bar{B}_4	\bar{B}_3	\bar{B}_2	\bar{B}_1	
H	H	H	H	H	L	L	L	L	

H = high level, L = low level, X = irrelevant

\bar{Q}_4 . . . Q_0 = The logic level of the same output before the high-to-low transition of C.

B4 . . . B0 = The logic level of the indicated multiplicand (B) input.

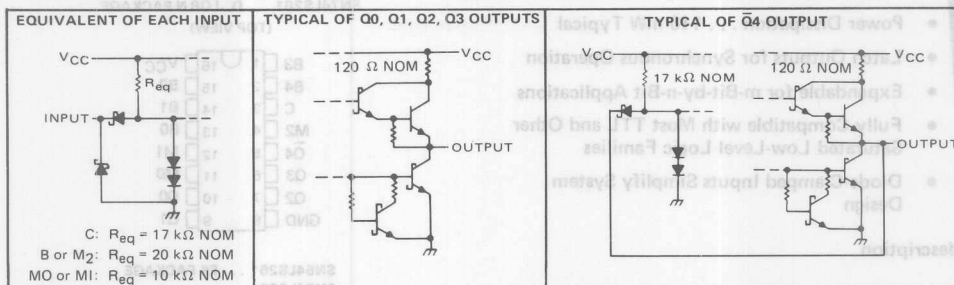
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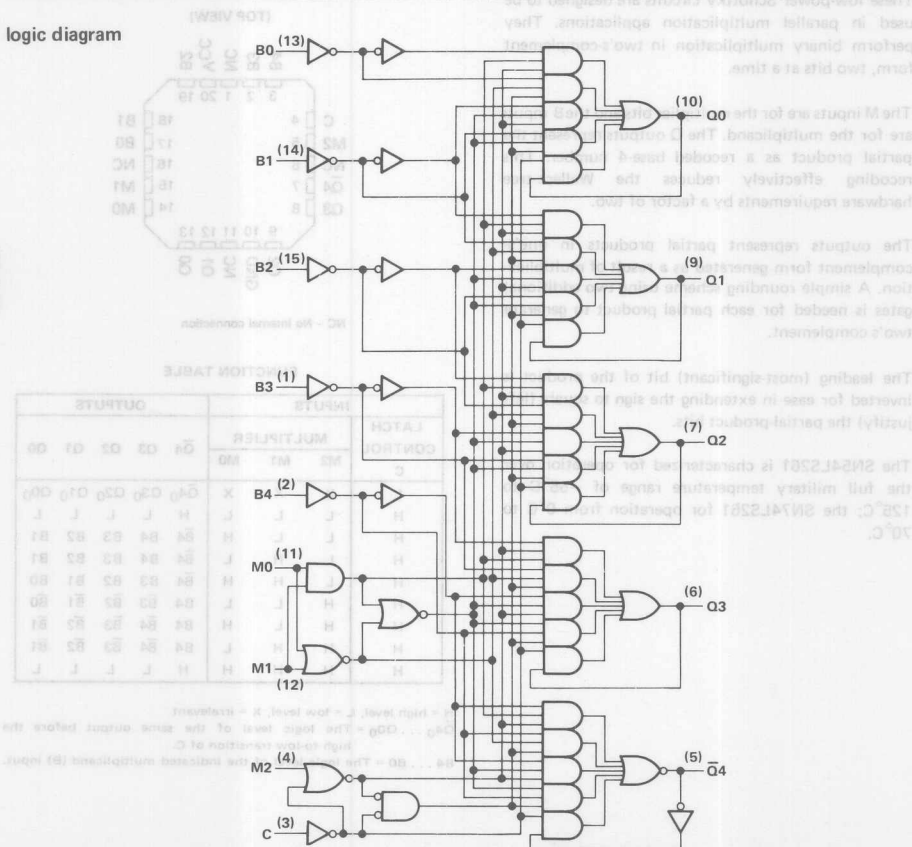
TEXAS
INSTRUMENTS

TYPES SN54LS261, SN74LS261 2-BIT BY 4-BIT PARALLEL BINARY MULTIPLEXERS

schematics of inputs and outputs



logic diagram



TYPES SN54LS261, SN74LS261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLEXERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS261	–55°C to 125°C
SN74LS261	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS261			SN74LS261			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–400			–400	μ A
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_W		25			25			ns
Setup time, t_{SU}	Any M input	17			17			ns
	Any B input	15			15			
Hold time, t_H	Any M input	0			0			ns
	Any B input	0			0			
Operating free-air temperature, T_A		–55		125	0		70	°C

† The arrow indicates that the falling edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS261			SN74LS261			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 8 \text{ mA}$			0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$	MO or MI		0.2	MO or MI		0.2	mA
		All others		0.1	All others		0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	MO or MI		40	MO or MI		40	μ A
		All others		20	All others		20	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	MO or MI		–0.8	MO or MI		–0.8	mA
		All others		–0.4	All others		–0.4	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, All inputs at 0 V, Outputs open	20	38		20	40		mA

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the output short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	C	Any Q	CL = 15 pF, RL = 2 kΩ, See Note 2	22	35	ns	
tPHL				20	30	ns	
tPLH	Any M input	Any Q		25	40	ns	
tPHL				22	35	ns	
tPLH	Any B input	Any Q		27	42	ns	
tPHL				24	37	ns	

¶ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS261, SN74LS261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLEXERS

TYPICAL APPLICATION DATA

Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:

	DECIMAL	BINARY	2-BIT-AT-A-TIME BINARY
UNIT			
B	26	011010	011010
M	29	011101	(+2) (-1) (+1)
V	234	011010	00000011010
A ₀	52	000000	111100110
A ₁	754	011010	0110100
A ₂		011010	01011110010
A ₃		011010	Product
A ₄		000000	Sign Bit
A ₅		01011110010	
A ₆		Sign Bit	
A ₇			
A ₈			
A ₉			
A ₁₀			
A ₁₁			
A ₁₂			
A ₁₃			
A ₁₄			
A ₁₅			

Two points should be noted in the two-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer.

A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.

2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	0
PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1									

Switching characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	C	Any D	C _L = 15 pF	22	35	38	ns
t _{PHL}	Any B input	Any D	R _L = 2 kΩ	20	30	34	ns
t _{PLH}	Any B input	Any D	See Note 2	22	40	44	ns
t _{PHL}	Any B input	Any D		21	42	46	ns
t _{PLH}	Any B input	Any D		24	37	40	ns

NOTE 2: See General Information Section for load circuit and voltage waveforms.

TYPES SN54LS261, SN74LS261

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLEXERS

TYPICAL APPLICATION DATA

2. Generate partial product (PPi) as shown in the following table:

MULTIPLIER BITS FROM			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
STEP 1				
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1 B	Copy multiplicand
0	1	0	+1 B	Copy multiplicand
0	1	1	+2 B	Shift multiplicand left one bit
1	0	0	-2 B	Shift two's complement of multiplicand left one bit
1	0	1	-1 B	Replace multiplicand by two's complement
1	1	0	-1 B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

3. Weight the partial products by indexing each two places left relative to the next-less-significant product.
4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.

EXAMPLE OF ALGORITHM

M = 29 = 011101

010
110
011

Operator
Symbol

B = 26 = 011010

+1 B
-1 B
+2 B

0000011010
1111001110
0110100

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 'LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

3

TTL DEVICES

TYPES SN54LS261, SN74LS261 2-BIT BY 4-BIT PARALLEL BINARY MULTIPLEXERS

TTL DEVICES

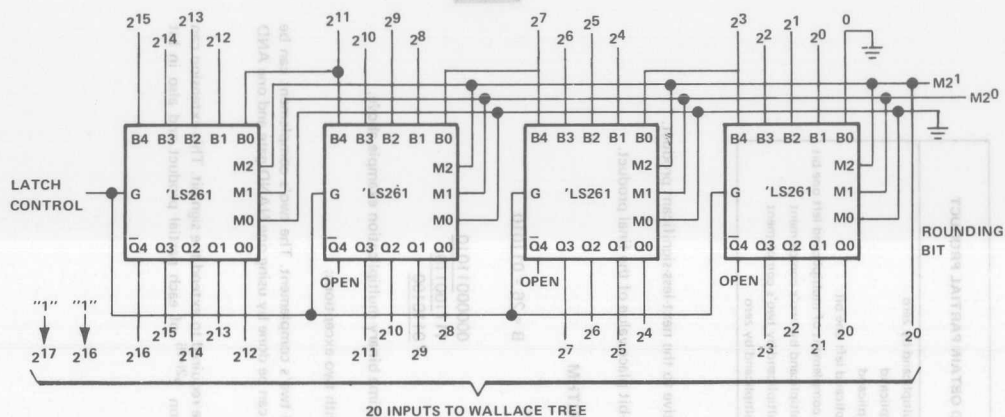


FIGURE A — FIRST PARTIAL PRODUCT, PPI

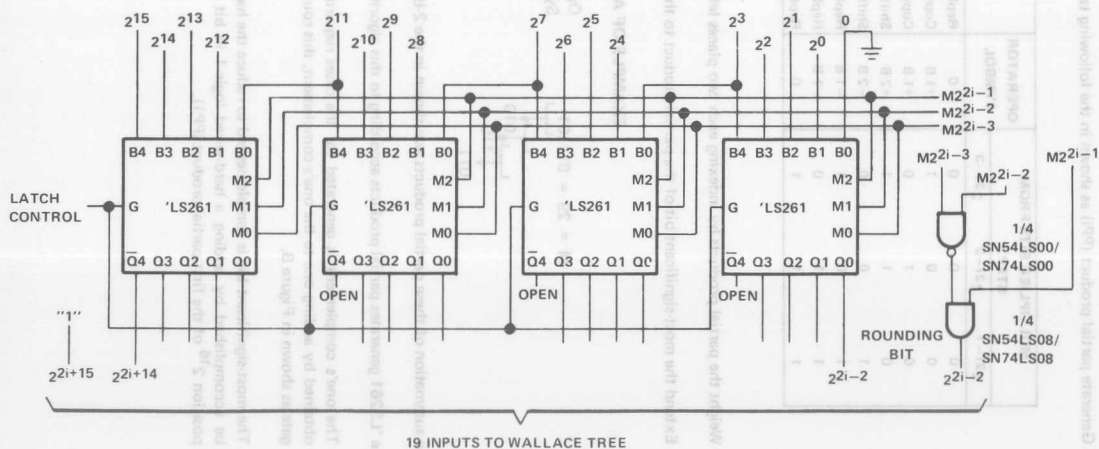


FIGURE B — OTHER PARTIAL PRODUCTS, PPI

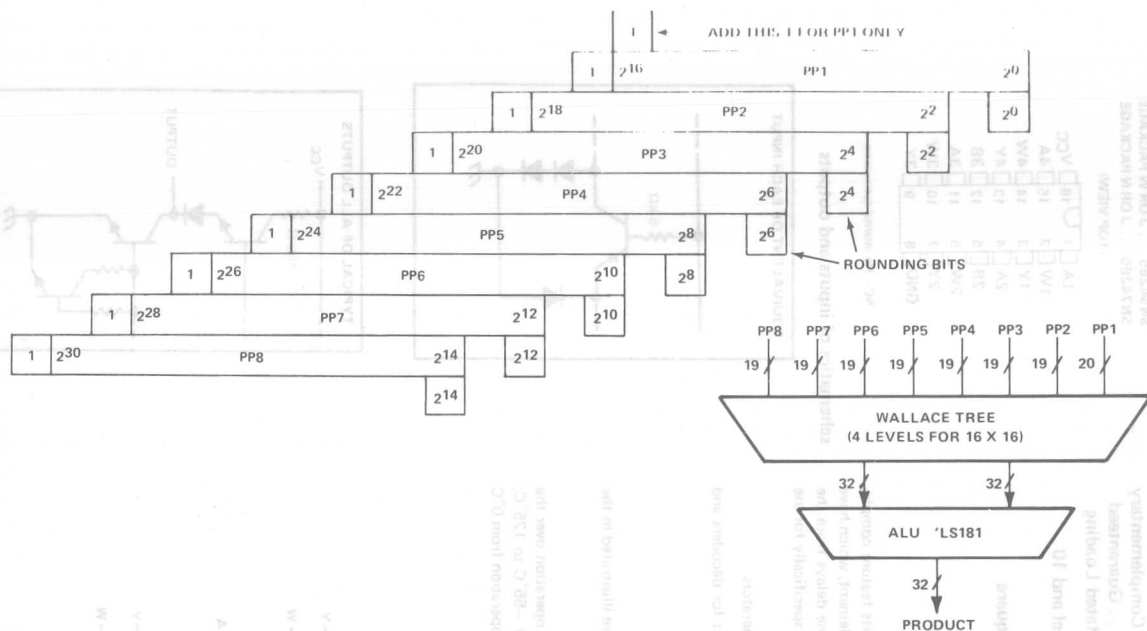


FIGURE C—MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 'LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 'LS261s, m x n ÷ 16 'LS00s, and m x n ÷ 16 'LS08s. The size of the Wallace tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

32	SN54LS261/SN74LS261
2	SN54LS00/SN74LS00
2	SN54LS08/SN74LS08
56	SN54LS183/SN74LS183
7	SN54LS181/SN74LS181
2	SN54S182/SN74S182

TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

REVISED DECEMBER 1983

FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Guaranteed to be No More than 3 ns at Rated Loading
- Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads
- Active Pull-Down Provides Square Transfer Characteristic

description

The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

- Symmetrical clock/clock generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

Examples of these four functions are illustrated in the typical application data.

The SN54265 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74265 is characterized for operation from 0°C to 70°C .

logic diagrams

ELEMENTS 1 and 4



positive logic

$$Y = \bar{A} \quad W = A$$

ELEMENTS 2 and 3



positive logic

$$Y = \overline{AB} \quad \text{or} \quad Y = \bar{A} + \bar{B}$$

$$W = AB \quad \text{or} \quad W = \bar{A} + \bar{B}$$

SN54265 . . . J OR W PACKAGE
SN74265 . . . J OR N PACKAGE

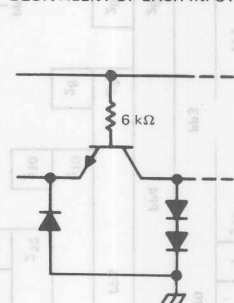
(TOP VIEW)

1A	1	16	VCC
1W	2	15	4A
1Y	3	14	4W
2A	4	13	4Y
2B	5	12	3B
2W	6	11	3A
2Y	7	10	3W
GND	8	9	3Y

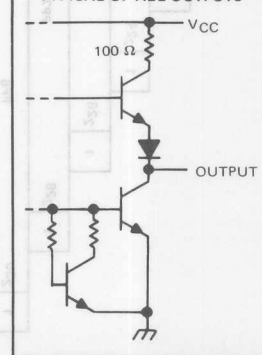
NC - No internal connection

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



PRODUCTION DATA

This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

3

TTL DEVICES

TYPES SN54265, SN74265

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54265	-55°C to 125°C
SN74265	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54265			SN74265			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$, SN54265	-20		-57	mA
	SN74265	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		25	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}(W)$	A or B	W	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$, See Note 3		11.6	18	ns
$t_{PHL}(Y)$	(as applicable)	Y			11.3	18	
$t_{PHL}(W)$	A or B	W			9.8	18	ns
$t_{PLH}(Y)$	(as applicable)	Y			10.2	18	
$t_{PLH}(W) - t_{PHL}(Y)$	A or B	W with respect to Y			+0.3	+3	ns
$t_{PHL}(W) - t_{PLH}(Y)$	(as applicable)				-0.4	+3	

¶ t_{PLH} = Propagation delay time, low-to-high-level output.

¶ t_{PHL} = Propagation delay time, high-to-low-level output.

¶ $t_{PXX}(W) - t_{PXX}(Y)$ = Difference in indicated propagation delay times at the W and Y outputs, respectively.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54265, SN74265
QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME DIFFERENCE
 VS
 FREE-AIR TEMPERATURE

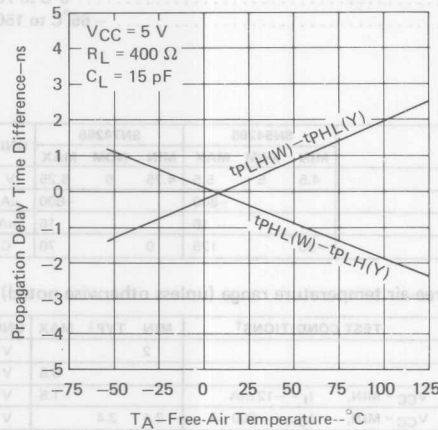


FIGURE 1

PROPAGATION DELAY TIME DIFFERENCE
 VS
 SUPPLY VOLTAGE

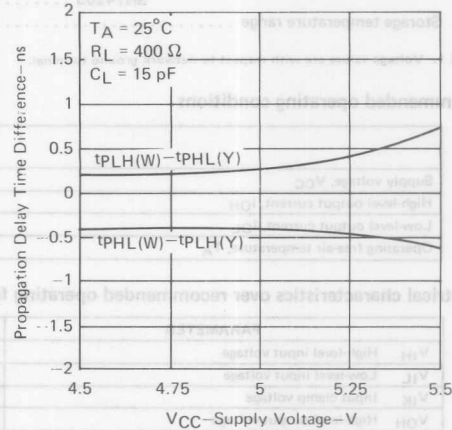


FIGURE 2

PROPAGATION DELAY TIME DIFFERENCE vs LOAD CAPACITANCE

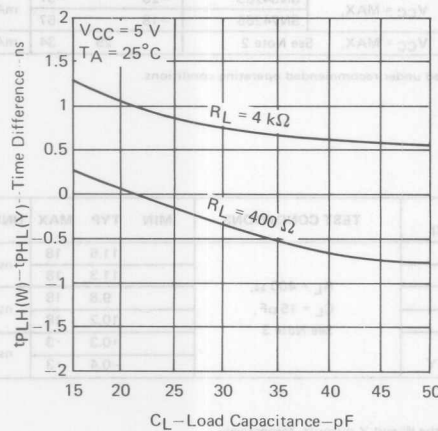


FIGURE 3

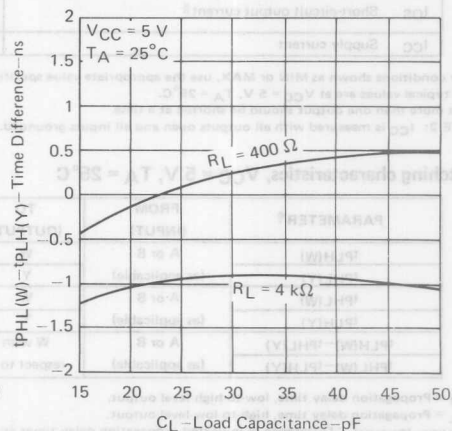


FIGURE 4

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54265 only.

TYPES SN54265, SN74265 QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL APPLICATION DATA

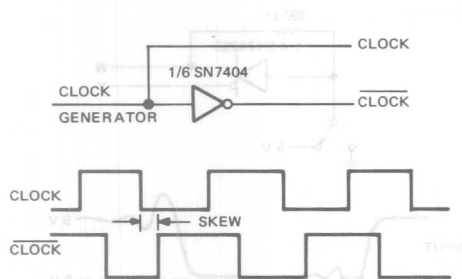


FIGURE A — TYPICAL CLOCK/CLOCK GENERATOR CIRCUIT

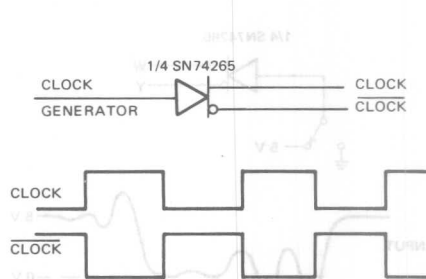


FIGURE B — SKEWLESS CLOCK/CLOCK GENERATOR CIRCUIT

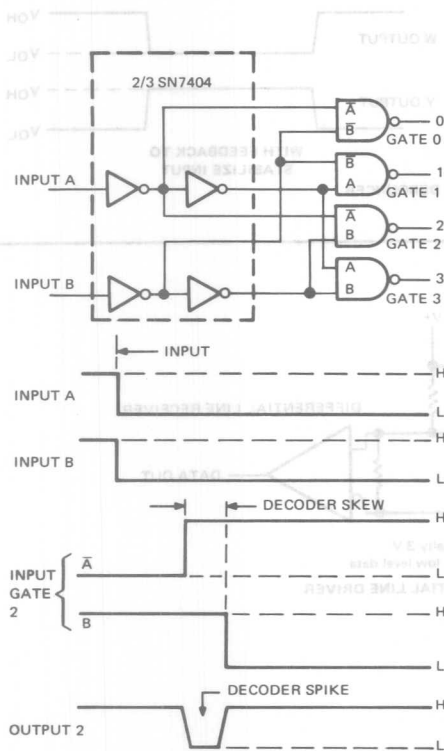


FIGURE C — TYPICAL DECODER/CODE CONVERTER

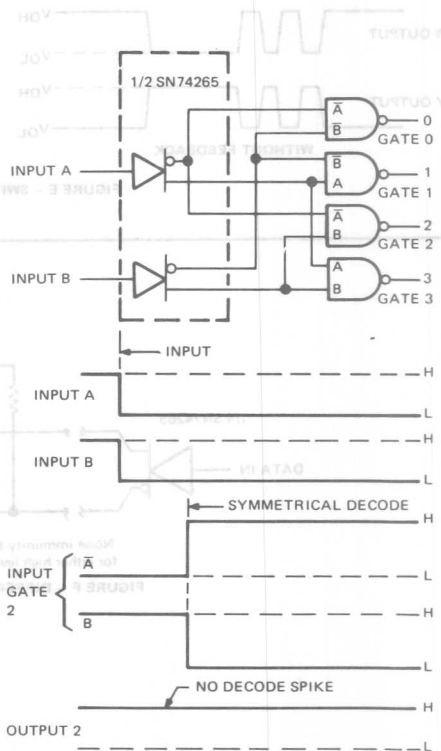


FIGURE D — SYMMETRICAL DECODER/CODE CONVERTER

3

TTL DEVICES

TYPES SN54265, SN74265

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

TYPICAL APPLICATION DATA

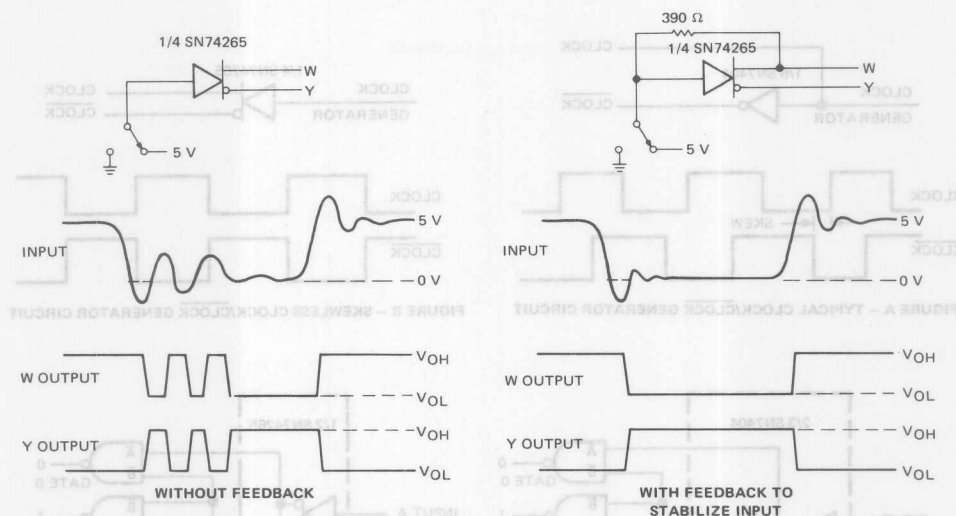


FIGURE E - SWITCH DEBOUNCER

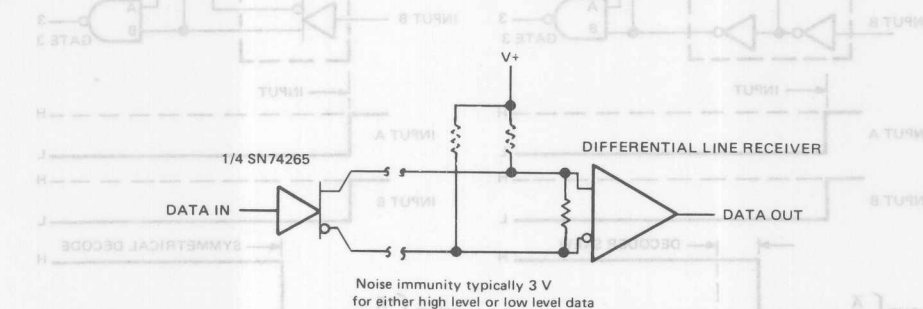


FIGURE F - DIFFERENTIAL LINE DRIVER

3

TTL DEVICES

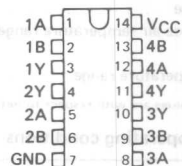
TYPES SN54LS266, SN74LS266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1972—REVISED DECEMBER 1983

- Can Be Used as a 4-Bit Digital Comparator
- Input Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

SN54LS266 ... J OR W PACKAGE
SN74LS266 ... D, J OR N PACKAGE

(TOP VIEW)



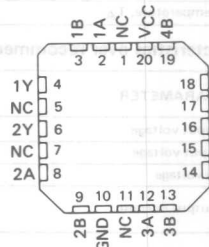
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

SN54LS266 ... FK PACKAGE
SN74LS266

(TOP VIEW)



NC - No internal connection

description

The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

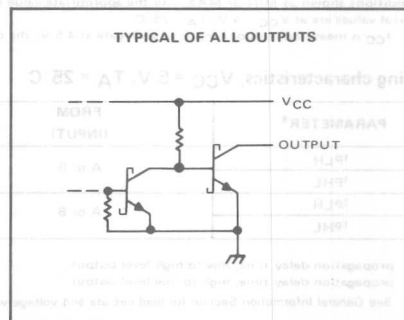
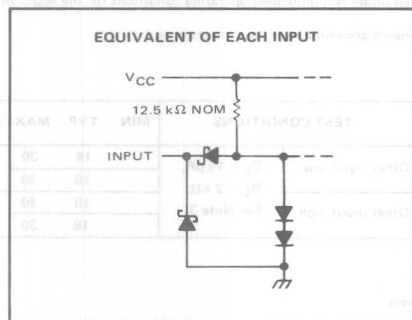
logic symbol (each gate)



positive logic

$$Y = A \oplus B = AB + \bar{A}\bar{B}$$

schematic of inputs and outputs



3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS266	-55°C to 125°C
SN74LS266	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS266			SN74LS266			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS266			SN74LS266			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 5.5 \text{ V}$			100			100	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	0.25	0.4		0.25	0.4		V
	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.2				0.2	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		40				40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.8				-0.8	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	8	13		8	13		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER‡	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3	18	30		ns
t_{PHL}				18	30		
t_{PLH}	A or B	Other input high	See Note 3	18	30		ns
t_{PHL}				18	30		

‡ t_{PLH} propagation delay time, low to high level output t_{PHL} propagation delay time, high to low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

OCTOBER 1976 • REVISED DECEMBER 1983

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
Buffer/Storage Registers
Shift Registers
Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

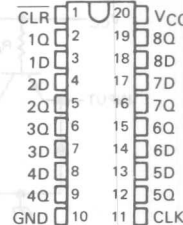
These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

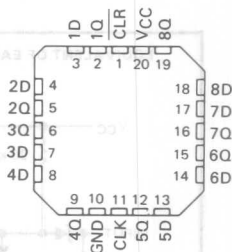
SN54273, SN54LS273 ... J PACKAGE
SN74273 ... J OR N PACKAGE
SN74LS273 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS273 ... FK PACKAGE
SN74LS273

(TOP VIEW)



3

TTL DEVICES

PRODUCTION DATA

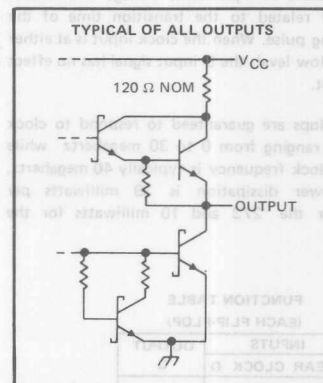
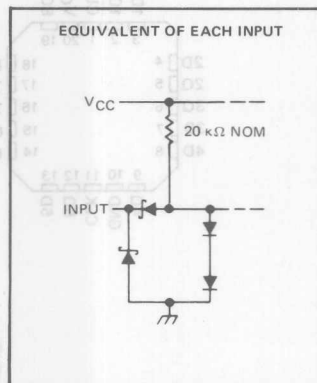
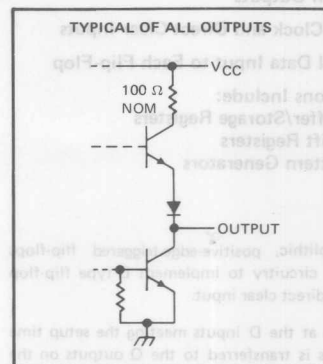
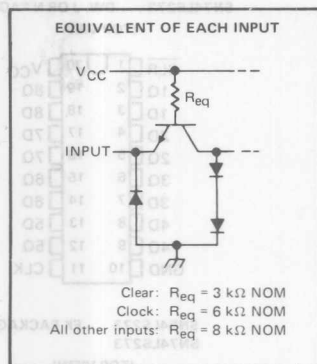
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TEXAS
INSTRUMENTS

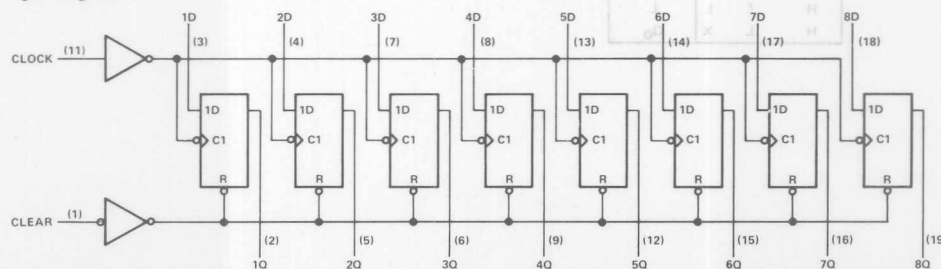
3-757

TYPES SN54273, SN74273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

schematics of inputs and outputs



logic diagram



Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54273, SN74273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature: SN54273	-55°C to 125°C
SN74273	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54273			SN74273			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, t_W		16.5			16.5		ns
Set-up time, t_{SU}		20†			20†		ns
Clear inactive state	25†			25†			ns
Data hold time, t_H		5†			5†		ns
Operating free-air temperature, T_A	-55		125	0		70	°C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	Clear			80	μ A
	Clock or D	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		40	
I_{IL} Low-level input current	Clear			-3.2	mA
	Clock or D	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-1.6	
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		62	94	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 3	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms

TYPES SN54LS273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS273	-55°C to 125°C
SN74LS273	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

				SN54LS273			SN74LS273			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}				4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}						-400			-400	μ A
Low-level output current, I_{OL}						4			8	mA
Clock frequency, f_{clock}				0		30	0		30	MHz
Width of clock or clear pulse, t_W					20			20		ns
Set-up time, t_{SU}				Data input	20†		20†			ns
				Clear inactive state	25†		25†			
Data hold time, t_H					5†			5†		ns
Operating free-air temperature, T_A				-55		125	0		70	°C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS273			SN74LS273			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}, V_{IL} = V_{ILmax}, I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = -0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20	-100		-20	-100		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	17	27		17	27		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}$		18	27	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	$R_L = 2 \text{ k}\Omega$		17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	See Note 4		18	27	ns

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TYPES SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

OCTOBER 1976—REVISED DECEMBER 1983

features

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Separate Negative-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Typical Clock Input Frequency . . . 50 MHz
- Fully Buffered Outputs

description

These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by up to 50%. They feature hysteresis at each clock input, fully buffered outputs, and direct clear capability, and are presettable through a buffer that also features an input hysteresis loop. The negative-edge-triggering clocks are directly compatible with earlier Series 54/74 single and dual pulse-triggered flip-flops. These circuits can be used to emulate D- or T-type flip-flops by hard-wiring the inputs, or to implement asynchronous sequential functions.

The SN54276 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74276 is characterized for operation from 0°C to 70°C .

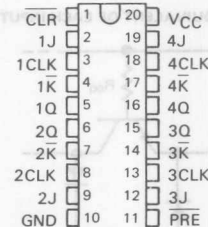
FUNCTION TABLE (EACH FLIP-FLOP)

COMMON INPUTS		INPUTS			OUTPUT
PRE	CLR	CLK	J	\bar{K}	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H^{\dagger}
H	H	\downarrow	L	H	Q_0
H	H	\downarrow	H	H	H
H	H	\downarrow	L	L	L
H	H	\downarrow	H	L	TOGGLE
H	H	H	X	X	Q_0

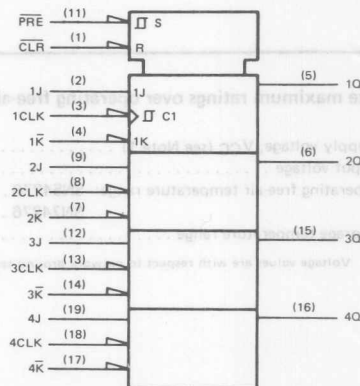
\dagger This configuration is nonstable; that is, it may not persist when preset and clear return to their inactive (high) level.

SN54276 . . . J PACKAGE
SN74276 . . . J OR N PACKAGE

(TOP VIEW)



logic symbol†



\dagger Pin numbers shown on logic symbol are for J and N packages only.

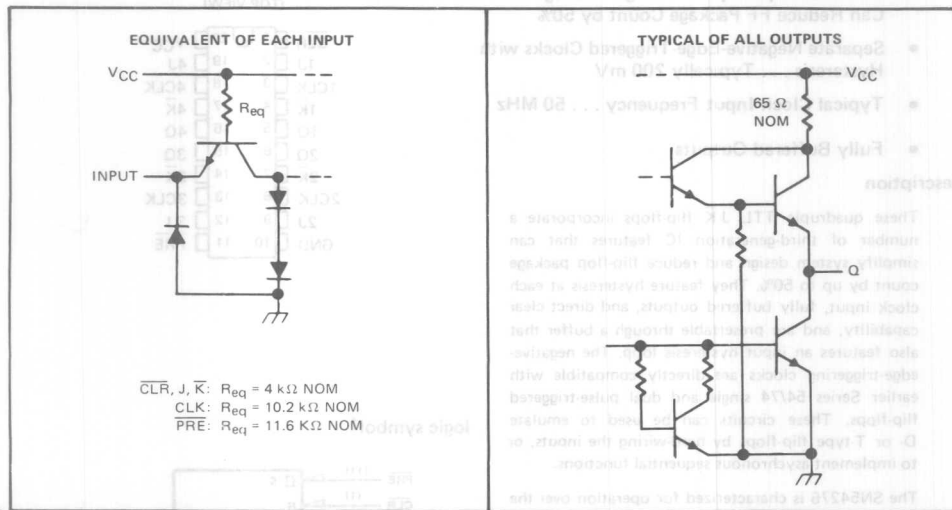
PRODUCTION DATA

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TEXAS
INSTRUMENTS

TYPES SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

schematics of inputs and outputs



3

TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54276	-55°C to 125°C
SN74276	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

recommended operating conditions

		SN54276			SN74276			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Clock frequency		0		35	0		35	MHz
Pulse width, t_W	Clock high	13.5			13.5			ns
	Clock low	15			15			
	Preset or clear low	12			12			
Setup time, t_{su}	J, K inputs	3↓			3↓			ns
	Clear and preset inactive state	10↓			10↓			
Input hold time, t_h		10↓			10↓			ns
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}$ C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$				40	μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$				-1.6	mA
I_{OS}	Short-circuit output current‡	$V_{CC} = \text{MAX}$		-30		-85	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			60	81	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		35	50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset	$C_L = 15 \text{ pF}$; $R_L = 400 \Omega$; See Note 2		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN74278		SN74279		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		4.5	5.5	4.5	5.5	V
High-level output current, I_{OH}			800		800	mA
Low-level output current, I_{OL}			15		15	mA
Clock frequency		0	30	0	30	kHz
Pulse width, μs	Clock high	13.5		13.5		ns
	Clock low	15		15		ns
	Setup to clock low	15		15		ns
	J-K inputs	31		31		ns
Setup time, μs		101		101		ns
Input hold time, μs		101		101		ns
Operating free-air temperature, T_A		-55	150	0	70	°C

1. The values indicated after the following sign are used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = 5V$, $I_K = -15mA$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = 5V$, $I_{OH} = 800\mu A$	3.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = 5V$, $I_{OL} = 15mA$		0.5	0.6	V
I_I Input current at maximum input voltage	$V_{CC} = 5V$, $V_I = 5V$			1	mA
I_{IH} High-level input current	$V_{CC} = 5V$, $V_I = 5V$			40	nA
I_{IL} Low-level input current	$V_{CC} = 5V$, $V_I = 0V$			-1.5	mA
I_{OS} Short-circuit output current	$V_{CC} = 5V$	-70		80	mA
I_{CC} Supply current	$V_{CC} = 5V$			81	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
3. Test inputs that are not specified should be treated as 1.

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

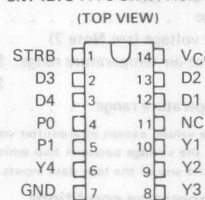
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{max} Maximum clock frequency		25	80		kHz
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15pF$		15	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	$C_L = 400pF$		18	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Note 2		15	20	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			20	30	ns

NOTE 2: See General Information Section for load circuit and voltage waveform.

3 TTL DEVICES

MAY 1972 - REVISED APRIL 1985

- SN54278 . . . J OR W PACKAGE
SN74278 . . . J OR N PACKAGE



NC—No internal connection

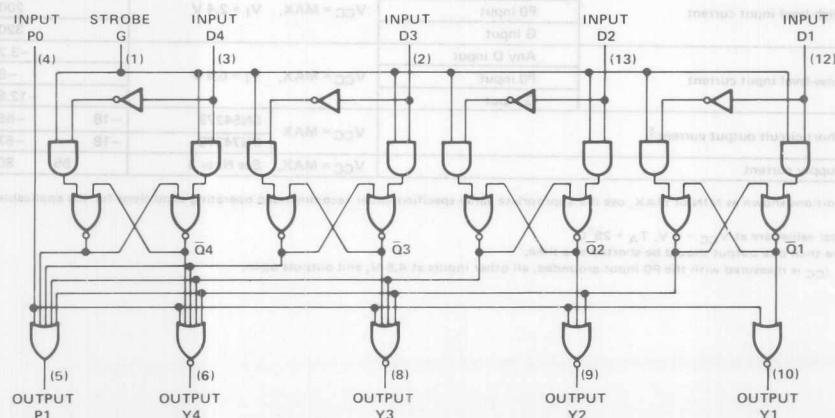
description

After the overriding P0 input, the order of priority is D1, D2, D3, and D4, respectively, within the package.

FUNCTION TABLE													
INPUTS						INTERNAL LATCH NODES				OUTPUTS			
P0	G	D1	D2	D3	D4	Q1	Q2	Q3	Q4	Y1	Y2	Y3	Y4
L	H	H	X	X	X	L	X	X	X	H	L	L	L
L	H	L	H	X	X	H	L	X	X	L	H	L	L
L	H	L	L	H	X	H	H	L	X	L	L	H	L
L	H	L	L	L	H	H	H	H	L	L	L	L	H
L	H	L	L	L	L	H	H	H	H	L	L	L	L
L	L	X	X	X	X	Latched when G goes low				Same function of nodes as on 1st 5 lines			
H	L	X	X	X	X					L	L	L	L
H	H	Internal Q levels are same function of D inputs as on first 5 lines								L	L	L	L

H = high level, L = low level, X = irrelevant

logic diagram



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TEXAS
INSTRUMENTS

TYPES SN54278, SN74278

4-BIT CASCADABLE PRIORITY REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54278 Circuits	-55°C to 125°C
SN74278 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the strobe input and any of the four data inputs.

recommended operating conditions

	SN54278			SN74278			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Data setup time, t_{SU} (see Figure 1)	20			20			ns
Data hold time, t_H (see Figure 1)	5			5			ns
Strobe pulse width, t_W (see Figure 1)	20			20			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	Any D input			80	μ A
		P0 input			200	μ A
		G input			320	μ A
I_{IL}	Low-level input current	Any D input			-3.2	mA
		P0 input			-8	mA
		G input			-12.8	mA
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54278	-18	-55	mA
			SN74278	-18	-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3		55	80	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the P0 input grounded, all other inputs at 4.5 V, and outputs open.

3

TTL DEVICES

TYPES SN54278, SN74278 4-BIT CASCADABLE PRIORITY REGISTERS

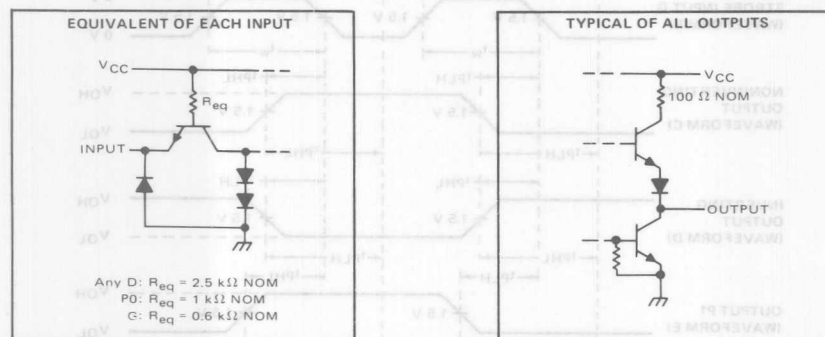
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	WAVEFORMS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	Data	Y	A and C (with strobe high)	C _L = 15 pF, R _L = 400 Ω, See Figure 1			30	ns
^t PHL							39	
^t PLH	Data	Y	A and D (with strobe high)				38	ns
^t PHL							31	
^t PLH	Data	P1	A and E (with strobe high)				46	ns
^t PHL							39	
^t PLH	Strobe	Any Y	B and C or B and D				30	ns
^t PHL							31	
^t PLH	Strobe	P1	B and E				38	ns
^t PHL							42	
^t PLH	P0	P1	F and G				23	ns
^t PHL							30	

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

schematics of inputs and outputs

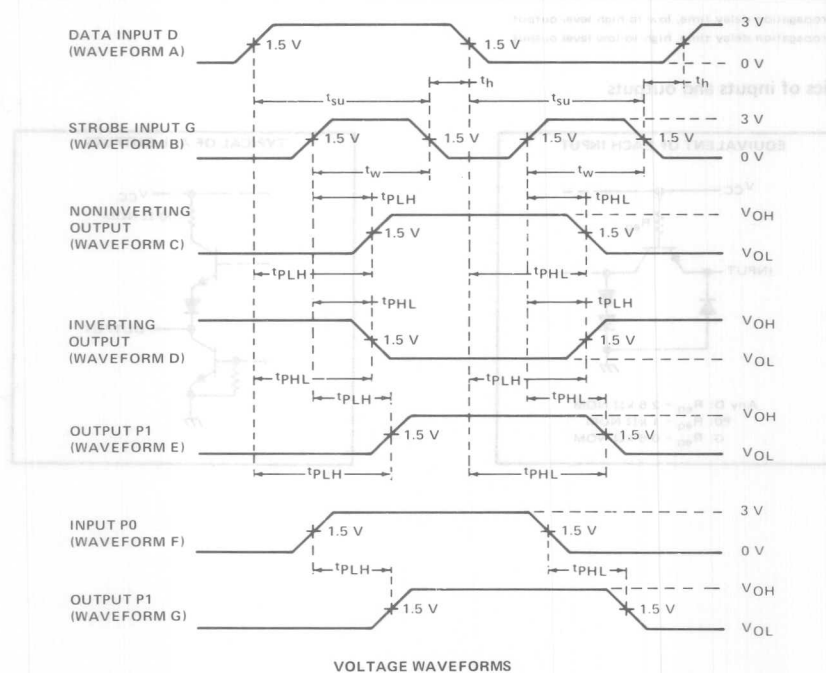
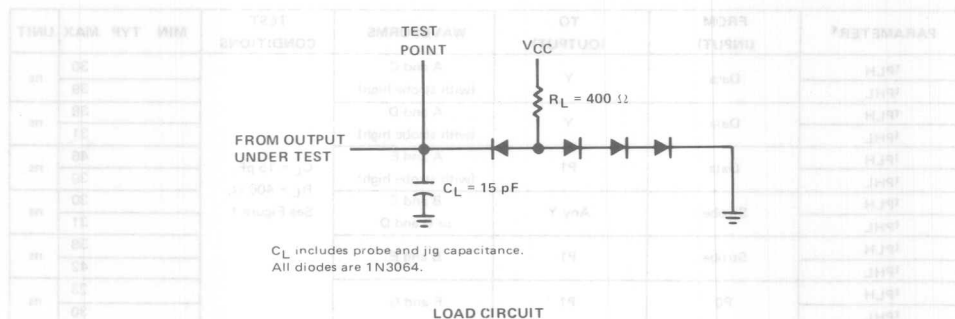


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TTL DEVICES

TYPES SN54278, SN74278 4-BIT CASCADABLE PRIORITY REGISTERS

PARAMETER MEASUREMENT INFORMATION



NOTE: Input pulses are supplied by a generator having the following characteristics: $t_r \leq 7 \text{ ns}$, $t_f \leq 7 \text{ ns}$, $\text{PRR} \leq \text{MHz}$, $Z_{\text{out}} \approx 50 \Omega$.

FIGURE 1—SWITCHING TIMES

3

TTL DEVICES

TYPES SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

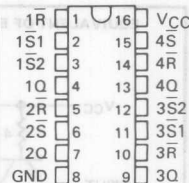
REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

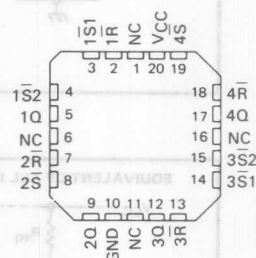
SN54279, SN54LS279A ... J OR W PACKAGE
SN74279 ... J OR N PACKAGE
SN74LS279A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS279A ... FK PACKAGE
SN74LS279A

(TOP VIEW)



NC - No internal connection

description

The '279 offers 4 basic S-R flip-flop latches in one 16-pin, 300-mil package. Under conventional operation, the S-R inputs are normally held high. When the S input is pulsed low, the Q output will be set high. When R is pulsed low, the Q output will be reset low. Normally, the S-R inputs should not be taken low simultaneously. The Q output will be unpredictable in this condition.

FUNCTION TABLE
(each latch)

INPUTS		OUTPUT
S†	R	Q
H	H	Q ₀
L	H	H
H	L	L
L	L	H*

H = high level

L = low level

Q₀ = the level of Q before the indicated input conditions were established.

*This configuration is nonstable: that is, it may not persist when the S and R inputs return to their inactive (high) level.

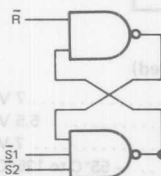
† For latches with double S inputs:

H = both S inputs high

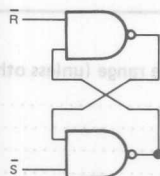
L = one or both S inputs low

logic diagram

(latches 1 and 3)



(latches 2 and 4)



PRODUCTION DATA

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TEXAS
INSTRUMENTS

3-769

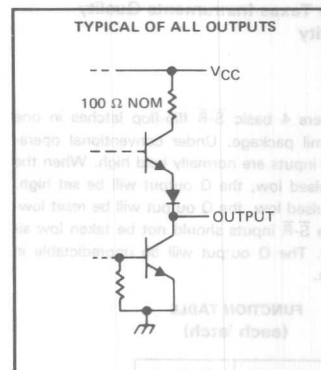
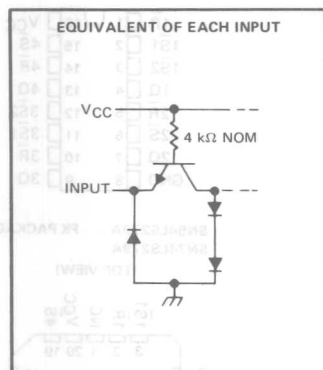
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TTL DEVICES

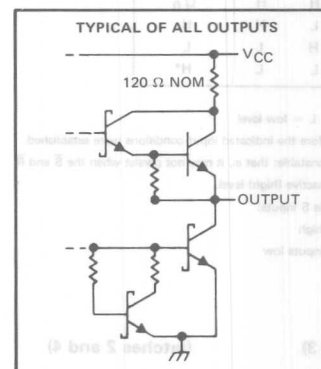
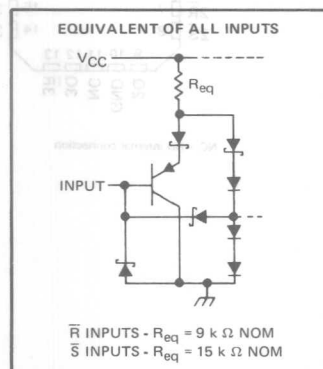
TYPES SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE \bar{S} -R LATCHES

schematics of inputs and outputs

'279 CIRCUITS



'LS279A CIRCUITS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '279	5.5 V
'LS279A	7 V
Operating free-air temperature range: SN54' TYPES	-55° C to 125° C
SN74' TYPES	0° C to 70° C
Storage temperature range	-65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54279, SN74279 QUADRUPLE S-R LATCHES

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54279			SN74279			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.8			-0.8	mA
I_{OL}	Low-level output current			16			16	mA
t_W	Pulse duration, low	20			20			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54279			SN74279			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.8 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-18		-55	-18		-57	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		18	30		18	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all R inputs grounded, all S inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	S	Q	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		12	22	ns
t_{PHL}	S	Q			9	15	ns
t_{PHL}	R	Q			15	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS279A, SN74LS279A QUADRUPLE S-R LATCHES

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS279A			SN74LS279A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
t _W	Pulse duration, low	20			20			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS279A			SN74LS279A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.25	0.5	V
I _I	V _{CC} = MAX, V _I = 7 V		0.1				0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.2			-0.2		mA
I _{OS} §	V _{CC} = MAX	-20		100	-20		100	mA
I _{CC}	V _{CC} = MAX, See note 2		3.8	7		3.8	7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should be less than one second.

NOTE 2: I_{CC} is measured with all R inputs grounded, all S inputs at 4.5 V, and all outputs open.

3

TTL DEVICES

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	S	Q	R _L = 2 kΩ, C _L = 15 pF		12	22	ns
t _{PHL}	S	Q			13	21	ns
t _{PHL}	R	Q			15	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

DECEMBER 1972—REVISED DECEMBER 1983

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:
'LS280 . . . 80 mW
'S280 . . . 335 mW

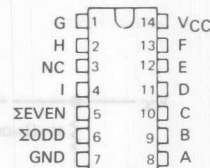
FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

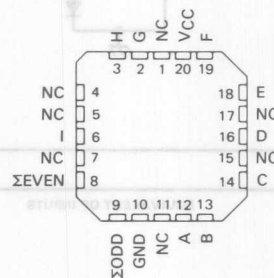
SN54LS280, SN54S280 . . . J OR W PACKAGE
SN74LS280, SN74S280 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS280, SN54S280 . . . FK PACKAGE
SN74LS280, SN74S280

(TOP VIEW)



NC - No internal connection

description

These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade-off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

These devices are fully compatible with most other TTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

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TTL DEVICES

PRODUCTION DATA

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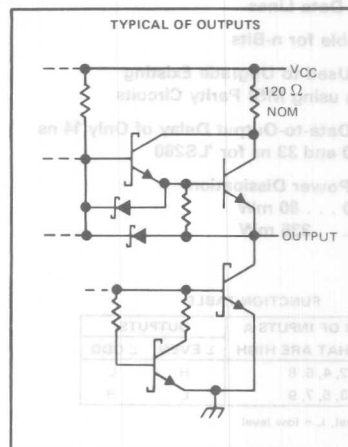
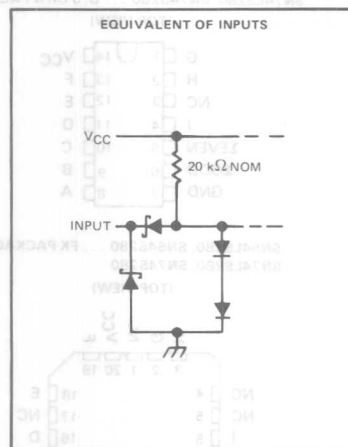
TEXAS
INSTRUMENTS

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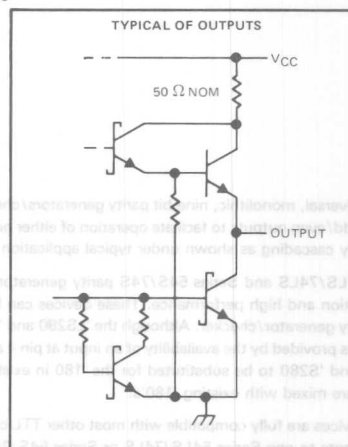
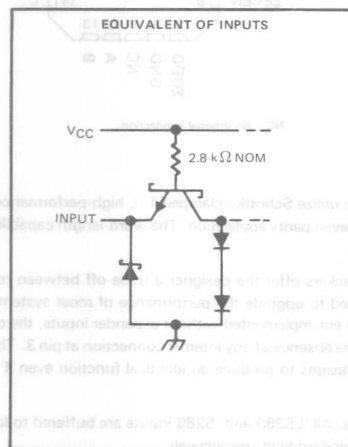
TYPES SN54S280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

schematics of inputs and outputs

'LS280



'S280



3

TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: 'LS280	7 V
'S280	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS280, SN74LS280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

recommended operating conditions

	SN54LS280			SN74LS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-0.4			-0.4	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LS280			SN74LS280			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 4 mA, I _{OL} = 8 mA	0.25	0.4		0.25	0.4		V
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20		μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
I _{OS} [§]	V _{CC} = MAX	-20	-100		-20	-100		mA
I _{CC}	V _{CC} = MAX, See Note 2		16	27		16	27	mA

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	≥ Even	C _L = 15 pF, R _L = 2 kΩ, Inputs not under test at 0 V, See Note 3	33	50		ns
t _{PHL}				29	45		ns
t _{PLH}	Data	≥ Odd	See Note 3	23	35		ns
t _{PHL}				31	50		ns

[¶] t_{PLH} propagation delay time, low-to-high-level output; t_{PHL} propagation delay time, high to low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54S280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

recommended operating conditions

	SN54S280			SN74S280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$ SN54S [‡] SN74S [‡]	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	SN54S280	67	99	mA
		SN74S280	67	105	
	$V_{CC} = \text{MAX}, T_A = 125^\circ \text{C}$, See Note 2	SN54S280N		94	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Data	Σ Even	CL = 15 pF. RL = 280 Ω, See Note 3	14	21		ns
tPHL				11.5	18		
tPLH	Data	Σ Odd		14	21		ns
tPHL					11.5	18	

¶ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

ITL DEVICES

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TTL DEVICES

TYPICAL APPLICATION DATA

81-LINE PARITY/GENERATOR CHECKER

Longer word lengths can be implemented by cascading 'LS280's or 'S280's. As shown here, parity can be generated for word lengths up to 81 bits in typically 75 or 25 nano seconds respectively.

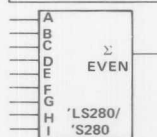
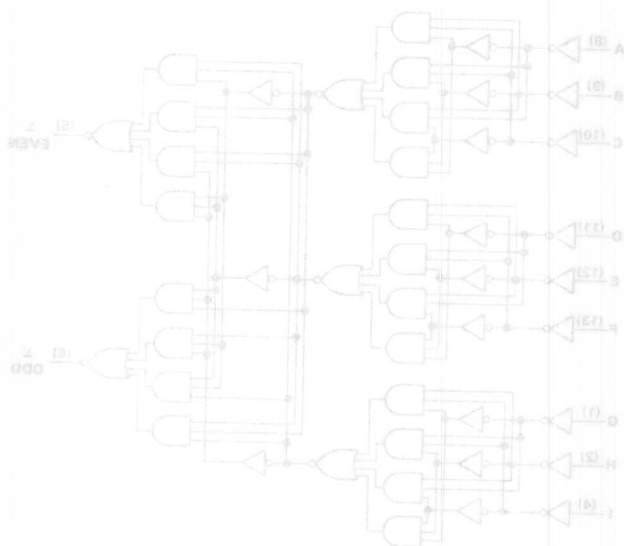


Diagram showing the connection of the 'EVEN' pin to the 'TO OTHER' pins of the 'LS280/S280' devices.

logic diagram

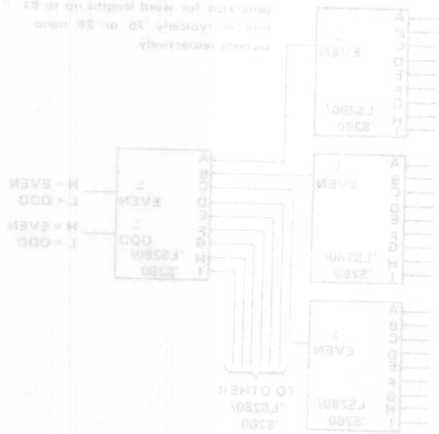


Pin numbers shown on logic diagram are for D, L or H packages.

TYPICAL APPLICATION DATA

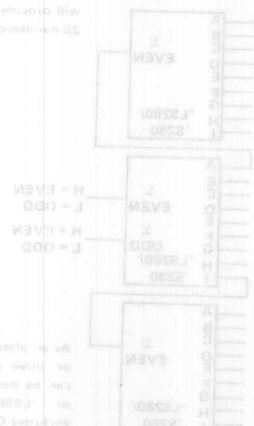
9-BIT PARITY/GENERATOR CHECKER

Longer word lengths can be made by cascading L2380's or L2380's. At present, parity can be generated for word lengths up to 91 bits in typically 75 or 50 nsec, depending respectively.



22-BIT PARITY/GENERATOR CHECKER

Types L2380 or L2380's can be used to implement a 22-bit parity generator/checker. This arrangement will produce parity in typically 75 or 50 nsec, depending respectively.



As an alternative, the outputs of two 9-bit parity generator/checkers can be decoded with a 3-input L2380 or L2380 or 3-input L2380 to produce OR data for 16 or 32 bits.

TYPES SN54283, SN54LS283, SN54S283, SN74283, SN74LS283, SN74S283 4-BIT BINARY FULL ADDERS WITH FAST CARRY

OCTOBER 1976—REVISED DECEMBER 1983

- Full-Carry Look-Ahead Across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

TYPICAL ADD TIMES

TYPE	TWO		TYPICAL POWER DISSIPATION PER ADDER
	8-BIT WORDS	16-BIT WORDS	

'283	23ns	43ns	310 mW
'LS283	25ns	45ns	95 mW
'S283	15ns	30ns	510 mW

description

The '283 and 'LS283 adders are electrically and functionally identical to the '83A and 'LS283, respectively; only the arrangement of the terminals has been changed. The 'S283, high performance versions are also functionally identical.

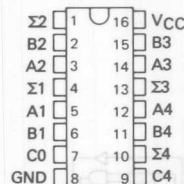
These improved full adders perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds, typically, for the '283 and 'LS283, and 7.5 nanoseconds for the 'S283. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full temperature range of -55°C to 125°C . Series 74, Series 74LS, and Series 74S circuits are characterized for 0°C to 70°C operation.

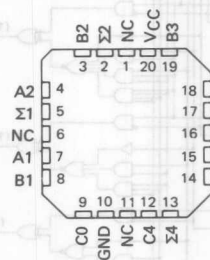
SN54283, SN54LS283 ... J OR W PACKAGE
SN54S283 ... J PACKAGE
SN74283 ... J OR N PACKAGE
SN74LS283, SN74S283 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS283, SN54S283 ... FK PACKAGE
SN74LS283, SN74S283

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUT				OUTPUT							
				WHEN C0 = L				WHEN C0 = H			
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2	Σ1	Σ2
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4	Σ3	Σ4
L	L	L	L	L	L	L	H	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L
H	H	L	L	L	H	L	H	H	L	L	L
L	L	H	L	L	H	L	H	H	L	L	L
H	L	H	L	H	H	L	L	L	L	L	H
L	H	H	L	H	H	L	L	L	L	L	H
H	H	H	L	L	L	H	H	H	L	L	H
L	L	L	H	L	H	L	H	L	H	L	H
H	L	L	H	H	H	L	L	L	L	L	H
L	L	H	H	L	L	H	H	L	L	L	H
H	L	H	H	H	L	H	L	L	L	L	H
L	H	H	H	H	L	H	L	L	L	L	H
H	H	H	H	L	H	H	H	H	L	L	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma 3$, $\Sigma 4$, and C4.

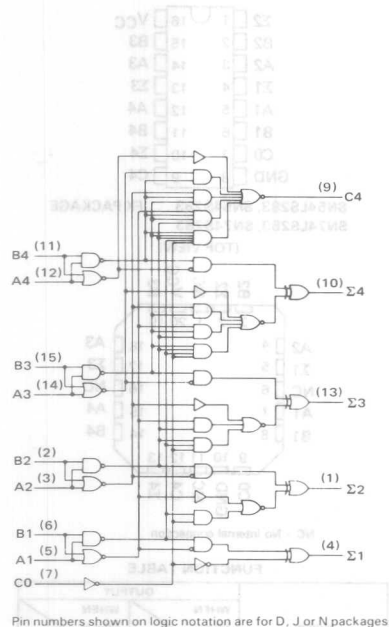
PRODUCTION DATA

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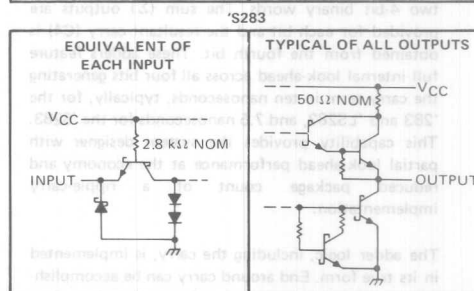
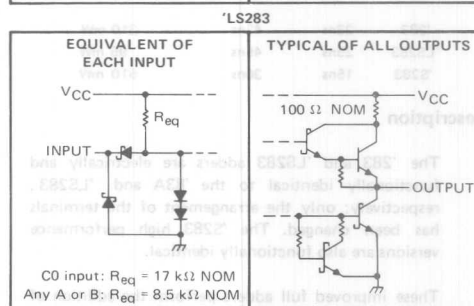
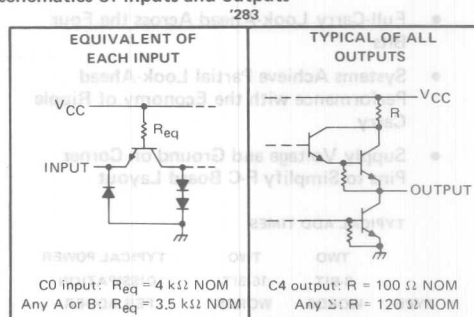
TEXAS
INSTRUMENTS

**TYPES SN54283, SN54LS283, SN54S283,
SN74283, SN74LS283, SN74S283
4-BIT BINARY FULL ADDERS WITH FAST CARRY**

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7V
Input voltage: '283, 'S283	5.5V
'LS283	7V
Interemitter voltage (see Note 2)	5.5V
Operating free-air temperature range: SN54283, SN54LS283, SN54S283	-55°C to 125°C
SN74283, SN74LS283, SN74S283	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple emitter transistor. This rating applies for the '283 and 'S283 only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

8852 TYPES SN54283, SN74283 4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

		SN54283			SN74283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			-800			-800	μ A
	Output C4			-400			400	
Low-level output current, I_{OL}	Any output except C4			16			16	mA
	Output C4			8			8	
Operating free-air temperature, T_A		-55		125	0		70	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54283			SN74283			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = \text{MAX}$		2.4	3.6		2.4	3.6		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = \text{MAX}$			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1		mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40		μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6		mA
I_{OS}	Short-circuit output current §	Any output except C4	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
		Output C4		-20		-70	-18		-70	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, Outputs open	All B low, other inputs at 4.5 V		56			56		mA
			All inputs at 4.5 V		66	99		66	110	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 3		14	21	ns
t_{PHL}					12	21	
t_{PLH}	A_i or B_i	Σ_i			16	24	ns
t_{PHL}					16	24	
t_{PLH}	C0	C4	$C_L = 15 \text{ pF}$, $R_L = 780 \Omega$, See Note 3		9	14	ns
t_{PHL}					11	16	
t_{PLH}	A_i or B_i	C4			9	14	ns
t_{PHL}					11	16	

¶ t_{PLH} Propagation delay time, low to high level output

t_{PHL} Propagation delay time, high to low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS283, SN74LS283 4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

	SN54LS283			SN74LS283			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS283			SN74LS283			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage			0.7			0.8		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5			-1.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$ $V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I	Input current	Any A or B		0.2			0.2		mA
	at maximum input voltage	C_0		0.1			0.1		
I_{IH}	High-level input current	Any A or B		40			40		μ A
		C_0		20			20		
I_{IL}	Low-level input current	Any A or B		-0.8			-0.8		mA
		C_0		-0.4			-0.4		
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100	-20	-20	-100		mA
I_{CC}	Supply current	All inputs grounded	22	39		22	39		mA
		All B low, other inputs at 4.5 V	19	34		19	34		
		All inputs at 4.5 V	19	34		19	34		

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§]Only one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	C ₀	Any Σ	C _L = 15 pF, See Note 3	R _L = 2 kΩ _i	16	24	ns	
t _{PHL}					15	24		
t _{PLH}	A _i or B _i	Σ _i			15	24	ns	
t _{PHL}					15	24		
t _{PLH}	C ₀	C ₄			11	17	ns	
t _{PHL}					11	22		
t _{PLH}	A _i or B _i	C ₄			11	17	ns	
t _{PHL}					12	17		

[¶] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54S283, SN74S283 4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

		SN54S283			SN74S283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			-1			-1	mA
	Output C4			-500			-500	μ A
Low-level output current, I_{OL}	Any output except C4			20			20	mA
	Output C4			10			10	mA
Operating free-air temperature, T_A		-55			0			$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA				-1.2	V
V _{OH}	High-level output voltage	SN54S283	V _{CC} = MIN, V _{IH} = 2 V,		2.5	3.4		V
		SN74S283	V _{IL} = 0.8 V, I _{OH} = MAX		2.7	3.4		
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX				0.5	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 5.5 V				1	mA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V				50	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5 V				-2	mA
I _{OS}	Short-circuit output current§	Any output except C4	V _{CC} = MAX		-40		-100	mA
		Output C4			-20		-100	
I _{CC}	Supply current	V _{CC} = MAX, Outputs open		All B low, other inputs at 4.5 V		80		mA
				All inputs at 4.5 V		95	160	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 3		11	18	ns
t_{PHL}					12	18	
t_{PLH}	A_i or B_i	Σ_i	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 3		12	18	ns
t_{PHL}					11.5	18	
t_{PLH}	C0	C4	$C_L = 15 \text{ pF}, R_L = 560 \Omega,$ See Note 3		6	11	ns
t_{PHL}					7.5	11	
t_{PLH}	A_i or B_i	C4	$C_L = 15 \text{ pF}, R_L = 560 \Omega,$ See Note 3		7.5	12	ns
t_{PHL}					8.5	12	

† t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

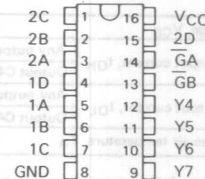
TYPES SN54284, SN54285, SN74284, SN74285 4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

MAY 1972 - REVISED DECEMBER 1983

- Fast Multiplication of Two Binary Numbers
8-Bit Product in 40 ns Typical
- Expandable for N-Bit-by-n-Bit Applications:
16-Bit Product in 70 ns Typical
32-Bit Product in 103 ns Typical
- Fully Compatible with Most TTL Circuits
- Diode-Clamped Inputs Simplify System Design

SN54284 ... J OR W PACKAGE
SN74284 ... J OR N PACKAGE

(TOP VIEW)



description

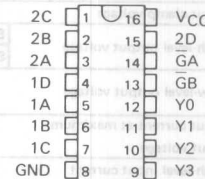
These high-speed TTL circuits are designed to be used in high-performance parallel multiplication applications. When connected as shown in Figure A, these circuits perform the positive-logic multiplication of two 4-bit binary words. The eight-bit binary product is generated with typically only 40 nanoseconds delay.

This basic four-by-four multiplier can be utilized as a fundamental building block for implementing larger multipliers. For example, the four-by-four building blocks can be connected as shown in Figure B to generate submultiple partial products. These results can then be summed in a Wallace tree, and, as illustrated, will produce a 16-bit product for the two eight-bit words typically in 70 nanoseconds. SN54H183/SN74H183 carry-save adders and SN54S181/SN74S181 arithmetic logic units with the SN54S182/SN74S182 look-ahead generator are used to achieve this high performance. The scheme is expandable for implementing N X M bit multipliers.

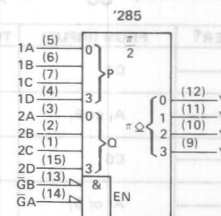
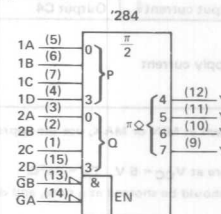
The SN54284 and SN54285 are characterized for operation over the full military temperature range of -55°C to 125°C; the SN74284 and SN74285 are characterized for operation from 0°C to 70°C.

SN54285 ... J OR W PACKAGE
SN74285 ... J OR N PACKAGE

(TOP VIEW)



logic symbols



Pin numbers shown are
for J and N packages.

3 TTL DEVICES

UNIT	MIN	TYP	MAX	TEST CONDITIONS	TO OUTPUT
m	18	17	18	$C_L = 15 \text{ pF}$, $R_L = 100 \Omega$ See Note 3	Any Z
	12	12	12		
	18	18	18		
	18	18	18		
m	12	12	12	$C_L = 15 \text{ pF}$, $R_L = 100 \Omega$ See Note 3	Z
	18	18	18		
	18	18	18		
	18	18	18		
m	12	12	12	$C_L = 15 \text{ pF}$, $R_L = 100 \Omega$ See Note 3	Z
	18	18	18		
	18	18	18		
	18	18	18		
m	12	12	12	$C_L = 15 \text{ pF}$, $R_L = 100 \Omega$ See Note 3	Z
	18	18	18		
	18	18	18		
	18	18	18		

PRODUCTION DATA

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3-784

TEXAS
INSTRUMENTS

TYPES SN54284, SN54285, SN74284, SN74285 4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

schematics

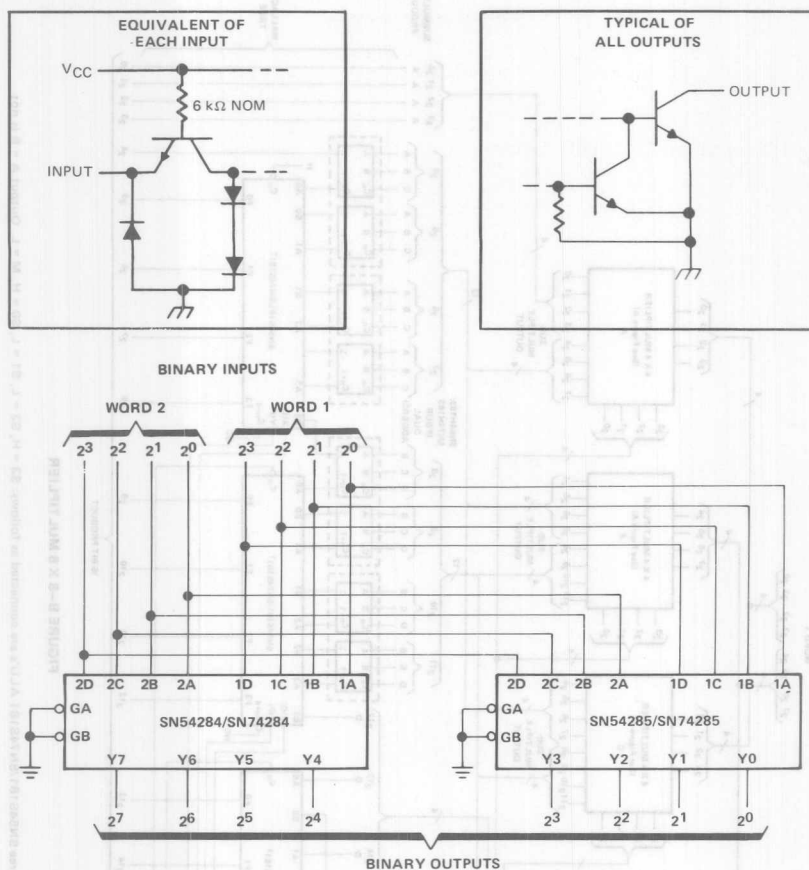


FIGURE A-4 X 4 MULTIPLIER

3

TTL DEVICES



[†]Other terminals of the three SN54S181/SN74S181 ALU's are connected as follows: S3 = H, S2 = L, S1 = L, S0 = H, M = L. Output A = B is not used for this application.

TYPES SN54284, SN54285, SN74284, SN74285 4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54 [†] Circuits	−55°C to 125°C
SN74 [†] Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54284 SN54285			SN74284 SN74285			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			−1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 5.5 \text{ V}$			40	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	$I_{OL} = 12 \text{ mA}$		0.4	V
		$I_{OL} = 16 \text{ mA}$		0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			−1	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, $T_A = 125^\circ\text{C}$, See Note 2	SN54284, SN54285 N package only		99	mA
	$V_{CC} = \text{MAX}$, See Note 2	SN54284, SN54285		92 110	
		SN74284, SN74285		92 130	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: With outputs open and both enable inputs grounded, I_{CC} is measured first by selecting an output product which contains three or more high-level bits, then by selecting an output product which contains four low-level bits.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from enable	$C_L = 30 \text{ pF}$ to GND, $R_{L1} = 300 \Omega$ to V_{CC} , $R_{L2} = 600 \Omega$ to GND, See Note 3	20	30		ns
t_{PHL} Propagation delay time, high-to-low-level output from enable				20 30	
t_{PLH} Propagation delay time, low-to-high-level output from word inputs		40	60		ns
t_{PHL} Propagation delay time, high-to-low-level output from word inputs				40 60	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

NOTE 3: See General Information Section for load circuit and voltage waveform.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output from weak drive	C _L = 30 pF to GND		30	50	ns
t _{PHL} Propagation delay time, high-to-low-level output from weak drive	R _L = 300 Ω to V _{CC}		30	50	ns
t _{PLH} Propagation delay time, low-to-high-level output from strong drive	R _L = 800 Ω to GND		40	50	ns
t _{PHL} Propagation delay time, high-to-low-level output from strong drive	See Note 1		40	50	ns

switching characteristics, V_{CC} = 5 V, T_A = 25°C

NOTE 2: With outputs open and both enable inputs grounded, t_{CC} is determined only by selecting an output buffer which contains drive or more high-level drive, then by selecting an output product which contains low-level drive.

T_A is typical values are at V_{CC} = 5 V, T_A = 25°C.

T_{PL} conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the appropriate device.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CC} Supply current	See Note 1 V _{CC} = MAX T _A = 25°C N package only	90	110	130	mA
I _{IL} Low-level input current	V _{CC} = MAX V _I = 0.4 V			-1	mA
I _{IH} High-level input current	V _{CC} = MAX V _I = 2.4 V			40	μA
I _I Input current at maximum input voltage	V _{CC} = MAX V _I = 2.4 V			40	μA
V _{OL} Low-level output voltage	V _{CC} = MAX V _I = 0.4 V I _{OL} = 10 mA			0.50	V
V _{OH} High-level output voltage	V _{CC} = MAX V _I = 0.4 V I _{OH} = 10 mA			0.4	V
V _I Input clamp voltage	V _{CC} = MIN V _{OH} = 2.4 V			40	μA
V _{IL} Low-level input voltage	V _{CC} = MIN I _I = 11 mA			-1.5	V
V _{IH} High-level input voltage	V _{CC} = MIN I _I = 11 mA			0.9	V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating free-air temperature, T _A		-55	0	125	°C
Low-level output current, I _{OL}				18	mA
High-level output voltage, V _{OH}				0.9	V
Supply voltage, V _{CC}				4.5	V

recommended operating conditions

NOTE 1: Voltage values are with respect to network ground terminal.

Storage temperature range:

55°C to 180°C

Operating free-air temperature range:

55°C to 125°C

Supply voltage, V_{CC} (see Note 1)

Input voltage:

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

4-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS
TYPES SN54284, SN54285, SN74284, SN74285

TYPES SN54290, SN54293, SN54LS290, SN54LS293, SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

MARCH 1974—REVISED DECEMBER 1983

'290, 'LS290 ... DECADE COUNTERS '293, 'LS293 ... 4-BIT BINARY COUNTERS

- GND and V_{CC} on Corner Pins
(Pins 7 and 14 Respectively)

description

The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

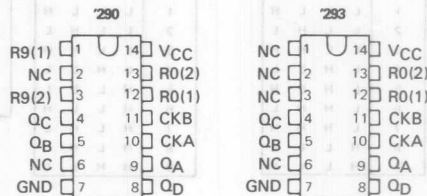
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

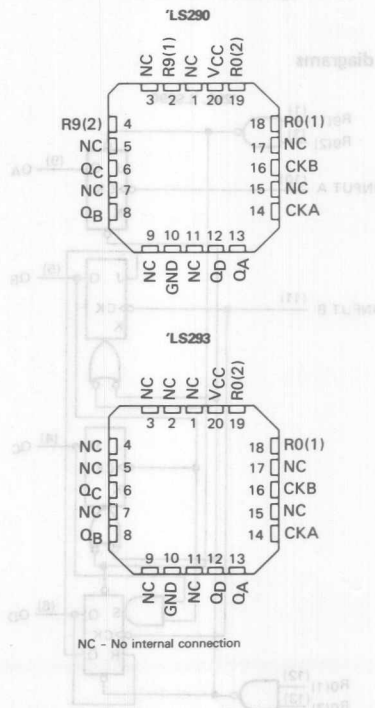
SN54290, SN54LS290, SN54293,
SN54LS293 ... J OR W PACKAGE
SN74290, SN74293 ... J OR N PACKAGE
SN74LS290, SN74LS293 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS290, SN54LS293 ... FK PACKAGE
SN74LS290, SN74LS293

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-789

TYPES SN54290, SN54293, SN54LS290, SN54LS293, SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

'290, 'LS290
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'290, 'LS290
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'290, 'LS290
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'293, 'LS293
COUNT SEQUENCE
(See Note C)

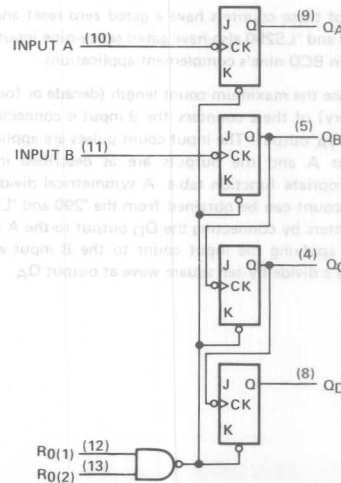
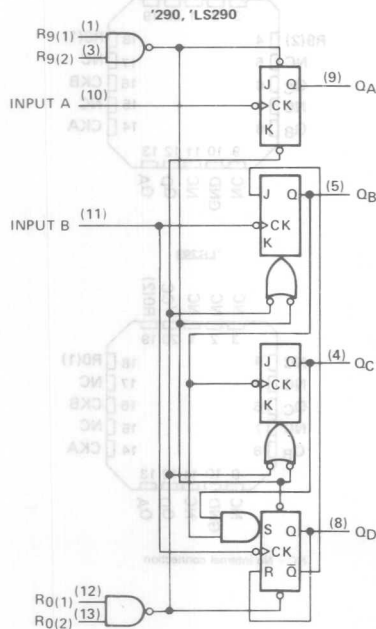
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

'293, 'LS293
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

logic diagrams

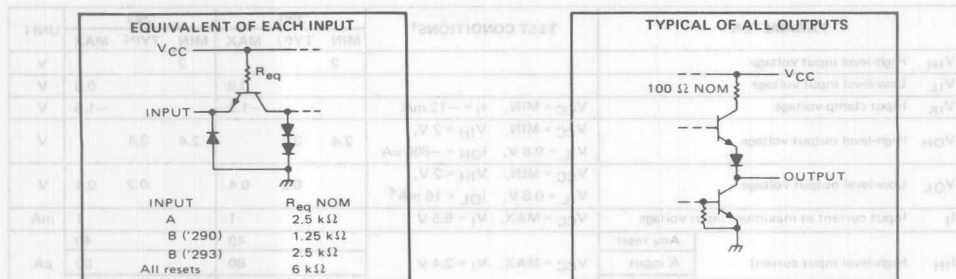


Pin numbers shown on logic notation are for D, J or N packages.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

TYPES SN54290, SN54293, SN74290, SN74293 DECADE AND 4-BIT BINARY COUNTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54' Circuits	-55°C to 125°C
SN74' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_9 inputs, and for the '290 circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN54'			SN74'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
	Reset inputs	15		15	15		15	
Pulse width, t_w		15		30	15		30	ns
Reset inactive-state setup time, t_{su}		25		25	25		25	ns
Operating free-air temperature, T_A		-55		125	0		70	°C

3

TTL DEVICES

TYPES SN54290, SN54293, SN74290, SN74293 DECADE AND 4-BIT BINARY COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'290			'293			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}^{\S}$	0.2	0.4		0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1			1		mA
I_{IH} High-level input current	Any reset		40			40		μA
	A input		80			80		
	B input		120			80		
I_{IL} Low-level input current	Any reset		-1.6			-1.6		mA
	A input		-3.2			-3.2		
	B input		-4.8			-3.2		
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54* -20	-57	-20	-57			mA
		SN74* -18	-57	-18	-57			
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 3	29	42		26	39		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

¶ QA outputs are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 4	32	42		32	42		MHz
	B	Q_B		16			16			
t_{PLH}	A	Q_A		10	16		10	16		ns
t_{PHL}	A	Q_A		12	18		12	18		
t_{PLH}	A	Q_D		32	48		46	70		ns
t_{PHL}	A	Q_D		34	50		46	70		
t_{PLH}	B	Q_B		10	16		10	16		ns
t_{PHL}	B	Q_B		14	21		14	21		
t_{PLH}	B	Q_C		21	32		21	32		ns
t_{PHL}	B	Q_C		23	35		23	35		
t_{PLH}	B	Q_D		21	32		34	51		ns
t_{PHL}	B	Q_D		23	35		34	51		
t_{PHL}	Set-to-0	Any		26	40		26	40		ns
t_{PLH}	Set-to-9	Q_A, Q_D		20	30					ns
t_{PHL}	Set-to-9	Q_B, Q_C		26	40					

f_{max} maximum count frequency

t_{PLH} propagation delay time, low-to-high level output

t_{PHL} propagation delay time, high-to-low level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

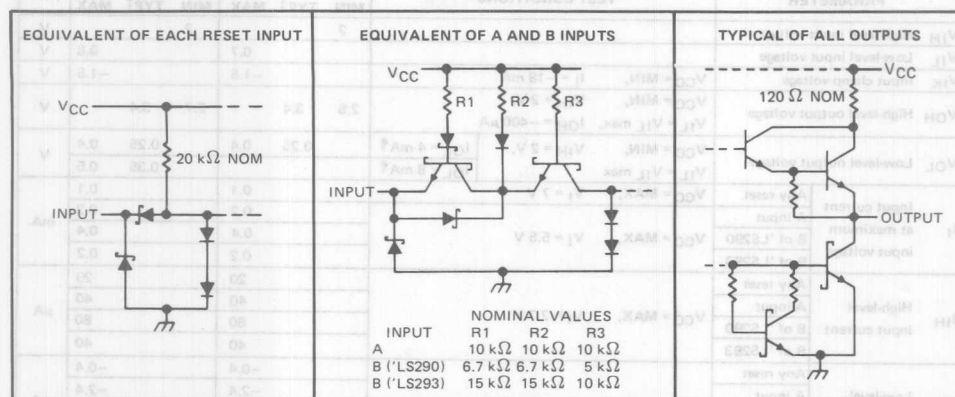
3

TTL DEVICES

TYPES SN54LS290, SN54LS293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

REVISED OCTOBER 1976

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 5)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293	-55°C to 125°C
SN74LS290, SN74LS293	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS*			SN74LS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
	Reset inputs	15		15				
Pulse width, t_w		30		30			30	ns
Reset inactive-state setup time, t_{su}		25		25			25	ns
Operating free-air temperature, T_A		-55		125	0		70	°C

3

TTL DEVICES

TYPES SN54LS290, SN54LS293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.7			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max							V
I _I Input current at maximum input voltage	Any reset							mA
	A input			0.1			0.1	
	B of 'LS290			0.2			0.2	
	B of 'LS293			0.4			0.4	
I _{IH} High-level input current	Any reset							µA
	A input			20			20	
	B of 'LS290			40			40	
	B of 'LS293			80			80	
I _{IL} Low-level input current	Any reset							mA
	A input			-0.4			-0.4	
	B of 'LS290			-2.4			-2.4	
	B of 'LS293			-3.2			-3.2	
I _{OS} Short-circuit output current§	V _{CC} = MAX	-20	-100		-20	-100		mA
I _{CC} Supply current	V _{CC} = MAX, See Note 3	'LS290	9	15	'LS290	9	15	mA
		'LS293	9	15	'LS293	9	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS290			'LS293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 0F, R _L = 2 kΩ, See Note 4	32	42		32	42		MHz
	B	Q _B		16			16			
t _{PLH}	A	Q _A			10	16		10	16	ns
t _{PHL}	A	Q _A			12	18		12	18	ns
t _{PLH}	A	Q _D			32	48		46	70	ns
t _{PHL}	A	Q _D			34	50		46	70	ns
t _{PLH}	B	Q _B			10	16		10	16	ns
t _{PHL}	B	Q _B			14	21		14	21	ns
t _{PLH}	B	Q _C			21	32		21	32	ns
t _{PHL}	B	Q _C			23	35		23	35	ns
t _{PLH}	B	Q _D			21	32		34	51	ns
t _{PHL}	B	Q _D			23	35		34	51	ns
t _{PLH}	Set-to-0	Any			26	40		26	40	ns
t _{PHL}	Set-to-9	Q _A , Q _D			20	30				ns
t _{PHL}	Set-to-9	Q _B , Q _C			26	40				ns

◇ f_{max} = maximum count frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

D2628, JANUARY 1981—REVISED DECEMBER 1983

- Count Divider Chain
- Digitally Programmable from 2^2 to 2^n
($n = 31$ for 'LS292, $n = 15$ for 'LS294)
- Useable Frequency Range from DC to 30 MHz
- Easily Expandable
- Applications
 - Frequency Division
 - Digital Timing

description

These programmable frequency dividers/digital timers contain 31 flip-flops plus 30 gates ('LS292) or 15 flip-flops plus 29 gates ('LS294) on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'LS292 and TP on the 'LS294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the function table below.)

A brief look at the digital timing capabilities of the 'LS292 will show that with a 1-MHz input frequency, programming for 2^{10} will give a period of 1.024 ms, and 2^{20} will give a period of 1.05 sec, 2^{26} will give a period of 1.12 min, and 2^{31} will give a period of 35.79 min.

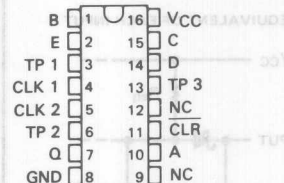
These devices are easily cascadable giving limitless possibilities to timing delays that can be achieved.

FUNCTION TABLE

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

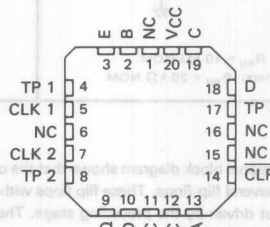
SN54LS292 ... J OR W PACKAGE
SN74LS292 ... J OR N PACKAGE

(TOP VIEW)



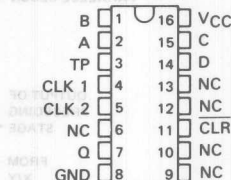
SN54LS292 ... FK PACKAGE
SN74LS292

(TOP VIEW)



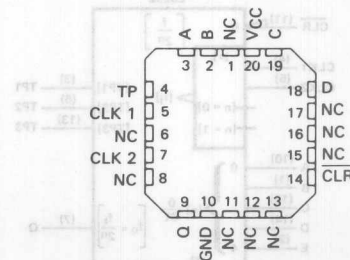
SN54LS294 ... J OR W PACKAGE
SN74LS294 ... J OR N PACKAGE

(TOP VIEW)



SN54LS294 ... FK PACKAGE
SN74LS294

(TOP VIEW)



NC — No internal connection.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

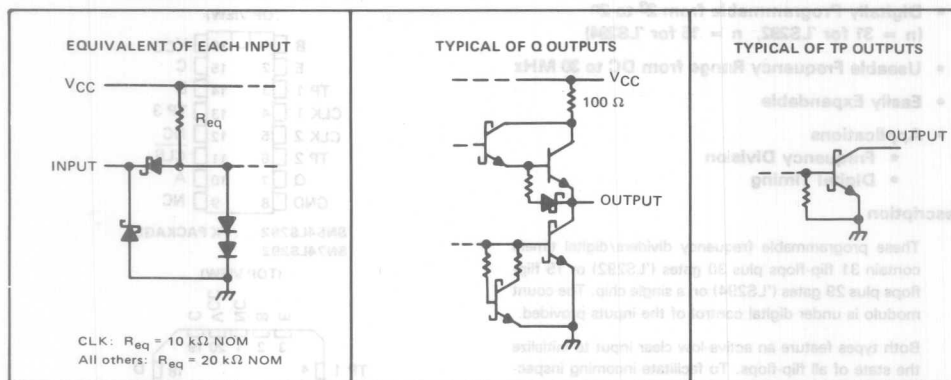
TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

schematics of inputs and outputs



operation

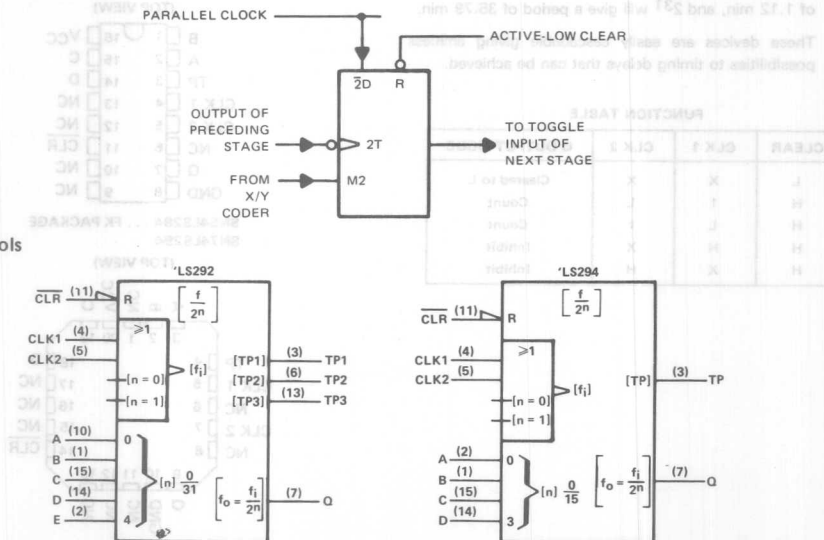
The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode control inputs of several flip-flops. These flip-flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of that flip-flop is enabled, and the signal from the parallel clock line ($f_{in} \div 4$) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.

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TTL DEVICES

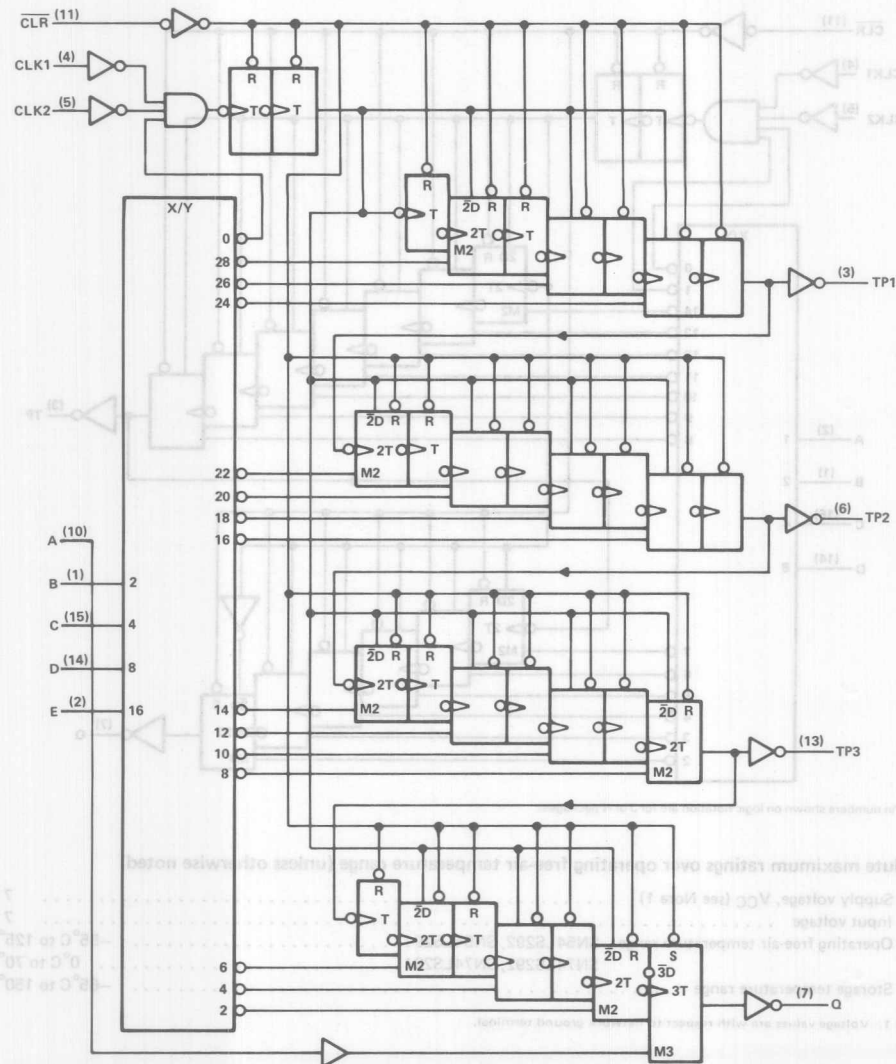
logic symbols



TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

logic diagram (positive logic)

'LS292



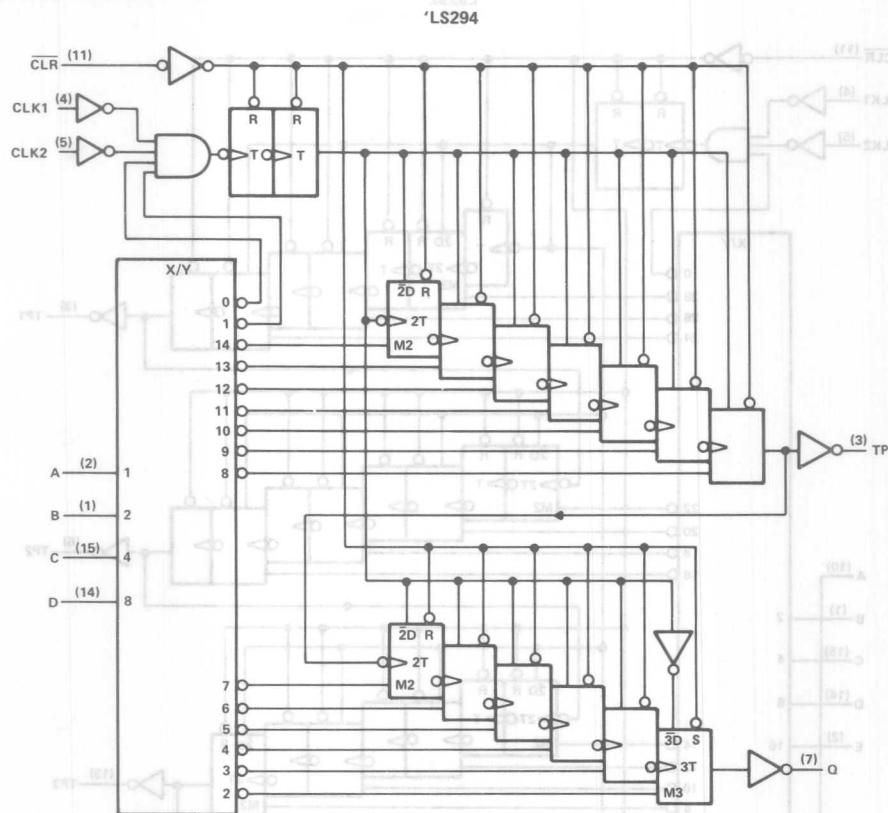
Pin numbers shown on logic notation are for J or N packages.

3

TTL DEVICES

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

logic diagram (positive logic)



Pin numbers shown on logic notation are for J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS292, SN54LS294	-55°C to 125°C
SN74LS292, SN74LS294	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

recommended operating conditions

SYMBOL	TEST CONDITIONS	SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current (Q only)			-1.2			-1.2	mA
I _{OL}	Low-level output current (Q only)			12			24	mA
f _{clock}	Clock frequency	0		30	0		30	MHz
t _w	Duration of clock input pulse	16			16			ns
t _w	Duration of clear pulse		'LS292	55		55		ns
			'LS294	35		35		
t _{su}	Clear inactive-state setup time	15			15			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IK}		V _{CC} = MIN., I _I = -18 mA		-1.5			-1.5			V
V _{OH}	Q	V _{CC} = MIN., V _{IH} = 2 V, I _{OH} = -1.2 mA, V _{IL} = MAX		2.4	3.4		2.4	3.4		V
V _{OL}	Q	V _{CC} = MIN., V _{IH} = 2 V, V _{IL} = MAX			0.25	0.4	0.25	0.4		V
							0.35	0.5		
	TP◆						0.25	0.4		
I _I		V _{CC} = MAX., V _I = 7 V		0.1			0.1			mA
I _{IH}		V _{CC} = MAX., V _I = 2.7 V		20			20			μA
I _{IL}	CLK1, CLK2	V _{CC} = MAX., V _I = 0.4 V		-0.8			-0.8			mA
	All others			-0.4			-0.4			
I _{OS} §		V _{CC} = MAX		-30		-130	-30		-130	mA
I _{CC}	LS292	V _{CC} = MAX., All inputs grounded,			40	75		40	75	mA
	LS294	All outputs open			30	50		30	50	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ The duration of the short-circuit should not exceed one second.

◆ The TP output or outputs are not intended to drive external loads but are solely provided for test points.

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS292			'LS294			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}				30	50		30	50		MHz
t_{PLH}	CLK1 or 2	Q	Modulo set at 22, A thru E = LLLHL ('LS292) A thru D = LLHL ('LS294)	55	90		55	90		ns
t_{PHL}		Q		80	120		80	120		ns
t_{PHL}	CLR	Q		85	130		35	65		ns

f_{MAX} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 2: See General Information Section for load circuits and voltage waveforms.

To be used on TP outputs only.

'LS292 FUNCTION TABLE

PROGRAMMING INPUTS					FREQUENCY DIVISION							
E	D	C	B	A	Q		TP1		TP2		TP3	
					BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2 ²	4	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	L	H	H	2 ³	8	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	L	L	2 ⁴	16	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	L	H	2 ⁵	32	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	H	L	2 ⁶	64	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	L	H	H	H	2 ⁷	128	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L	H	L	L	L	2 ⁸	256	2 ⁹	512	2 ¹⁷	131,072	2 ²²	4
L	H	L	L	H	2 ⁹	512	2 ⁹	512	2 ¹⁷	131,072	2 ²²	4
L	H	L	H	L	2 ¹⁰	1,024	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16
L	H	L	H	H	2 ¹¹	2,048	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16
L	H	H	L	L	2 ¹²	4,096	2 ⁹	512	2 ¹⁷	131,072	2 ²⁶	64
L	H	H	L	H	2 ¹³	8,192	2 ⁹	512	2 ¹⁷	131,072	2 ²⁶	64
L	H	H	H	L	2 ¹⁴	16,384	2 ⁹	512	Disabled Low		2 ²⁸	256
L	H	H	H	H	2 ¹⁵	32,768	2 ⁹	512	Disabled Low		2 ²⁸	256
H	L	L	L	L	2 ¹⁶	65,536	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H	L	L	L	H	2 ¹⁷	131,072	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H	L	L	H	L	2 ¹⁸	262,144	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H	L	L	H	H	2 ¹⁹	524,288	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H	L	H	L	L	2 ²⁰	1,048,576	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H	L	H	L	H	2 ²¹	2,097,152	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H	L	H	H	L	2 ²²	4,194,304	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H	L	H	H	H	2 ²³	8,388,608	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H	H	L	L	L	2 ²⁴	16,777,216	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H	H	L	L	H	2 ²⁵	33,554,432	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H	H	L	H	L	2 ²⁶	67,108,864	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H	H	L	H	H	2 ²⁷	134,217,728	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H	H	H	L	L	2 ²⁸	268,435,456	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H	H	H	L	H	2 ²⁹	536,870,912	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H	H	H	H	L	2 ³⁰	1,073,741,824	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
H	H	H	H	H	2 ³¹	2,147,483,648	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216

3 TTL DEVICES

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

'LS294 FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2 ²	4	2 ⁹	512
L	L	H	H	2 ³	8	2 ⁹	512
L	H	L	L	2 ⁴	16	2 ⁹	512
L	H	L	H	2 ⁵	32	2 ⁹	512
L	H	H	L	2 ⁶	64	2 ⁹	512
L	H	H	H	2 ⁷	128	Disabled Low	
H	L	L	L	2 ⁸	256	2 ²	4
H	L	L	H	2 ⁹	512	2 ³	8
H	L	H	L	2 ¹⁰	1,024	2 ⁴	16
H	L	H	H	2 ¹¹	2,048	2 ⁵	32
H	H	L	L	2 ¹²	4,096	2 ⁶	64
H	H	L	H	2 ¹³	8,192	2 ⁷	128
H	H	H	L	2 ¹⁴	16,384	2 ⁸	256
H	H	H	H	2 ¹⁵	32,768	2 ⁹	512

switching loads

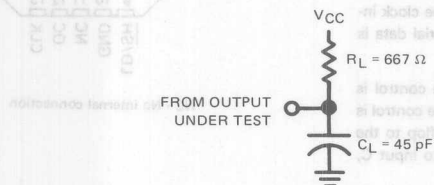
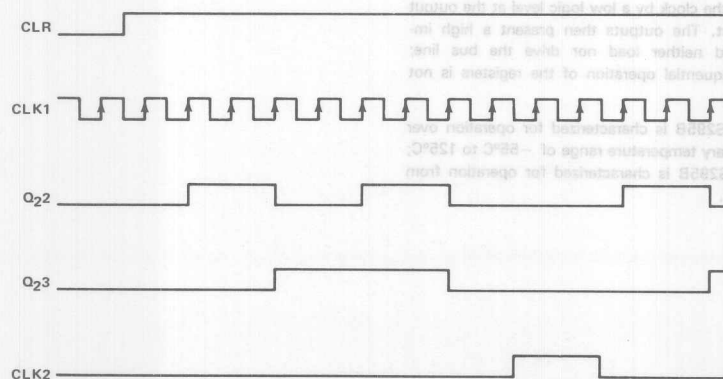


FIGURE 1

'LS292 and 'LS294 timing diagram



TYPES SN54LS295B, SN74LS295B 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

OCTOBER 1976—REVISED DECEMBER 1983

- **'LS295B Offers Three Times the Sink-Current Capability of 'LS295A**
- **Schottky-Diode-Clamped Transistors**
- **Low Power Dissipation . . . 80 mW Typical (Enabled)**
- **Applications:**
 - N-Bit Serial-To-Parallel Converter**
 - N-Bit Parallel-To-Serial Converter**
 - N-Bit Storage Register**

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock (CLK), serial (SER), mode (LD/SH), and outputs control (OC) inputs. The registers have three modes of operation:

Parallel (broadside) load

Shift right (the direction Q_A toward Q_D)

Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

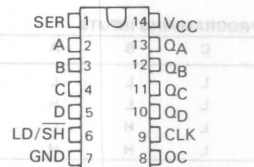
Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

The SN54LS295B is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS295B is characterized for operation from 0°C to 70°C .

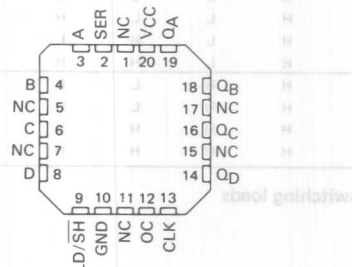
SN54LS295B . . . J OR W PACKAGE
SN74LS295B . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS295B . . . FK PACKAGE
SN74LS295B

(TOP VIEW)

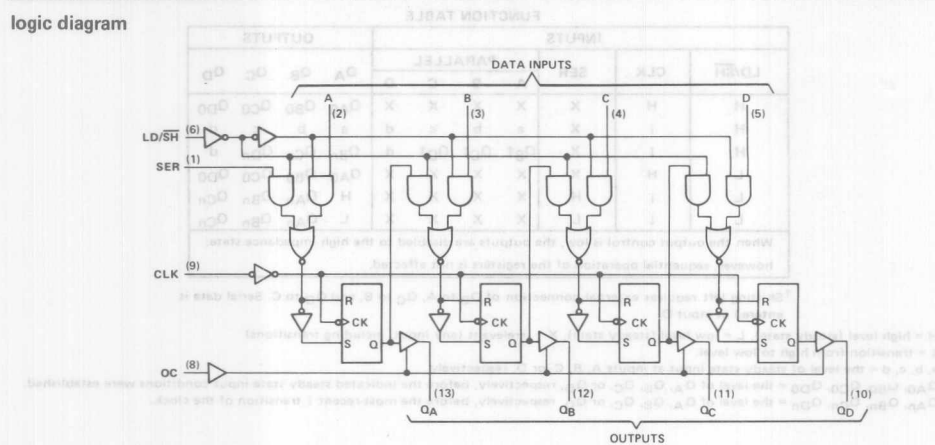


NC - Nc internal connection

3 TTL DEVICES

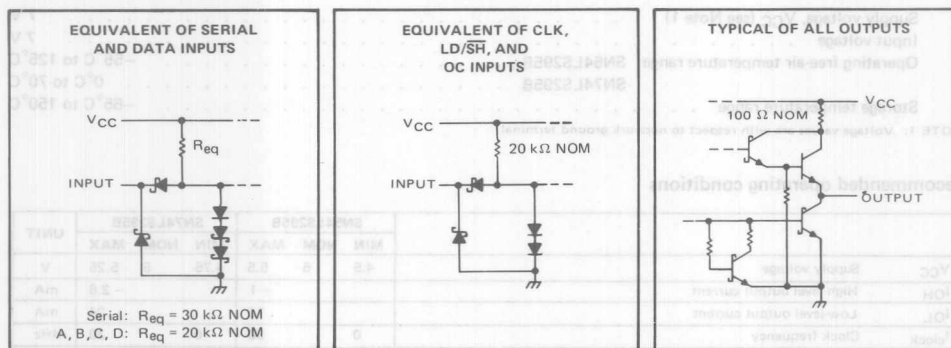
TYPES SN54LS295B, SN74LS295B 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54LS295B, SN74LS295B 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

FUNCTION TABLE										
INPUTS						OUTPUTS				
LD/ $\overline{\text{SH}}$	CLK	SER	PARALLEL				Q _A	Q _B	Q _C	Q _D
			A	B	C	D				
H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q _B [†]	Q _C [†]	Q _D [†]	d	Q _{Bn}	Q _{Cn}	Q _{Dn}	d
L	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
L	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
L	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.										

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

[†]Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS295B	−55°C to 125°C
SN74LS295B	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS295B			SN74LS295B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			−1			−2.6	mA
I _{OL}	Low-level output current			12			24	mA
f _{clock}	Clock frequency	0		30	0		30	MHz
t _{w(clock)}	Width of clock pulse	16			16			ns
t _{su}	Setup time, high-level or low-level data	20			20			ns
t _{su}	Setup time, LD/ $\overline{\text{SH}}$ to CLK	high-level		25	high-level		25	ns
		low-level		30	low-level		30	
t _h	Hold time, high-level or low-level data	5			5			ns
t _h	Hold time, high-level or low-level LD/ $\overline{\text{SH}}$ to CLK	0			0			ns
T _A	Operating free-air temperature	−55		125	0		70	°C

3

TTL DEVICES

TYPES SN54LS295B, SN74LS295B
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS
WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS295B			SN74LS295B			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.7			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4		2.4	3.1		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max		0.25	0.4		0.25	0.4	V
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IL} = V _{IL} max, V _O = 2.7 V			20			20	μA
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-20			-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS} Short-circuit output current [§]	V _{CC} = MAX	-30		-130	-30		-130	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	Condition A		20	29		20	29
		Condition B		22	33		22	33

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:

- A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
- B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} Maximum clock frequency		30	45		MHz
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 45 pF, See Note 3		14	20	ns
t _{PHL} Propagation delay time, high-to-low-level output			19	30	ns
t _{PZH} Output enable time to high level			18	26	ns
t _{PZL} Output enable time to low level			20	30	ns
t _{PHZ} Output disable time from high level	C _L = 5 pF, See Note 3		13	20	ns
t _{PLZ} Output disable time from low level			13	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	SNAL2255B		UNIT
		MIN	TYP. MAX	
V_{IH} High-level input voltage		2		V
V_{IL} Low-level input voltage		0.1		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN.}$ $I_I = -18 \text{ mA}$	-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MAX.}$ $V_{IH} = 3 \text{ V}$ $V_{IL} = V_{IL} \text{ MAX.}$ $I_{OH} = \text{MAX.}$	2.4	2.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 3 \text{ V}$ $V_{IL} = V_{IL} \text{ MAX.}$ $I_{OL} = 24 \text{ mA}$	0.1	0.1	V
On-state output current	$V_{CC} = \text{MAX.}$ $V_{IL} = V_{IL} \text{ MAX.}$	20	20	mA
High-level output current	$V_{CC} = \text{MAX.}$ $V_{OH} = 2.3 \text{ V}$	20	20	mA
Low-level output current	$V_{CC} = \text{MAX.}$ $V_{OL} = 0.4 \text{ V}$	20	20	mA
Input current at maximum input voltage	$V_{CC} = \text{MAX.}$ $V_I = 3 \text{ V}$	0.1	0.1	mA
High-level input current	$V_{CC} = \text{MAX.}$ $V_I = 2.3 \text{ V}$	20	20	mA
Low-level input current	$V_{CC} = \text{MAX.}$ $V_I = 0.4 \text{ V}$	-0.4	-0.4	mA
Short-circuit output current ²	$V_{CC} = \text{MAX.}$	30	30	mA
Supply current	$V_{CC} = \text{MAX.}$	35	35	mA

¹ For conditions shown as MIN or MAX, use the appropriate value shown in the recommended operating conditions table. All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

² For conditions shown as MIN or MAX, use the appropriate value shown in the recommended operating conditions table. All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$. For conditions shown as MIN or MAX, use the appropriate value shown in the recommended operating conditions table. All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

3

TTL DEVICES

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 867 \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock frequency		30	45		MHz
Propagation delay time, low-to-high level output	$C_L = 48 \text{ pF}$ See Note 2	14	20	28	ns
Propagation delay time, high-to-low level output		13	20	28	ns
Output enable time to high level		18	28		ns
Output enable time to low level		20	30		ns
Output disable time from high level	$C_L = 48 \text{ pF}$ See Note 2	13	20		ns
Output disable time from low level		12	20		ns

NOTE 2: See General Information section for load circuit and voltage waveforms.

TYPES SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED -LOOP FILTERS

D2629, JANUARY 1981

- Digital Design Avoids Analog Compensation Errors
- Easily Cascadable for Higher Order Loops
- Useful Frequency from DC to:
50 MHz Typical (K Clock)
35 MHz Typical (I/D Clock)

description

The SN54LS297 and SN74LS297 devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-N counter, to build first order phase-locked loops as described in Figure 1.

Both exclusive-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher order phase-locked loops.

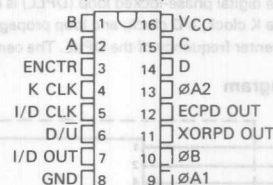
The length of the up/down K counter is digitally programmable according to the K counter function table.

With A, B, C, and D all low, the K counter is disabled.

With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C, and D are all programmed high, the K counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A through D inputs can maximize the overall performance of the digital phase-locked loop.

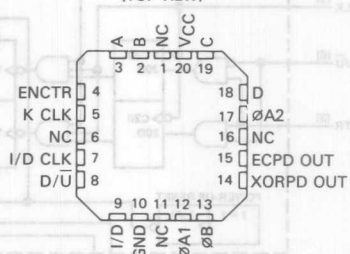
SN54LS297 ... J OR W PACKAGE
SN74LS297 ... J OR N PACKAGE

(TOP VIEW)



SN54LS297 ... FK PACKAGE
SN74LS297

(TOP VIEW)



NC-No internal connection

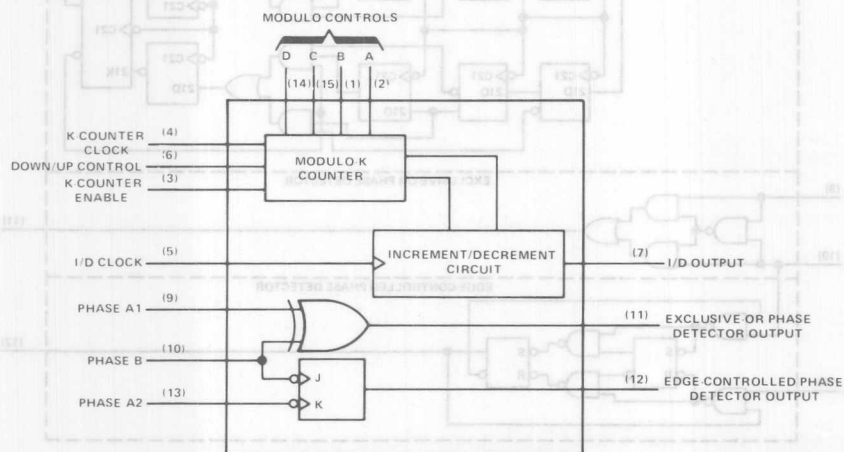


FIGURE 1—SIMPLIFIED BLOCK DIAGRAM

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3

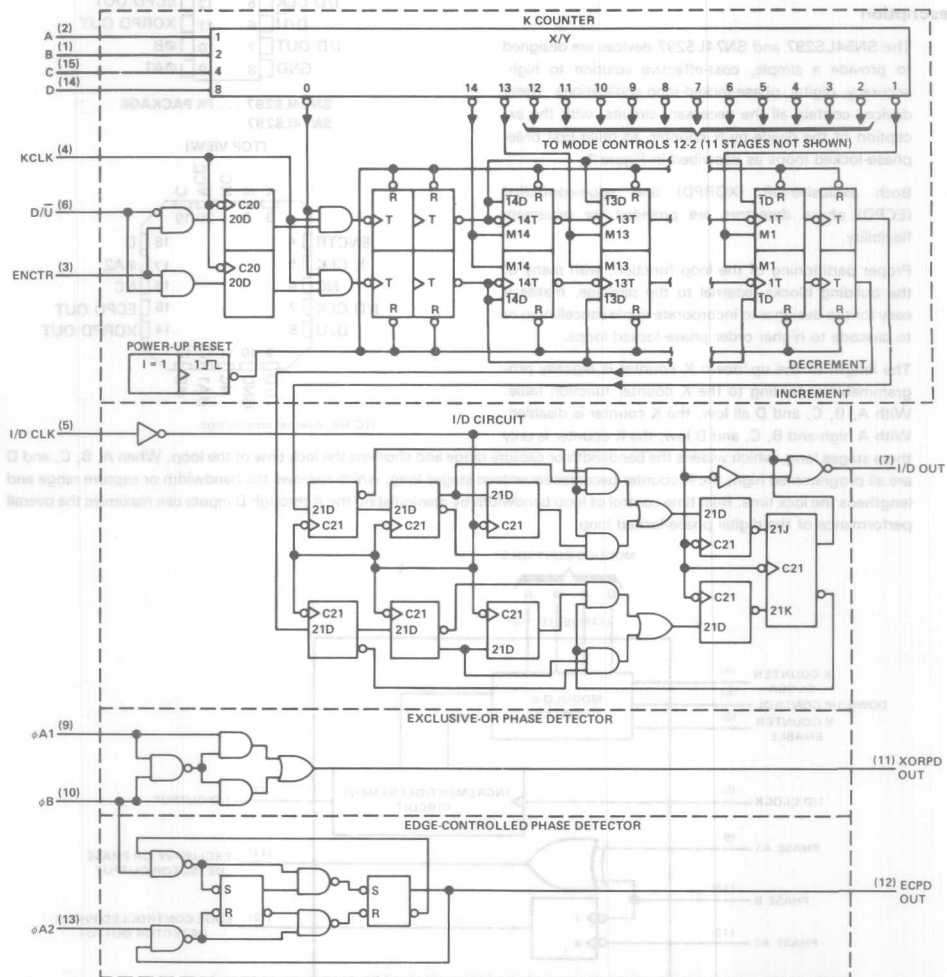
TTL DEVICES

TYPES SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

description (continued)

The 'LS297 can perform the classic first-order phase-locked loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K clock, I/D clock, and loop propagation delays. The I/D clock frequency and the divide-by-N modulus will determine the center frequency of the DPLL. The center frequency is defined by the relationship $f_c = I/D \text{ Clock}/2N \text{ (Hz)}$.

logic diagram



Pin numbers shown on logic notation are for J or N packages.

3

TTL DEVICES

TYPES SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	23
L	L	H	L	24
L	L	H	H	25
L	H	L	L	26
L	H	L	H	27
L	H	H	L	28
L	H	H	H	29
H	L	L	L	210
H	L	L	H	211
H	L	H	L	212
H	L	H	H	213
H	H	L	L	214
H	H	L	H	215
H	H	H	L	216
H	H	H	H	217

FUNCTION TABLE

EXCLUSIVE-OR PHASE DETECTOR

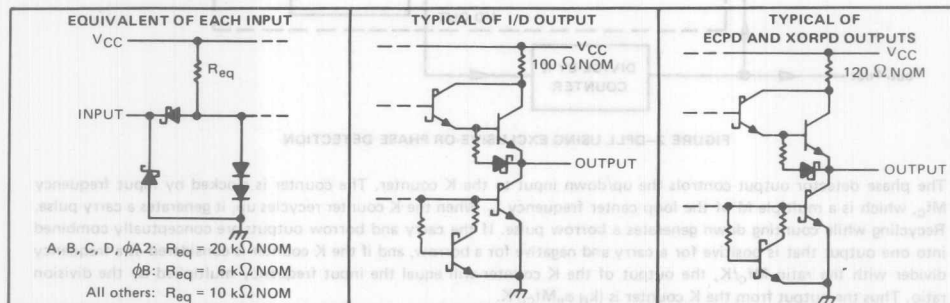
$\phi A1$	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR

$\phi A2$	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

schematics of inputs and outputs



operation

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty cycle square wave. At the limits of linear operation, the phase detector output will be either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase detector output varies linearly with the input phase error according to the gain k_d , which is expressed in terms of phase detector output per cycle of phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{PD Output} = \frac{\% \text{ high} - \% \text{ low}}{100} \quad (1)$$

The output of the phase detector will be $k_d \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

TYPES SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

Exclusive-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function, but can be described generally as a circuit that changes states on one of the transitions of its inputs. k_d for an XORPD is 4 because its output remains high (PD output = 1) for a phase error of 1/4 cycle. Similarly, k_d for the ECPD is 2 since its output remains high for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for ϕ_e defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase detector output is a square wave. The XORPD inputs are 1/4 cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are 1/2 cycle out of phase.

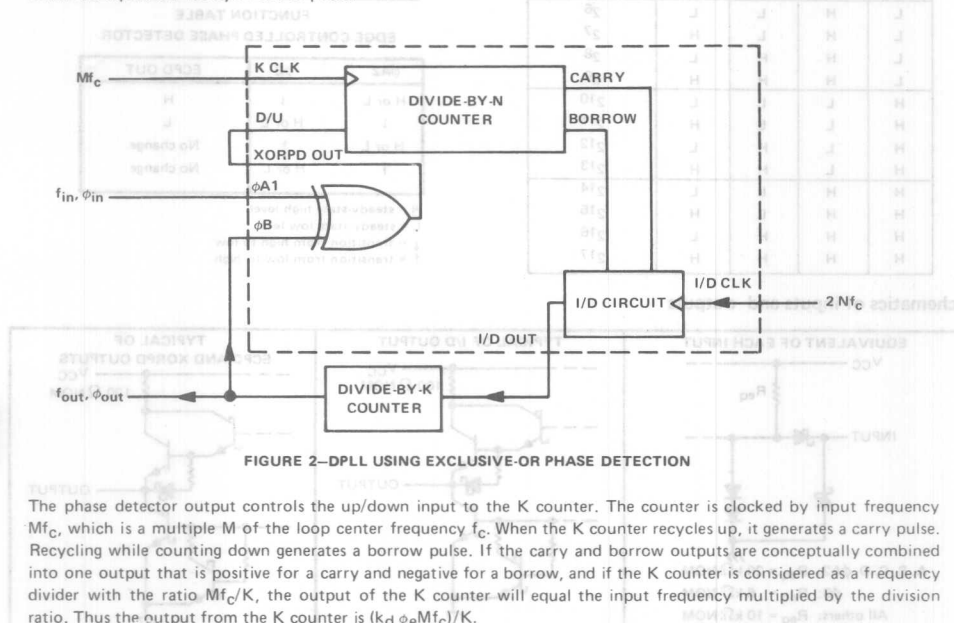


FIGURE 2—DPLL USING EXCLUSIVE-OR PHASE DETECTION

The phase detector output controls the up/down input to the K counter. The counter is clocked by input frequency Mf_c , which is a multiple M of the loop center frequency f_c . When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio Mf_c/K , the output of the K counter will equal the input frequency multiplied by the division ratio. Thus the output from the K counter is $(k_d \phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is 1/2 of the input clock I/D CLK. The input clock is just a multiple, $2N$, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D OUT. Thus the output of the I/D circuit will be $Nf_c + (k_d \phi_e Mf_c)/2K$.

The output of the N counter (or the output of the phase-locked loop) is thus:

$$(1) \quad f_o = f_c + (k_d \phi_e Mf_c)/2KN$$

If this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for $M = 2N$.

Thus the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

TYPES SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

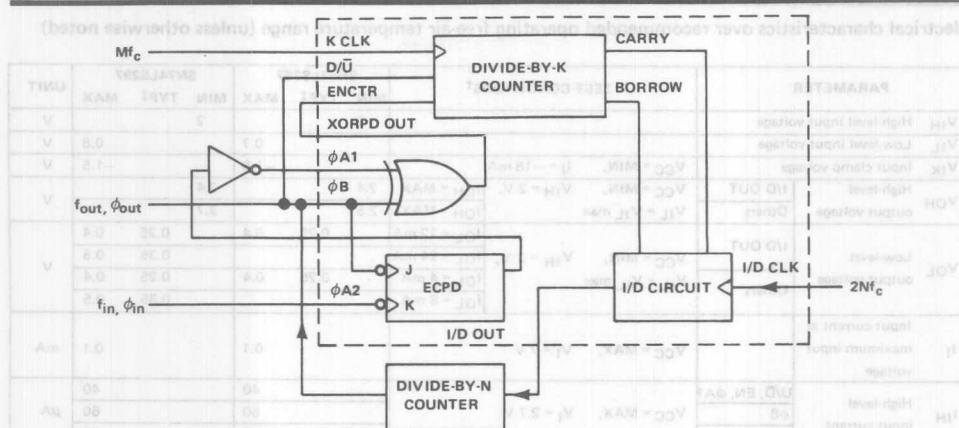


FIGURE 3—DPPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS297	– 55°C to 125°C
SN74LS297	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS297			SN74LS297			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	I/D OUT			– 1.2			– 1.2	mA
		EXOR, ECPD			– 400			– 400	μ A
I_{OL}	Low-level output current	I/D OUT			12			24	mA
		XOR, ECPD			4			8	mA
f_{clock}	Clock frequency	K Clock	0		32	0		32	MHz
		I/D Clock	0		16	0		16	MHz
t_w	Width of clock input pulse	K Clock	16			16			ns
		I/D Clock	33			33			ns
$t_{su, to K}$	Setup time to K Clock t	U/D, ENCTR	30			30			ns
t_h	Hold time from K Clock t	U/D, ENCTR	0			0			ns
T_A	Operating free-air temperature		– 55		125	0		70	°C

TYPES SN54LS297, SN74LS297 DIGITAL PHASE-LOCKED-LOOP FILTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS297			SN74LS297			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	I/D OUT	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = \text{MAX}$	2.4		2.4			V
	Others	$V_{IL} = V_{IL \text{ max}}, I_{OH} = \text{MAX}$	2.5		2.7			V
V_{OL} Low-level output voltage	I/D OUT	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}$				0.35	0.5	V
	Others	$V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$				0.35	0.5	V
I_I Input current at maximum input voltage		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1	mA
I_{IH} High-level input current	U/D, EN, $\phi A1$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		40			40	μA
	ϕB			60			60	μA
	All others			20			20	μA
I_{IL} Low-level input current	U/D, EN, $\phi A1$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8			-0.8	mA
	ϕB			-1.2			-1.2	mA
	All others			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	I/D OUT	$V_{CC} = \text{MAX}$	-30	-130	-30	-130	-130	mA
	Others		-20	-100	-20	-100	-100	mA
I_{CC} Supply current		$V_{CC} = \text{MAX}, \text{All inputs grounded, All outputs open}$	75	120	75	120	120	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are of $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER†	FROM (INPUT)		TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	K CLK		I/D OUT	$R_L = 667 \Omega,$ $C_L = 45 \text{ pF},$ See Note 2	32	50		MHz
	I/D CLK		I/D OUT		16	35		MHz
t_{PLH}	I/D CLK †		I/D OUT	See Note 2		15	25	ns
t_{PHL}	I/D CLK †		I/D OUT			22	35	ns
t_{PLH}	$\phi A1$ or ϕB	Other input low	XOR OUT	$R_L = 2 \text{ k}\Omega,$ $C_L = 45 \text{ pF},$ See Note 2		10	15	ns
	$\phi A1$ or ϕB	Other input high	XOR OUT			17	25	ns
t_{PHL}	$\phi A1$ or ϕB	Other input low	XOR OUT	See Note 2		15	25	ns
	$\phi A1$ or ϕB	Other input high	XOR OUT			17	25	ns
t_{PLH}	$\phi B \downarrow$		ECPD OUT	See Note 2		20	30	ns
t_{PHL}	$\phi A2 \downarrow$		ECPD OUT			20	30	ns

† t_{PLH} = propagation delay time, low-to-high level output

t_{PHL} = propagation delay time, high-to-low level output

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

ITL DEVICES

TYPES SN54298, SN54LS298, SN74298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

MARCH 1974 - REVISED DECEMBER 1983

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
 - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
 - Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability
 - Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

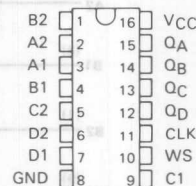
description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 or SN54LS157/SN74LS157 and SN54175/SN74175 or SN54LS175/SN74LS175) in a single 16-pin package.

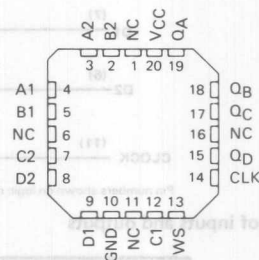
When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 195 milliwatts for the '298 and 65 milliwatts for the 'LS298. SN54298 and SN54LS298 are characterized for operation over the full military temperature range of -55°C to 125°C ; SN74298 and SN74LS298 are characterized for operation from 0°C to 70°C .

SN54298, SN54LS298 ... J OR W PACKAGE
SN74298 ... J OR N PACKAGE
SN74LS298 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS298 ... FK PACKAGE
SN74LS298 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	QA	QB	QC	QD
L	L	a1	b1	c1	d1
H	L	a2	b2	c2	d2
X	H	QA0	QB0	QC0	QD0

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

L = transition from high to low level

a1, a2, etc. = the level of steady state input at A1, A2, etc.

QA0, QB0, etc. = the level of QA, QB, etc. entered on the most recent L transition of the clock input.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

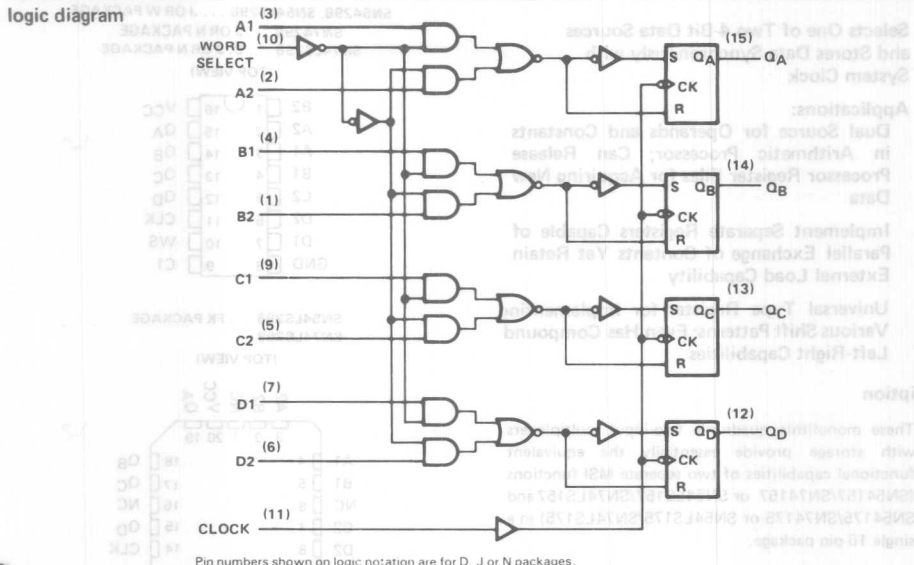
TEXAS
INSTRUMENTS

3-813

3

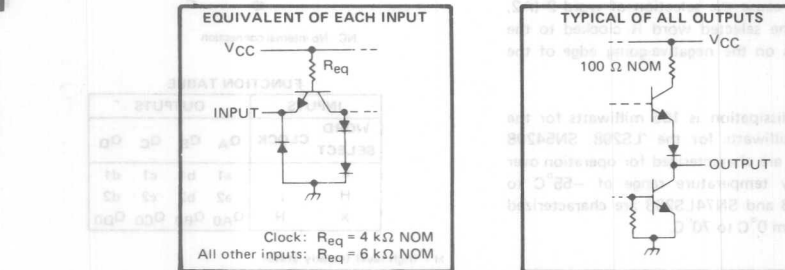
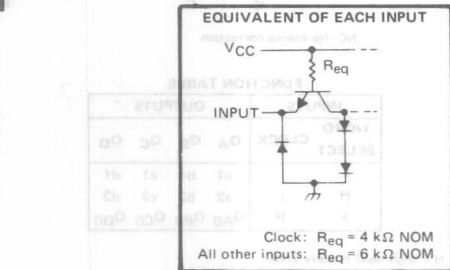
TTL DEVICES

logic diagram (3)

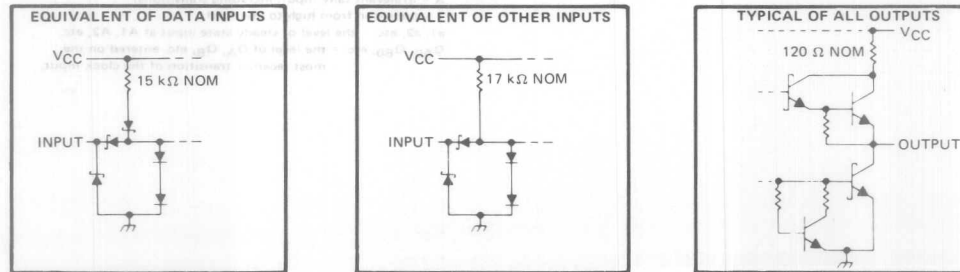
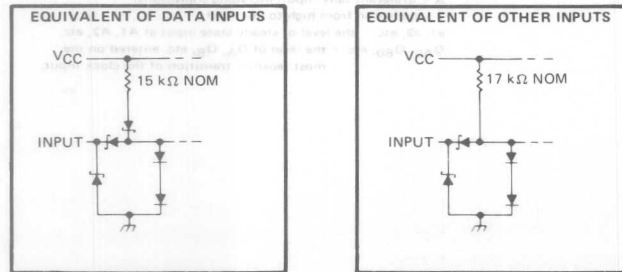
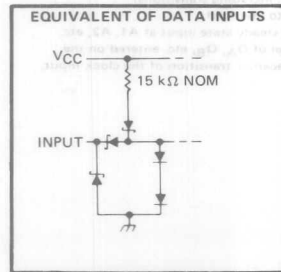


TTL DEVICES

schematics of inputs and outputs



'LS298



TYPES SN54298, SN74298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54298	-55°C to 125°C
SN74298	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54298			SN74298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, high or low level, t_W		20			20			ns
Setup time, t_{SU}	Data	15			15			ns
	Word select	25			25			ns
Hold time, t_H	Data	5			5			ns
	Word select	0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54298 -20		-57	mA
		SN74298 -18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		39	65	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 3		21	32	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS298	–55°C to 125°C
SN74LS298	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS298			SN74LS298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–400			–400	μ A
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_W		20			20			ns
Setup time, t_{SU}	Data	15			15			ns
	Word select	25			25			ns
Hold time, t_H	Data	5			5			ns
	Word select	0			0			ns
Operating free-air temperature, T_A		–55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS298			SN74LS298			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			–0.4			–0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	13	21		13	21		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$		18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 3		21	32	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

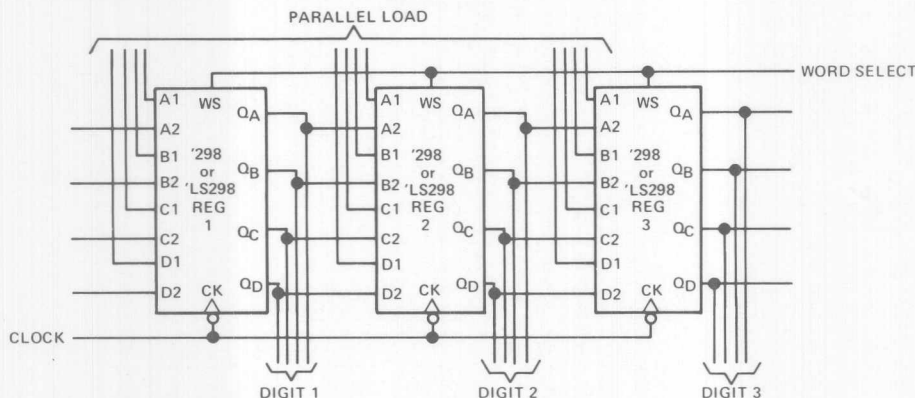
TTL DEVICES

TYPES SN54298, SN54LS298, SN74298, SN74LS298 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

TYPICAL APPLICATION DATA

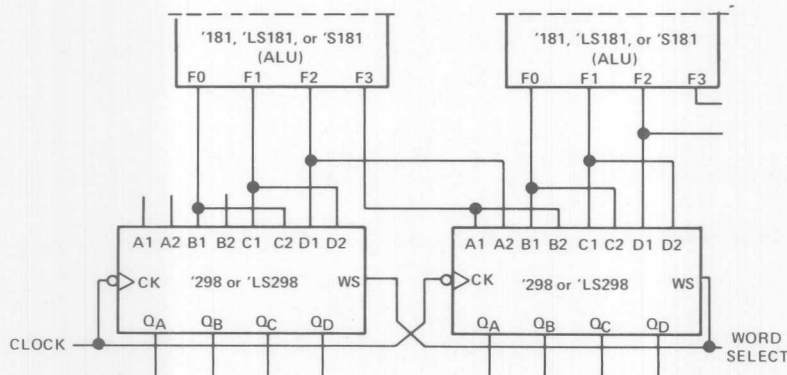
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '298 or 'LS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one place/two-place shift register.

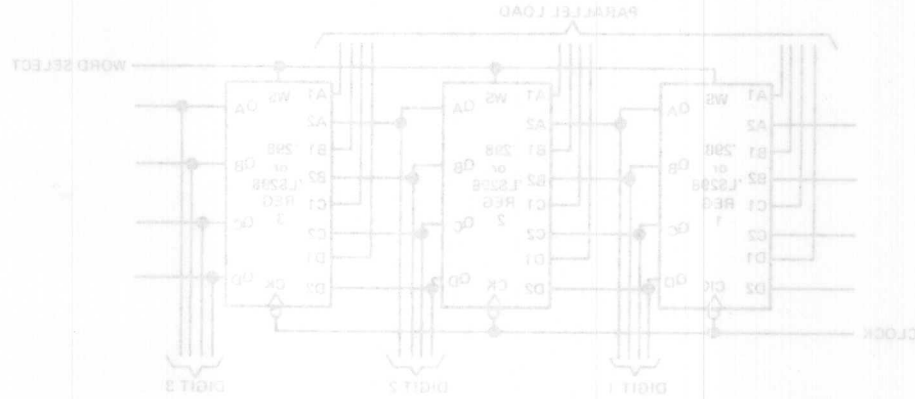


When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

TYPICAL APPLICATION DATA

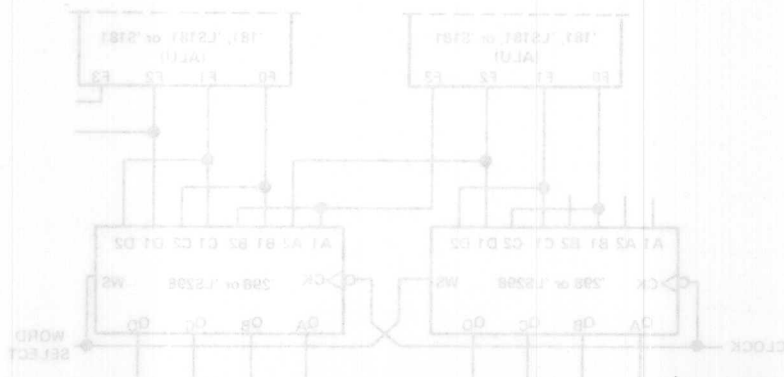
This versatile multiplexer/register can be connected to operate as a shift register that can shift N places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 transfer to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application requires a parallel load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '258 or 'L258 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place two-track shift register.



When word select is low and the registers are clocked, the outputs of the arithmetic units (A1's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

3

TTL DEVICES

TYPES SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

MARCH 1974 - REVISED APRIL 1985

- Multiplexed Inputs/Outputs Provide Improved Bit Density

- Four Modes of Operations:
Hold (Store) Shift Left
Shift Right Load Data

- Operates with Outputs Enabled or at High Z

- 3-State Outputs Drive Bus Lines Directly

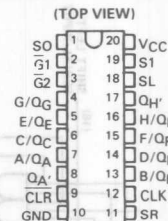
- Can Be Cascaded for N-Bit Word Lengths

- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear

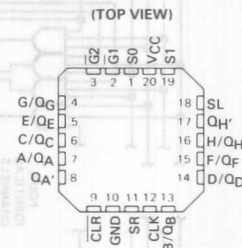
- Applications:
Stacked or Push-Down Registers
Buffer Storage, and Accumulator
Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW, J OR N PACKAGE



SN54LS299, SN54S299 . . . FK PACKAGE
SN74LS299, SN74S299



description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS												OUTPUT	
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'		
		S1	S0	G1 [†]	G2 [†]		SL	SR												
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L		
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L		
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0		
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0		
Shift Right	H	L	H	L	L	†	X	H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QH _n		
	H	L	H	L	L	†	X	L	L	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	L	QH _n		
Shift Left	H	H	L	L	L	†	H	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	H	QB _n	H		
	H	H	L	L	L	†	L	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	L	QB _n	L		
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h		

[†]When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

[†]When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

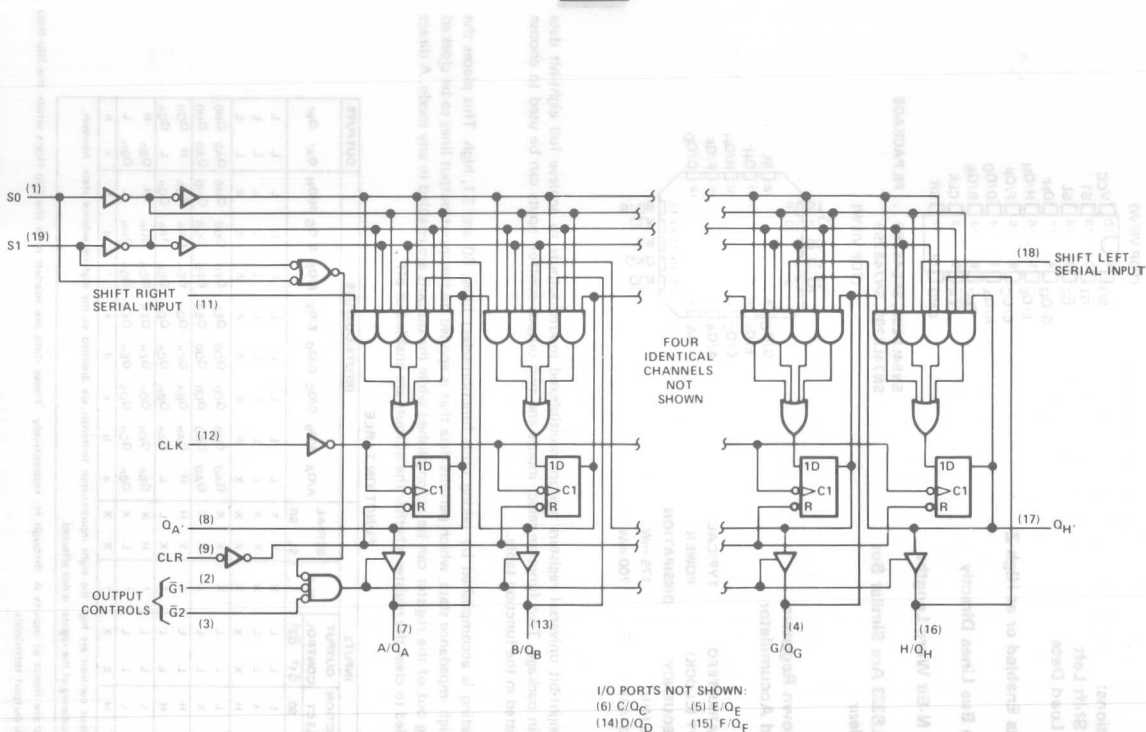
PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-819

TYPES SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

Logic diagram



TTL DEVICES

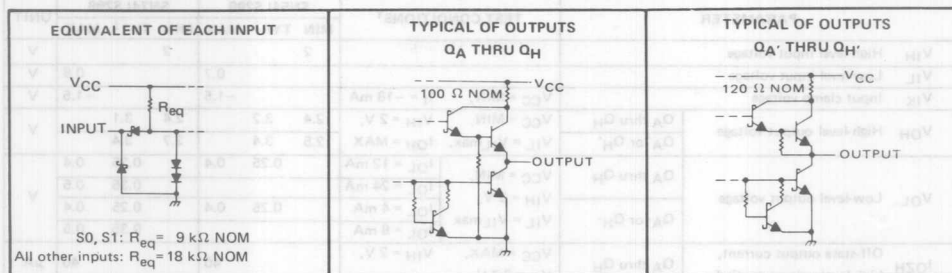
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3-820

TEXAS
INSTRUMENTS

TYPES SN54LS299, SN74LS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS299	-55°C to 125°C
SN74LS299	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	Q _A thru Q _H			-1			-2.6	mA
	Q _A ' or Q _H '			-0.4			-0.4	
Low-level output current, I _{OL}	Q _A thru Q _H			12			24	mA
	Q _A ' or Q _H '			4			8	
Clock frequency, f _{clock}		0		20	0		20	MHz
Width of clock pulse, t _{w(clock)}	Clock high	30			30			ns
	Clock low	10			10			
Width of clear pulse, t _{w(clear)}	Clear low	20			20			ns
	Select	35†			35†			
Setup time, t _{su}	High-level data [◇]	20†			20†			ns
	Low-level data [◇]	20†			20†			
	Clear inactive-state	20†			20†			
	Select	10†			10†			
Hold time, t _h	Data [◇]	0†			0†			ns
Operating free-air temperature, T _A		-55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.

3

TTL DEVICES

TYPES SN54LS299, SN74LS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS299			SN74LS299			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.7			0.8	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V	
V _{OH}	High-level output voltage	Q _A thru Q _H Q _A ' or Q _H '	V _{CC} = MIN, V _{IH} = 2 V, V _I L = V _I Lmax, I _{OH} = MAX	2.4	3.2		2.4	3.1	V	
V _{OL}	Low-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V, V _I L = V _I Lmax	I _{OL} = 12 mA I _{OL} = 24 mA	0.25	0.4	0.25	0.4		V
		Q _A ' or Q _H '		I _{OL} = 4 mA I _{OL} = 8 mA	0.25	0.4	0.35	0.5		
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V			40		40	μA	
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V			-400		-400	μA	
I _I	Input current at maximum input voltage	S0, S1	V _{CC} = MAX	V _I = 7 V		200		200	μA	
		A thru H		V _I = 5.5 V		100		100		
		Any other		V _I = 7 V		100		100		
I _{IH}	High-level input current	A thru H, S0, S1 Any other	V _{CC} = MAX, V _I = 2.7 V			40		40	μA	
I _{IL}	Low-level input current	S0, S1				20		20		
		Any other	V _{CC} = MAX, V _I = 0.4 V			-0.8		-0.8	mA	
I _{OS}	Short-circuit output current§	Q _A thru Q _H	V _{CC} = MAX			-30		-130		mA
		Q _A ' or Q _H '				-20		-100		
I _{CC}	Supply current		V _{CC} = MAX			33		53	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	20	35		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 2 kΩ, C _L = 15 pF		22	33	ns
t _{PHL}		Q _A ' or Q _H '			26	39	
t _{PLH}	CLK	Q _A thru Q _H	R _L = 665 Ω, C _L = 45 pF		17	25	ns
t _{PHL}		Q _A thru Q _H			26	39	
t _{PZH}	G1, G2	Q _A thru Q _H	R _L = 665 Ω, C _L = 5 pF		13	21	ns
t _{PZL}		Q _A thru Q _H			19	30	
t _{PHZ}	G1, G2	Q _A thru Q _H			10	20	ns
t _{PLZ}		Q _A thru Q _H			10	15	

¶f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

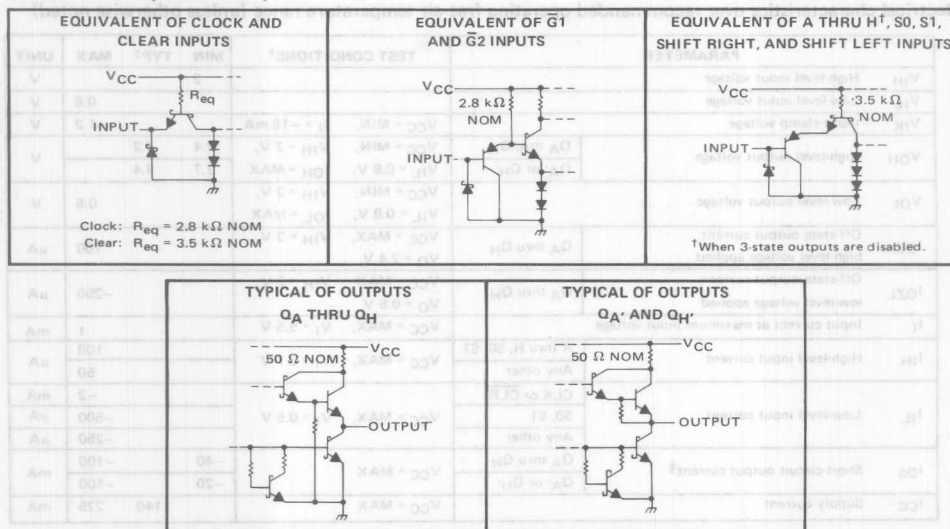
t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

See General Information Section for load circuits and voltage waveforms.

TYPES SN54S299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S299 (see Note 2)	-55°C to 125°C
SN74S299	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			-2			-6.5	mA
	Q_A' or Q_H'			-0.5			-0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	Q_A' or Q_H'			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_w(\text{clock})$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_w(\text{clear})$	Clear low	10			10			ns
	Clear high							
Setup time, t_{su}	Select	15 [†]			15 [†]			ns
	High-level data [◊]	7 [†]			7 [†]			
	Low-level data [◊]	5 [†]			5 [†]			
	Clear inactive-state	10 [†]			10 [†]			
Hold time, t_h	Select	5 [†]			5 [†]			ns
	Data [◊]	5 [†]			5 [†]			
Operating free-air temperature, T_A		-55		125	0		70	°C

[◊]Data includes the two serial inputs and the eight input/output data lines.

TYPES SN54S299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH} High-level output voltage	Q_A thru Q_H	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.2	V
	Q_A' or Q_H'		2.7	3.4	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$			0.5	V
I_{OZH} Off-state output current, high-level voltage applied	Q_A thru Q_H	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.4 \text{ V}$		100	μA
I_{OZL} Off-state output current, low-level voltage applied	Q_A thru Q_H	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.5 \text{ V}$		-250	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	A thru H, S0, S1	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		100	μA
	Any other			50	
I_{IL} Low-level input current	CLK or CLR	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2	mA
	S0, S1			-500	
	Any other			-250	
I_{OS} Short-circuit output current§	Q_A thru Q_H	$V_{CC} = \text{MAX}$		-40	mA
	Q_A' or Q_H'			-100	
I_{CC} Supply current	$V_{CC} = \text{MAX}$			140	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	50	70		MHz
t_{PLH}	CLK	Q_A' or Q_H'	$R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}$	12	20		ns
t_{PHL}		Q_A' or Q_H'		13	20		
t_{PHL}	CLR	Q_A' or Q_H'		14	21		ns
t_{PLH}	CLK	Q_A thru Q_H	$R_L = 280 \Omega, C_L = 45 \text{ pF}$	15	21		ns
t_{PHL}		Q_A thru Q_H		15	21		
t_{PHL}	CLR	Q_A thru Q_H		16	24		ns
t_{PZH}	$\bar{G}1, \bar{G}2$	Q_A thru Q_H	$R_L = 280 \Omega, C_L = 5 \text{ pF}$	10	18		ns
t_{PZL}		Q_A thru Q_H		12	18		
t_{PHZ}	$\bar{G}1, \bar{G}2$	Q_A thru Q_H		7	12		ns
t_{PLZ}		Q_A thru Q_H		7	12		

¶ f_{max} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max} , all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321 CRYSTAL-CONTROLLED OSCILLATORS

D2418, DECEMBER 1978—REVISED JANUARY 1981

'LS320

- Crystal-Controlled Oscillator Operation from 1 MHz to 20 MHz
- 2-Phase Driver Outputs

'LS321

- Similar to 'LS320 But Includes f/2 and f/4 Count-Down Outputs

description

The 'LS320 is a crystal-controlled oscillator/clock driver. It features complementary standard and high-current driver outputs. A synchronization flip-flop is included.

The driver outputs, F' and \bar{F}' have very-low impedance and can be used to drive highly capacitive TTL-level lines. If the driver outputs are not used, then the VCC' terminal can be left open.

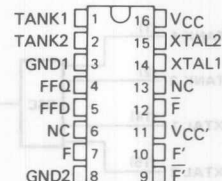
The 'LS321 is identical to the 'LS320 except it additionally features two count-down outputs, F/2 and F/4.

These circuits were designed for series resonant crystal control of frequency, and a capacitive control is not recommended. The crystal is connected between the inputs XTAL1 and XTAL2. A parallel-resonant circuit has to be connected between the inputs TANK1 and TANK2 (see Typical Application Data).

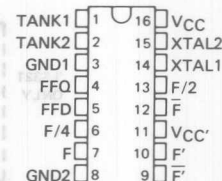
Interaction of the driver outputs with the other outputs limits useful frequencies as shown in the frequency-limits table.

The SN54LS320 and SN54LS321 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS320 and SN74LS321 are characterized for operation from 0°C to 70°C.

SN54LS320 ... J PACKAGE
SN74LS320 ... J OR N PACKAGE
(TOP VIEW)



SN54LS321 ... J PACKAGE
SN74LS321 ... J OR N PACKAGE
(TOP VIEW)



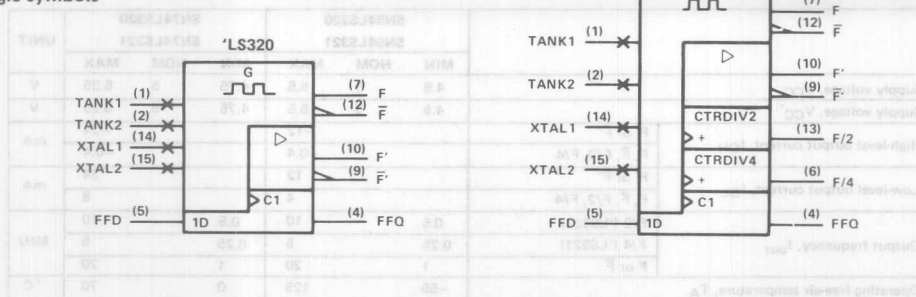
NC - No internal connection

For chip carrier information,
contact the factory.

FREQUENCY LIMITS

OUTPUTS IN USE	VCC	VCC'	f _{max}
Driver outputs only	5 V	5 V	20 MHz
Other outputs only	5 V	Open	20 MHz
Driver and any other outputs	5 V	5 V	10 MHz

logic symbols



PRODUCTION DATA

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TEXAS
INSTRUMENTS

3-825

3

TTL DEVICES

Supply voltage, V_{CC} (see Note 1)Supply voltage, V_{CC}

Input voltage to FFD terminal

Operating free-air temperature range: SN54LS320, SN54LS321

SN74LS320, SN74LS321

Storage temperature range

7 V

7 V

-0.5 V to 7 V

–55°C to 125°C

0°C to 70°C

–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

Input and output schematics are similar to those shown for SN74LS326.

TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321 CRYSTAL-CONTROLLED OSCILLATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS320		SN74LS320		UNIT		
				SN54LS321		SN74LS321				
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, V _{CC} ' = MIN, I _I = -18 mA				-1.5			-1.5	V
V _{OH}	High-level output voltage	F', F̄'	V _{CC} = 4.5 V, V _{CC} ' = 4.5 V, I _{OH} = -12 mA	2.5	3.3					V
			V _{CC} = 4.75 V, V _{CC} ' = 4.75 V, I _{OH} = -24 mA			2.7	3.3			
		Others	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -400 μA	2.5	3.4	2.7	3.4			
V _{OL}	Low-level output voltage	F', F̄'	V _{CC} = MIN, V _{CC} ' = MIN	I _{OL} = 12 mA	0.25	0.4	0.25	0.4		V
				I _{OL} = 24 mA			0.35	0.5		
		Others	V _{CC} = MIN, V _{IL} = V _{IL} max	I _{OL} = 4 mA	0.25	0.4	0.25	0.4		
				I _{OL} = 8 mA			0.35	0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1		0.1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				20		20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V				-0.4		-0.4	mA	
I _{OS}	Short-circuit output current§	V _{CC} = MAX				-20	-100	-20	-100	mA
I _{CC}	Supply current from V _{CC}	V _{CC} = MAX, FFD at GND	'LS320	42	70	42	70		mA	
			'LS321	47	75	47	75			
I _{CC} '	Supply current from V _{CC} '	V _{CC} = MAX, V _{CC} ' = MAX, FFD at GND			4	8	4	8	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, V_{CC}' = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs F' and \bar{F}' do not have short-circuit protection and these limits do not apply.

switching characteristics, $V_{CC} = 5 \text{ V}, V_{CC}' = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	OUTPUTS	TEST CONDITIONS	'LS320			'LS321			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum operating frequency	F/2				10	15		MHz
		F/4				5	7.5		
		All others				20	30		
t_r	Rise time, 1 V to 3 V	F', \bar{F}'	$C_L = 100 \text{ pF}$	$R_L = 667 \Omega$					ns
					6	12	6	12	
					7	14	7	14	
					7	14	7	14	
		Others	$C_L = 100 \text{ pF}$	$R_L = 2 \text{ k}\Omega$	11	22	11	22	
					25	40	25	40	
					45	70	45	70	
					45	70	45	70	
t_f	Fall time, 3 V to 1 V	F', \bar{F}'	$C_L = 100 \text{ pF}$	$R_L = 667 \Omega$	5	10	5	10	ns
					5	10	5	10	
					6	12	6	12	
					6	12	6	12	
		Others	$C_L = 100 \text{ pF}$	$R_L = 2 \text{ k}\Omega$	10	20	10	20	
					10	20	10	20	
					17	30	17	30	
					17	30	17	30	

¶ See General Information Section for load circuits and voltage waveforms.

TTL DEVICES

The SN54/74LS320 and 'LS321 are crystal-controlled oscillators. Figure 1 shows the device with all required external components.

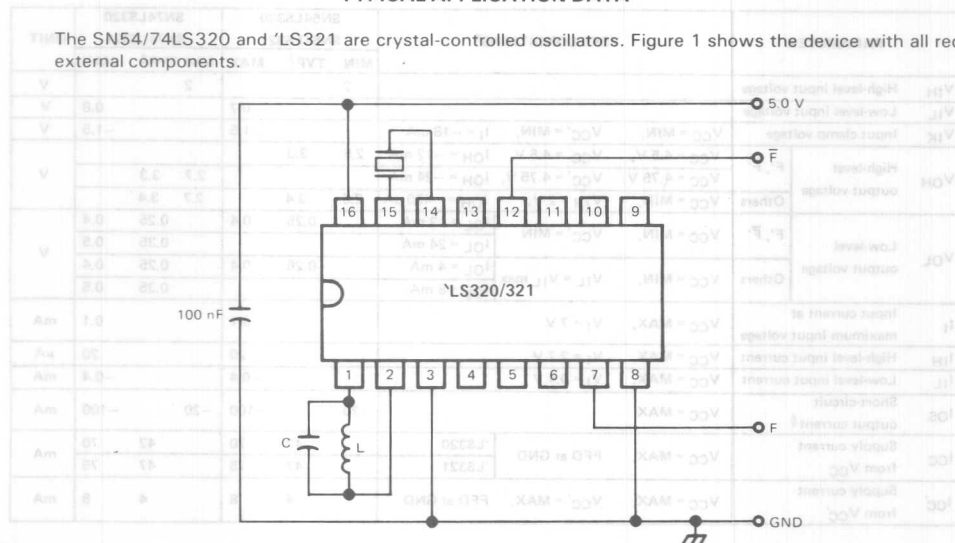


FIGURE 1. CRYSTAL-CONTROLLED OSCILLATOR 'LS320/321

If a fundamental crystal is used the value of the inductor L has to be determined according to curve 1 in figure 2. The value of the capacitor C is calculated:

$$C = \frac{1}{4 \times \pi^2 \times f^2 \times L} \quad (1)$$

The XTAL1 and XTAL2 inputs have a input capacitance of 6 to 8 pF. These values have to be included into the calculation.

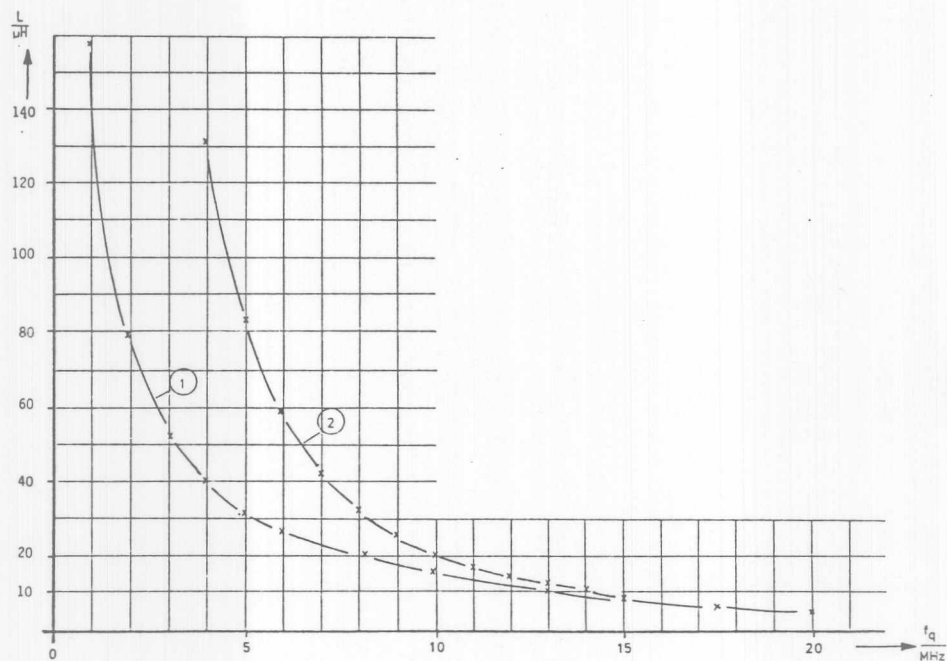
If a capacitor C1 for frequency adjustment is included in the circuit, the value of the inductor L has to be determined according to curve 2 in figure 2. In this case no capacitor in parallel to the inductor is needed.

If an overtone crystal is used, the value of the inductor L is calculated:

$$L = \frac{65}{f} \quad (2)$$

The value of the capacitor C has to be calculated according to formula 1.

TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321
CRYSTAL-CONTROLLED OSCILLATORS



— FUNDAMENTAL CRYSTAL FREQUENCY — MHz

FIGURE 2

3

TTL DEVICES

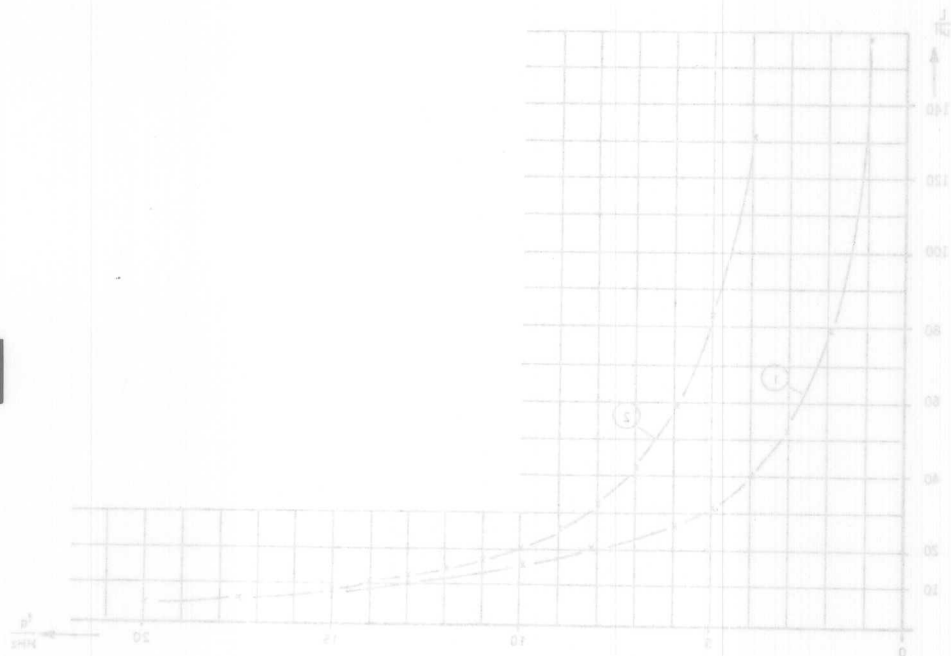


FIGURE 2
— FUNDAMENTAL CRYSTAL FREQUENCY — MHz

CRYSTAL-CONTROLLED OSCILLATORS
TYPES SN74LS320, SN74LS321, SN74LS320, SN74LS321

TYPES SN54LS322A, SN74LS322A 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

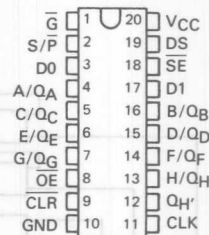
D2411, OCTOBER 1977—REVISED APRIL 1985

- **Multiplexed Inputs/Outputs**
Provide Improved Bit Density
- **3-State Outputs Drive Bus**
Lines Directly
- **Sign Extend Function**
- **Direct Overriding Clear**

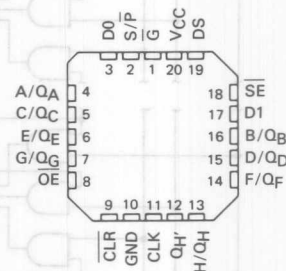
description

These low-power Schottky eight-bit shift registers feature multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output (Q_H') is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the Q_A flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

SN54LS322A ... J PACKAGE
SN74LS322A ... DW, J OR N PACKAGE
(TOP VIEW)



SN54LS322A ... FK PACKAGE
SN74LS322A
(TOP VIEW)



FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT QH
	CLR	REGISTER ENABLE G	S/P	SIGN EXTEND SE	DATA SELECT DS	OUTPUT ENABLE OE	CLK	A/QA	B/QB	C/QC . . . H/QH		
Clear	L	H	X	X	X	L	X	L	L	L	L	
	L	X	H	X	X	L	X	L	L	L	L	
Hold	H	H	X	X	X	L	X	QA0	QB0	QC0	QH0	
Shift Right	H	L	H	H	L	L	↑	D0	QA0	QB0	QH0	
	H	L	H	H	H	L	↑	D1	QAn	QBn	QHn	
Sign Extend	H	L	H	L	X	L	↑	QAn	QAn	QBn	QHn	
Load	H	L	L	X	X	X	↑	a	b	c	h	

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

$Q_{A0} \dots Q_{H0}$ = the level of Q_A through Q_H , respectively, before the indicated steady-state conditions were established

$Q_{An} \dots Q_{Hn}$ = the level of Q_A through Q_H , respectively, before the most recent ↑ transition of the clock

D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively

a ... h = the level of steady-state inputs at inputs A through H respectively

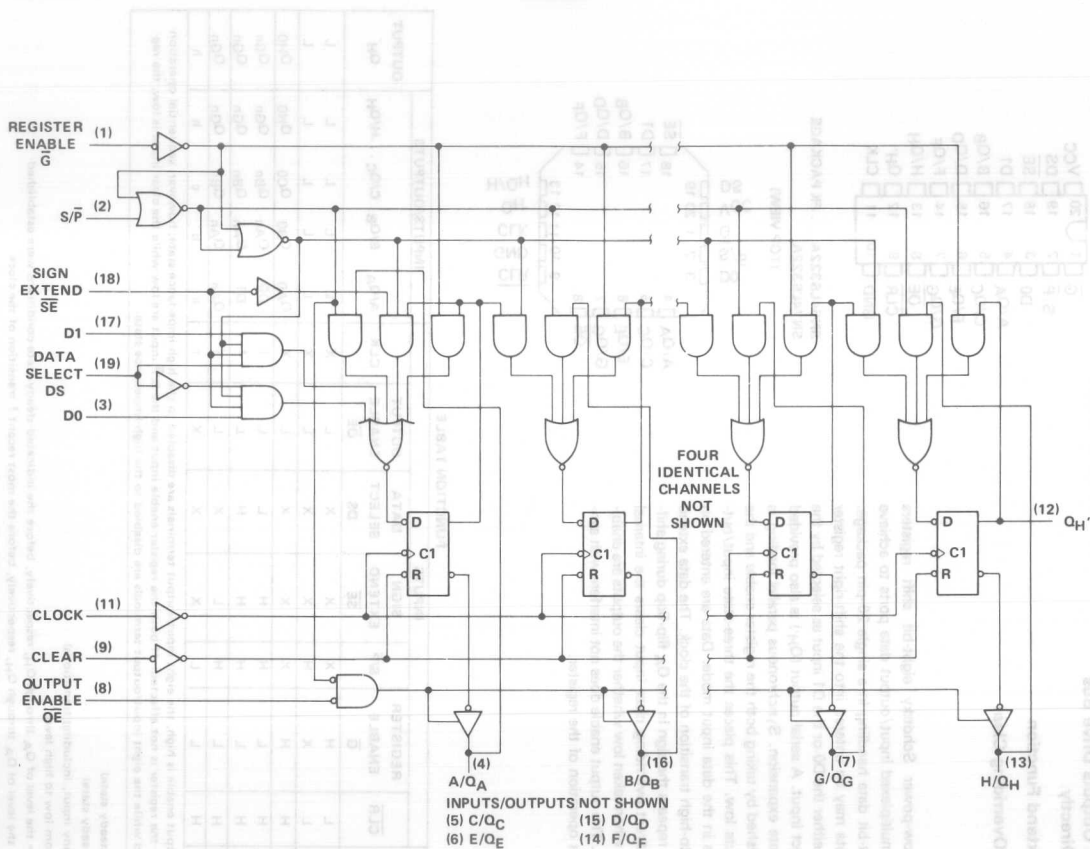
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54LS332A, SN74LS32A 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

TTL DEVICES

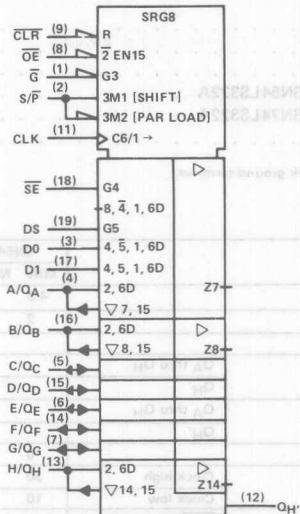
3

3-832

TEXAS
INSTRUMENTS

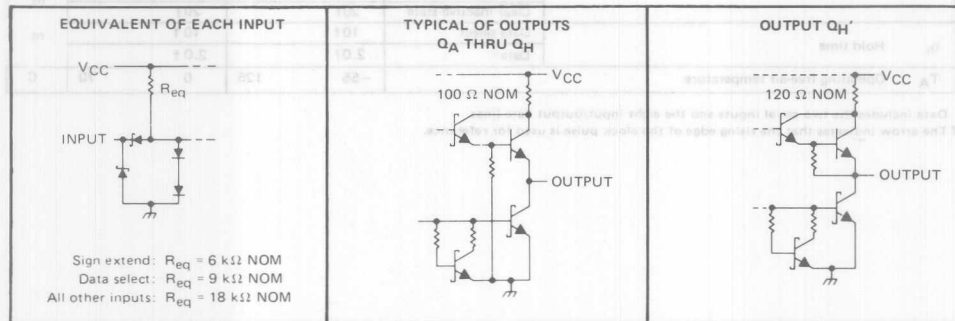
TYPES SN54LS322A, SN74LS322A
8-BIT SHIFT REGISTERS WITH SIGN EXTEND

logic symbol



Pin numbers shown on logic notation are for DW, J or N packages.

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54LS322A, SN74LS322A 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54LS322A	−55°C to 125°C
SN74LS322A	0°C to 70°C
Storage temperature	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS322A			SN74LS322A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	Q_A thru Q_H		−1	Q_A thru Q_H		−2.6	mA
		Q_H'		−0.4	Q_H'		−0.4	
I_{OL}	Low-level output current	Q_A thru Q_H		12	Q_A thru Q_H		24	mA
		Q_H'		4	Q_H'		8	
f_{clock}	Clock frequency	0		20	0		20	MHz
$t_{w(clock)}$	Width of clock pulse	Clock high		30	Clock high		30	ns
		Clock low		10	Clock low		10	
$t_{w(clear)}$		Clear low		20	Clear low		20	ns
t_{su}	Setup time	Data select		10†	Data select		10†	ns
		High-level data ^o		20†	High-level data ^o		20†	
		Low-level data ^o		20†	Low-level data ^o		20†	
		Clear inactive-state		20†	Clear inactive-state		20†	
		Data select		10†	Data select		10†	
t_h	Hold time	Data ^o		2.0†	Data ^o		2.0†	ns
T_A	Operating free-air temperature	−55		125	0		70	°C

^o Data includes the two serial inputs and the eight input/output data lines.

† The arrow indicates that the rising edge of the clock pulse is used for reference.

3

TTL DEVICES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)*

PARAMETER	TEST CONDITIONS†	SN54LS322A			SN74LS322A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	Q_A thru Q_H	2.4	3.2		2.4	3.1		V
	Q_H'	2.5	3.4		2.7	3.4		
V_{OL}	Q_A thru Q_H			0.25			0.25	V
	Q_H'			0.25			0.35	
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$			0.25			0.25	
	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$			0.25			0.35	
I_{OZH}	Q_A thru Q_H			40			40	μA
I_{OZL}	Q_A thru Q_H			-0.4			-0.4	mA
I_I	A thru H			0.1			0.1	mA
	Data select			0.2			0.2	
	Sign extend			0.3			0.3	
	Any other			0.1			0.1	
I_{IH}	A thru H, DS			40			40	μA
	Sign extend			60			60	
	Any other			20			20	
I_{IL}	Data select			-0.8			-0.8	mA
	Sign extend			-1.2			-1.2	
	Any other			-0.4			-0.4	
$I_{OS}§$	Q_A thru Q_H	-30		-130	-30		-130	mA
	Q_H'	-20		-100	-20		-100	
I_{CC}	$V_{CC} = \text{MAX}$	35	60		35	60		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	20	35		MHz
t_{PLH}	CLK	Q_H'	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		22	33	ns
t_{PHL}	CLK	Q_H'	See Note 2		26	35	
t_{PHL}	$\overline{\text{CLR}}$	Q_H'			27	35	ns
t_{PLH}	CLK	Q_A thru Q_H			16	25	ns
t_{PHL}	CLK	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 45 \text{ pF}$		22	33	
t_{PHL}	$\overline{\text{CLR}}$	Q_A thru Q_H	See Note 2		22	35	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A thru Q_H			15	35	ns
t_{PZL}	$\overline{\text{OE}}$	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 5 \text{ pF}$		15	25	
t_{PLZ}	$\overline{\text{OE}}$	Q_A thru Q_H	See Note 2		15	25	ns

¶ f_{max} = maximum clock frequency

t_{PZL} = output enable time to low level

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHZ} = output disable time from high level

t_{PHL} = propagation delay time, high-to-low-level output

t_{PLZ} = output disable time from low level

t_{PZH} = output enable time to high level

NOTE 2: For testing f_{max} , all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See General Information Section for load circuits and voltage waveforms.

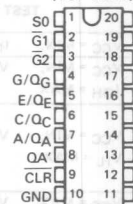
TYPES SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

OCTOBER 1976 - REVISED APRIL 1985

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
Hold (Store) Shift Left
Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Typical Power Dissipation . . . 175 mW
- Guaranteed Shift (Clock) Frequency . . . 25 MHz
- Applications:
Stacked or Push-Down Registers,
Buffer Storage, and
Accumulator Registers
- SN54LS299 and SN74LS299 Are Similar
But Have Direct Overriding Clear

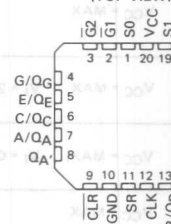
SN54LS323 . . . J PACKAGE
SN74LS323 . . . DW, J OR N PACKAGE

(TOP VIEW)



SN54LS323 . . . FK PACKAGE
SN74LS323

(TOP VIEW)



description

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

FUNCTION TABLE

MODE	CLR	INPUTS					INPUTS/OUTPUTS										OUTPUTS	
		FUNCTION SELECT	OUTPUT CONTROL		CLK	SERIAL		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A ¹	Q _H ¹	
			S1	S0		G1 ¹	G2 ¹											SL
Clear	L	X	L	L	L	†	X	X	L	L	L	L	L	L	L	L	L	
	L	L	X	L	L	†	X	X	L	L	L	L	L	L	L	L	L	
	L	H	H	X	X	†	X	X	X	X	X	X	X	X	X	L	L	
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	
Shift Right	H	L	H	L	L	†	X	H	Q _{A_n}	Q _{B_n}	Q _{C_n}	Q _{D_n}	Q _{E_n}	Q _{F_n}	Q _{G_n}	H	Q _{B_n}	
	H	L	H	L	L	†	X	L	Q _{A_n}	Q _{B_n}	Q _{C_n}	Q _{D_n}	Q _{E_n}	Q _{F_n}	Q _{G_n}	L	Q _{G_n}	
Shift Left	H	H	L	L	L	†	H	X	Q _{B_n}	Q _{C_n}	Q _{D_n}	Q _{E_n}	Q _{F_n}	Q _{G_n}	Q _{H_n}	H	Q _{B_n}	
	H	H	L	L	L	†	L	X	Q _{B_n}	Q _{C_n}	Q _{D_n}	Q _{E_n}	Q _{F_n}	Q _{G_n}	Q _{H_n}	L	Q _{H_n}	
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	

[†]When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

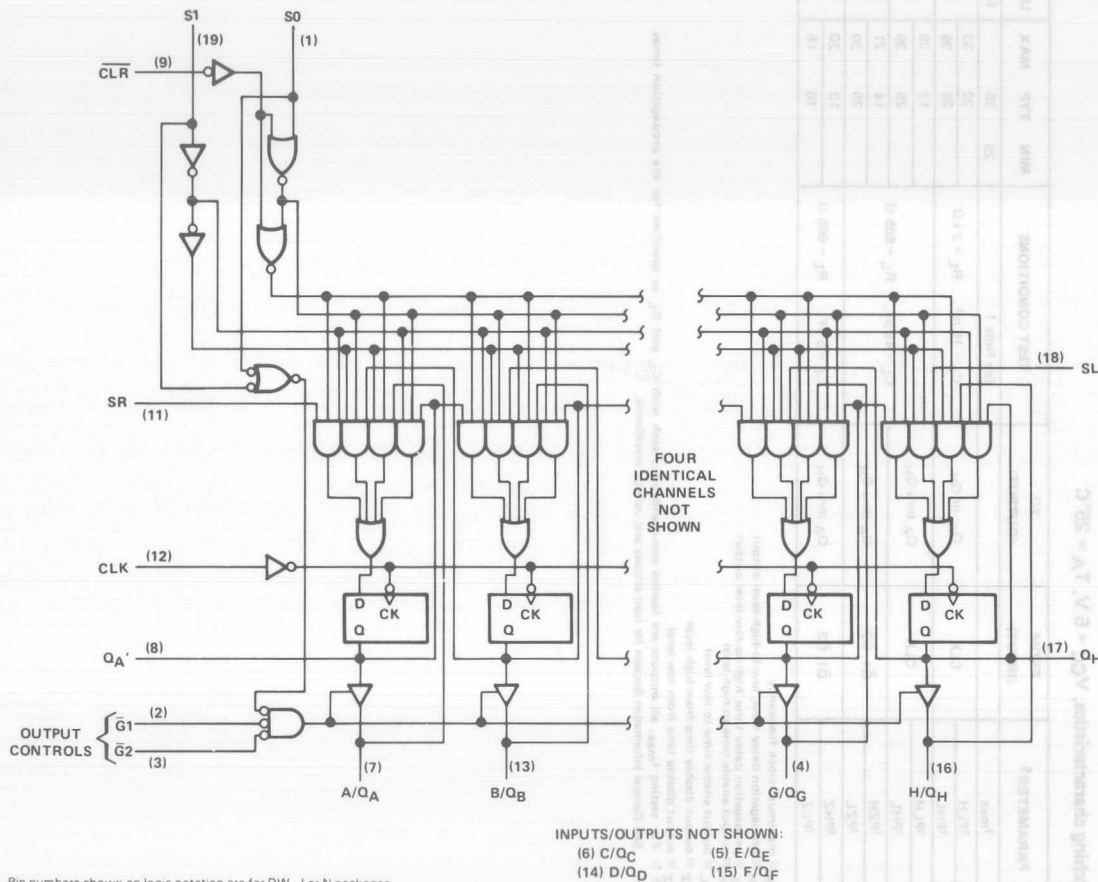
a . . . h the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

3

TTL DEVICES

TYPES SN64LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

logic diagram



TTL DEVICES

3

TYPES SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

Same as SN54LS299 and SN74LS299, except t_{SU} (Clear inactive) does not apply.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 1	25	35		MHz
t_{PLH}	CLK	Q_A or Q_H	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$		22	33	ns
t_{PHL}		Q_A or Q_H			26	39	
t_{PLH}	CLK	Q_A thru Q_H	$C_L = 45\text{ pF}$, $R_L = 665\ \Omega$		17	25	ns
t_{PHL}		Q_A thru Q_H			25	39	
t_{PZH}	\bar{G}_1, \bar{G}_2	Q_A thru Q_H	$C_L = 45\text{ pF}$, $R_L = 665\ \Omega$		14	21	ns
t_{PZL}	\bar{G}_1, \bar{G}_2	Q_A thru Q_H			20	30	
t_{PHZ}	\bar{G}_1, \bar{G}_2	Q_A thru Q_H	$C_L = 5\text{ pF}$, $R_L = 665\ \Omega$		10	20	ns
t_{PLZ}	\bar{G}_1, \bar{G}_2	Q_A thru Q_H			10	15	

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 1: For testing f_{max} , all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See General Information Section for load circuits and voltage waveforms.

3

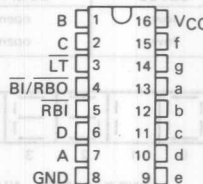
TTL DEVICES

TYPES SN54LS347, SN74LS347 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

D2426, NOVEMBER 1977—REVISED DECEMBER 1983

- Low-Voltage Version of SN54LS47/SN74LS47
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

SN54LS347 ... J OR W PACKAGE
SN74LS347 ... D, J OR N PACKAGE
(TOP VIEW)



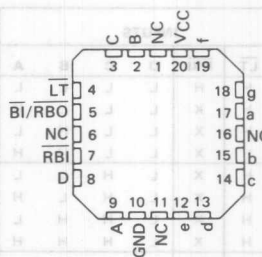
description

The 'LS347 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly. These circuits also have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on the next page. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The 'LS347 incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time when the BI/RBO node is at a high level. These devices also contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

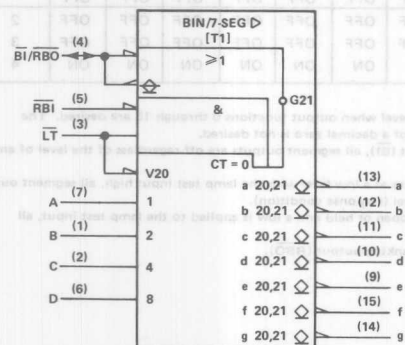
SN54LS347 ... FK PACKAGE
SN74LS347

(TOP VIEW)



NC - No internal connection

logic symbol†



Pin numbers shown on logic notation are for D, J or N packages.

PRODUCTION DATA
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TEXAS
INSTRUMENTS

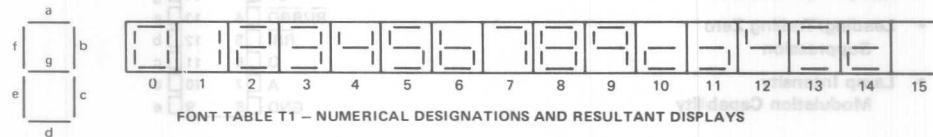
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TTL DEVICES

3-839

TYPES SN54LS347, SN74LS347 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

TYPE	DRIVER OUTPUTS				TYPICAL
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	POWER DISSIPATION
SN54LS347	low	open-collector	12 mA	7 V	35 mW
SN74LS347	low	open-collector	24 mA	7 V	35 mW



FONT TABLE T1 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

SEGMENT IDENTIFICATION

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						$\overline{\text{BI}}/\text{RBO}^\dagger$	OUTPUTS							NOTE
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
$\overline{\text{LT}}$	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

- NOTES:
- The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input ($\overline{\text{RBI}}$) must be open or high if blanking of a decimal zero is not desired.
 - When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are off regardless of the level of any other input.
 - When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output ($\overline{\text{RBO}}$) goes to a low level (response condition).
 - When the blanking input/ripple blanking output ($\overline{\text{BI}}/\text{RBO}$) is open or held and a low is applied to the lamp test input, all segment outputs are on.

$^\dagger \overline{\text{BI}}/\text{RBO}$ is wire AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$).

3 TTL DEVICES

TYPES SN54LS347, SN74LS347

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_W \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off-state	1 mA
Operating free-air temperature range: SN54LS347	-55°C to 125°C
SN74LS347	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS347			SN74LS347			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
$V_{O(off)}$	Off-state output voltage	a thru g			7			7	V
$I_{O(on)}$	On-state output current	a thru g			12			24	mA
I_{OH}	High-level output current	BI/RBO			-50			-50	μA
I_{OL}	Low-level output current	BI/RBO			1.6			3.2	mA
T_A	Operating free-air temperature		-55		125	0		70	$^\circ\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS347			SN74LS347			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					-1.5			-1.5	V
V_{OH}	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -50 \mu\text{A}$			2.4	4.2		2.4	4.2		V
V_{OL}	BI/RBO	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 1.6 \text{ mA}$			0.25	0.4		0.25	0.4	V
			$I_{OL} = 3.2 \text{ mA}$						0.35	0.5	
$I_{O(off)}$	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{O(off)} = 7 \text{ V}$					0.25			0.25	mA
$V_{O(on)}$	a thru g	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{O(on)} = 12 \text{ mA}$			0.25	0.4		0.25	0.4	V
			$I_{O(on)} = 24 \text{ mA}$						0.35	0.5	
I_I		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$					0.1			0.1	mA
I_{IH}		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$					20			20	μA
I_{IL}	Any input except BI/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.4			-0.4		mA
	BI/RBO					-1.2			-1.2		
I_{OS}	BI/RBO	$V_{CC} = \text{MAX}$			-0.3		-2	-0.3		-2	mA
I_{CC}		$V_{CC} = \text{MAX}, \text{ See Note 2}$				7	13		7	13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off} Turn-off time from A input	$R_L = 665 \Omega, C_L = 15 \text{ pF}$ See Note 3			100	ns
t_{on} Turn-on time from A input				100	ns
t_{off} Turn-off time from RBI input				100	ns
t_{on} Turn-on time from RBI input				100	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms, t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL} .

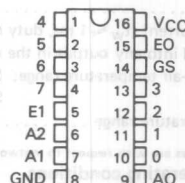
TYPES SN54LS348, SN74LS348 (TIM9908) 8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

OCTOBER 1976—REVISED DECEMBER 1983

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
N-Bit Encoding
Code Converters and Generators
- Typical Data Delay . . . 15 ns
- Typical Power Dissipation . . . 60 mW

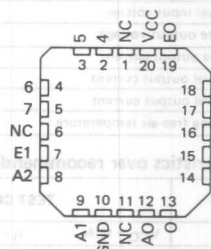
SN54LS348 . . . J OR W PACKAGE
SN74LS348 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS348 . . . FK PACKAGE
SN74LS348

(TOP VIEW)



NC - No internal connection

description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output EO) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.

FUNCTION TABLE

	INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance state

3 TTL DEVICES

PARAMETER	TEST CONDITIONS		UNIT
	MIN	TYP	
t _{PLH} Turn-on time from A input	100		ns
	100		ns
t _{PHL} Turn-off time from A input	100		ns
	100		ns

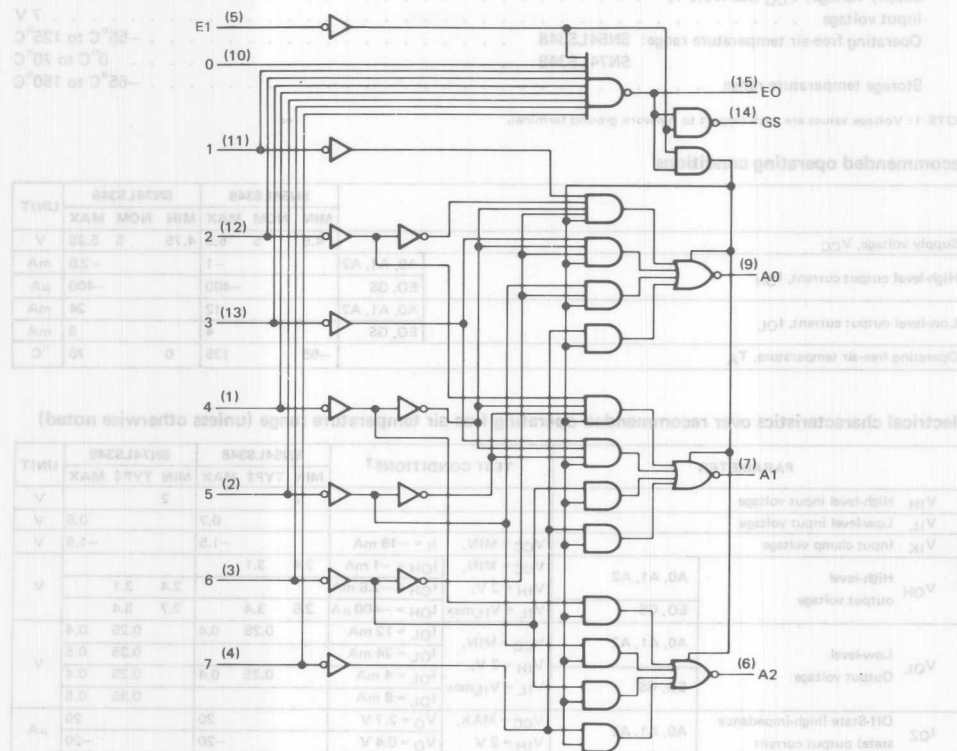
PRODUCTION DATA

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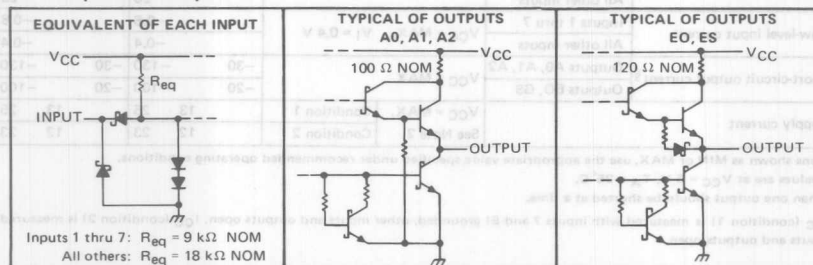
TEXAS
INSTRUMENTS

TYPES SN54LS348, SN74LS348 (TIM9908) 8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

logic diagram



schematic of inputs and outputs



TYPES SN54LS348, SN74LS348 (TIM9908)

8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS348	-55°C to 125°C
SN74LS348	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS348			SN74LS348			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	A0, A1, A2			-1			-2.6	mA
	EO, GS			-400			-400	μ A
Low-level output current, I_{OL}	A0, A1, A2			12			24	mA
	EO, GS			4			8	mA
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS348		SN74LS348		UNIT
				MIN	TYP‡	MAX	MIN	
V_{IH}	High-level input voltage			2			2	V
V_{IL}	Low-level input voltage					0.7		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5		V
V_{OH}	High-level output voltage	A0, A1, A2	$V_{CC} = \text{MIN}, I_{OH} = -1 \text{ mA}$	2.4	3.1			V
		EO, GS	$V_{IH} = 2 \text{ V}, I_{OH} = -2.6 \text{ mA}$			2.4	3.1	
V_{OL}	Low-level output voltage	A0, A1, A2	$V_{IL} = V_{ILmax}, I_{OH} = -400 \mu\text{A}$	2.5	3.4	2.7	3.4	V
			$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4	
		EO, GS	$V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}$			0.35	0.5	
			$V_{IL} = V_{ILmax}, I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	
I_{OZ}	Off-State (high-impedance state) output current	A0, A1, A2	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}$			20	20	μ A
			$V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$			-20	-20	
I_I	Input current at maximum input voltage	Inputs 1 thru 7	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.2	0.2	mA
		All other inputs				0.1	0.1	
I_{IH}	High-level input current	Inputs 1 thru 7	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			40	40	μ A
		All other inputs				20	20	
I_{IL}	Low-level input current	Inputs 1 thru 7	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8	-0.8	mA
		All other inputs				-0.4	-0.4	
I_{OS}	Short-circuit output current§	Outputs A0, A1, A2	$V_{CC} = \text{MAX}$	-30	-130	-30	-130	mA
		Outputs EO, GS		-20	-100	-20	-100	
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{Condition 1}$		13	25	13	25	mA
		See Note 2, Condition 2		12	23	12	23	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open. I_{CC} (condition 2) is measured with all inputs and outputs open.

3

TTL DEVICES

TYPES SN54LS348, SN74LS348 (TIM9908)

8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
tPLH	1 thru 7	A0, A1, or A2	In-phase output	CL = 45 pF, RL = 667 Ω, See Note 3		11	17	ns	
tPHL						20	30		
tPLH			Out-of-phase output			23	35	ns	
tPHL						23	35		
tPZH	EI	A0, A1, or A2				25	39	ns	
tPZL						24	41		
tPLH	0 thru 7	EO	Out-of-phase output		CL = 15 pF RL = 2 kΩ, See Note 3		11	18	ns
tPHL							26	40	
tPLH	0 thru 7	GS	In-phase output			38	55	ns	
tPHL						9	21		
tPLH	EI	GS	In-phase output			11	17	ns	
tPHL						14	36		
tPLH	EI	EO	In-phase output			17	26	ns	
tPHL						25	40		
tPHZ	EI	A0, A1, or A2		CL = 5 pF RL = 667 Ω		18	27	ns	
tPLZ						23	35		

[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPICAL APPLICATION DATA

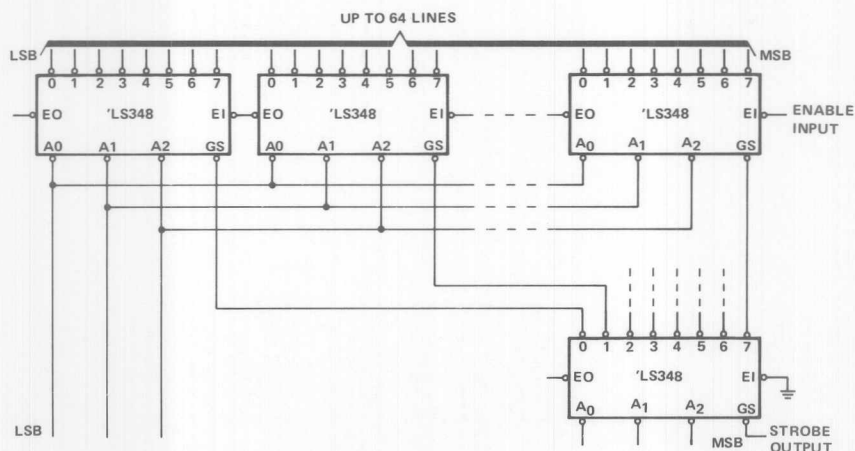


FIGURE 1—PRIORITY ENCODER WITH UP TO 64 INPUTS.

8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS TYPES SN74LS348, SN74ALS348 (LM9308)

Switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase	$C_L = 40 pF$ $R_L = 687 \Omega$ See Note 2	11	13	17	ns
t_{PHL}	1 thru 7	A0, A1, or A2	Out-of-phase		20	20	25	ns
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase		23	23	28	ns
t_{PHL}	1 thru 7	A0, A1, or A2	Out-of-phase		23	23	28	ns
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase		25	25	30	ns
t_{PHL}	1 thru 7	A0, A1, or A2	Out-of-phase		24	24	29	ns
t_{PLH}	0 thru 7	E0	In-phase	$C_L = 10 pF$ $R_L = 2 k\Omega$ See Note 3	11	13	17	ns
t_{PHL}	0 thru 7	E0	Out-of-phase		20	20	25	ns
t_{PLH}	0 thru 7	E0	Out-of-phase		23	23	28	ns
t_{PHL}	0 thru 7	E0	Out-of-phase		23	23	28	ns
t_{PLH}	0 thru 7	E0	Out-of-phase		25	25	30	ns
t_{PHL}	0 thru 7	E0	Out-of-phase		24	24	29	ns
t_{PLH}	0 thru 7	E0	In-phase	$C_L = 40 pF$ $R_L = 687 \Omega$	11	13	17	ns
t_{PHL}	0 thru 7	E0	Out-of-phase		20	20	25	ns
t_{PLH}	0 thru 7	E0	Out-of-phase		23	23	28	ns
t_{PHL}	0 thru 7	E0	Out-of-phase		23	23	28	ns
t_{PLH}	0 thru 7	E0	Out-of-phase		25	25	30	ns
t_{PHL}	0 thru 7	E0	Out-of-phase		24	24	29	ns

¹ t_{PLH} = propagation delay time, low to high-level output
 t_{PHL} = propagation delay time, high-level output
 t_{PLH} = output enable time to high level
 t_{PHL} = output enable time to low level
 t_{PLH} = output disable time from high level
 t_{PHL} = output disable time from low level
² t_{PLH} = output enable time from high level
³ t_{PHL} = output disable time from low level
 NOTE 3: See General Information Section for load circuit and voltage waveform

TYPICAL APPLICATION DATA

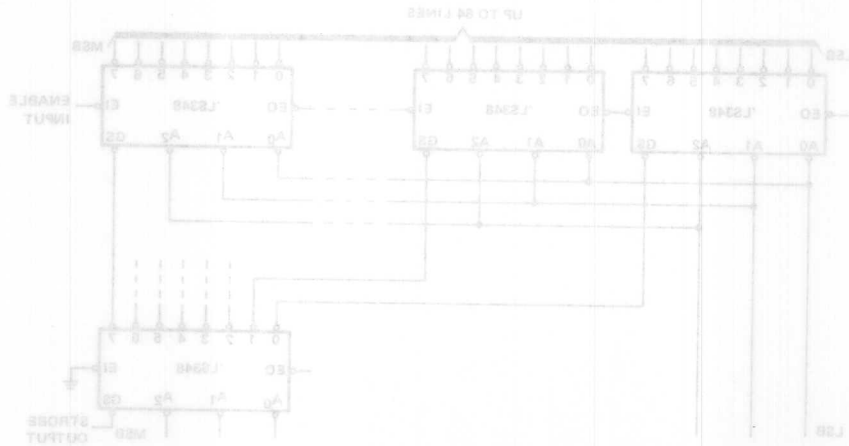


FIGURE 1—PRIORITY ENCODER WITH UP TO 64 INPUTS

3

TTL DEVICES

TYPES SN54LS352, SN74LS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

OCTOBER 1976 - REVISED DECEMBER 1983

- Inverting Versions of SN54LS153, SN74LS153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Typical Average Propagation Delay Times:
Data Input to Output . . . 15 ns
Strobe Input to Output . . . 19 ns
Select Input to Output . . . 22 ns
- Fully Compatible with most TTL Circuits
- Low Power Dissipation . . . 31 mW Typical (Enabled)

description

Each of these Schottky-clamped data selectors/-multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	\bar{G}	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

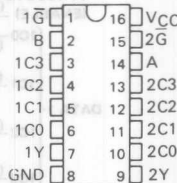
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS352	-55°C to 125°C
SN74LS352	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

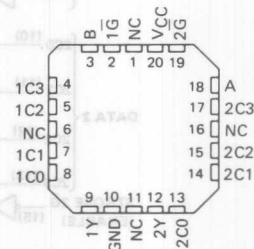
SN54LS352 . . . J OR W PACKAGE
SN74LS352 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS352 . . . FK PACKAGE
SN74LS352

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

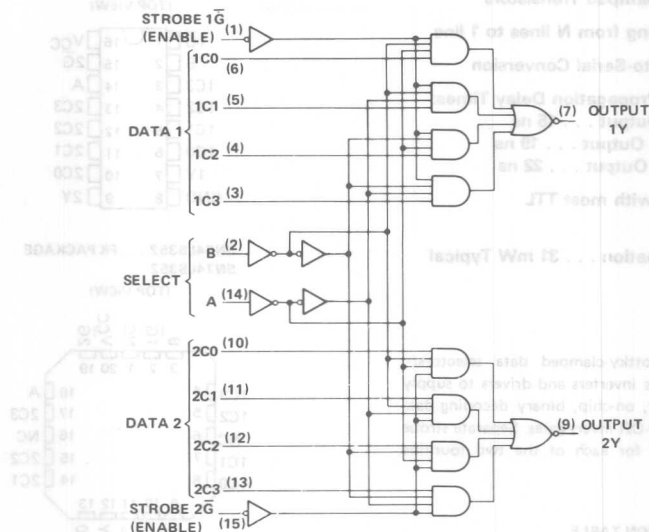
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TEXAS
INSTRUMENTS

3-847

TYPES SN54LS352, SN74LS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

logic diagram

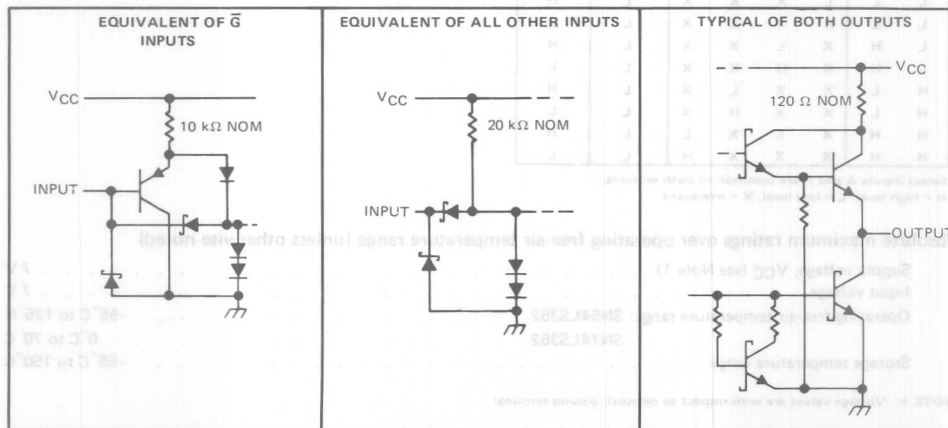


Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

schematics of inputs and outputs



TYPES SN54LS352, SN74LS352

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

		SN54LS352			SN74LS352			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS352			SN74LS352			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
						0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	\bar{G}			-0.2			-0.2	mA
	All other			-0.4			-0.4	mA
I _{OS} ‡	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC} ‡	V _{CC} = MAX, See Note 2		6.2	10		6.2	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating.

All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Y	R _L = 2 kΩ, C _L = 15 pF, See Note 3		13	20	ns
t _{PHL}	Data	Y			17	26	ns
t _{PLH}	A or B	Y			19	29	ns
t _{PHL}	A or B	Y			25	38	ns
t _{PLH}	\bar{G}	Y			16	24	ns
t _{PHL}	\bar{G}	Y			21	32	ns

† t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS353, SN74LS353

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

WITH 3-STATE OUTPUTS

BULLETIN NO. DLS 12464, OCTOBER 1976—REVISED DECEMBER 1983

Inverting Versions of SN54LS253, SN74LS253

Schottky-Diode-Clamped Transistors

Permits Multiplexing from N lines to 1 line

Performs Parallel-to-Serial Conversion

Typical Average Propagation Delay Times:

Data Input to Output . . . 12 ns

Control Input to Output . . . 16 ns

Select Input to Output . . . 21 ns

Fully Compatible with most TTL Circuits

Low Power Dissipation . . . 35 mW Typical (Enabled)

Inverted Data

description

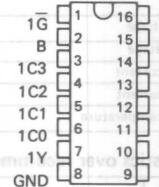
Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

SN54LS353 . . . J OR W PACKAGE

SN74LS353 . . . D, J OR N PACKAGE

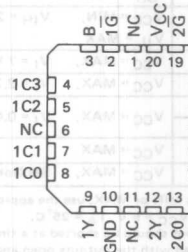
(TOP VIEW)



SN54LS353 . . . FK PACKAGE

SN74LS353

(TOP VIEW)



NC = No internal connection

3

TTL DEVICES

logic

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	\bar{G}	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

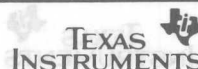
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS353	−55°C to 125°C
SN74LS353	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

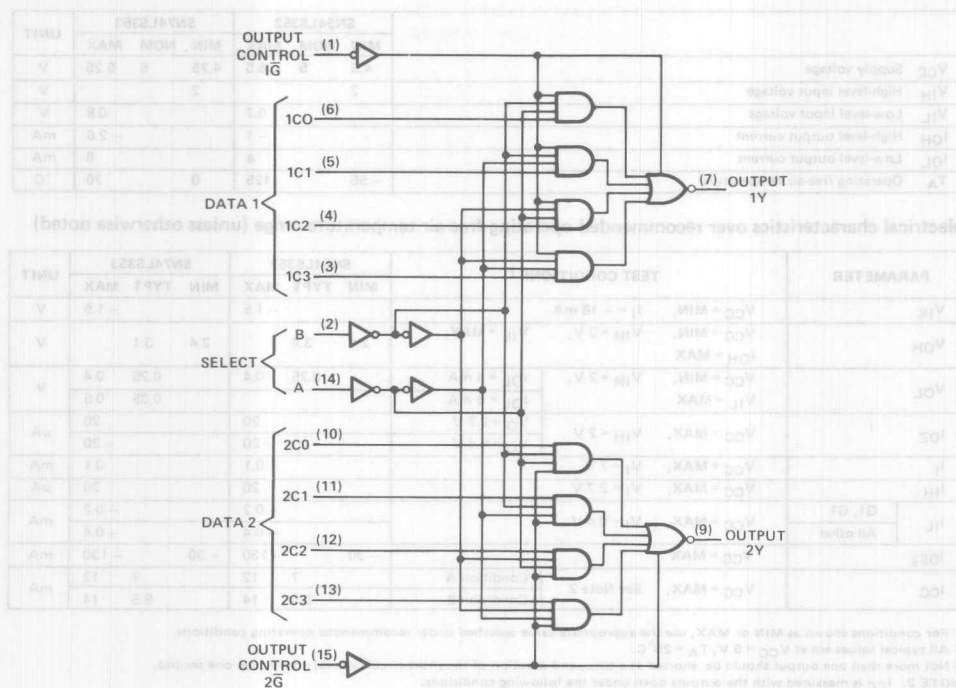
PRODUCTION DATA

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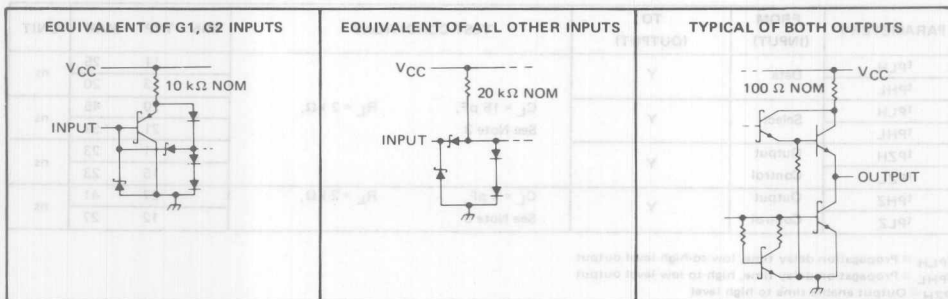
TYPES SN54LS353, SN74LS353 DUAL 4-LINE TO 1-LINE DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

schematic of inputs and outputs



TYPES SN54LS353, SN74LS353 **DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS** **WITH 3-STATE OUTPUTS**

recommended operating conditions

	SN54LS353			SN74LS353			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			− 1			− 2.6	mA
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54LS353			SN74LS353			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = − 18 mA			− 1.5			− 1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = MAX	2.4	3.4		2.4	3.1		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX			0.25 0.4			0.25 0.4	V
I _{OZ}		V _{CC} = MAX, V _{IH} = 2 V			20			20	μA
I _I		V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	G1, G1	V _{CC} = MAX, V _I = 0.4 V			− 0.2			− 0.2	mA
	All other								
I _{OS} §		V _{CC} = MAX	− 30		− 130	− 30		− 130	mA
I _{CC}		V _{CC} = MAX, See Note 2			7 12			7 12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Data	Y	C _L = 15 pF, See Note 3	R _L = 2 kΩ,		11	25	ns
t _{PHL}						13	20	
t _{PLH}	Select	Y				20	45	ns
t _{PHL}						21	32	
t _{PZH}	Output Control	Y	C _L = 5 pF, See Note 3	R _L = 2 kΩ,		11	23	ns
t _{PZL}						15	23	
t _{PHZ}	Output Control	Y				27	41	ns
t _{PLZ}						12	27	

¶ t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

t_{PLZ} = Output disable time from low level

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS354, SN54LS355, SN54LS356, SN54LS357, SN74LS354, SN74LS355, SN74LS356, SN74LS357 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

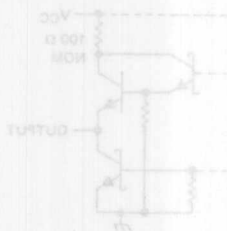
D2544, JULY 1979 — REVISED APRIL 1985

- Transparent Latches on Data Select Inputs
- Choice of Data Registers:
Transparent ('LS354, 'LS355)
Edge-Triggered ('LS356, 'LS357)
- Choice of Outputs:
Three-State ('LS354, 'LS356)
Open-Collector ('LS355, 'LS357)
- Complementary Outputs
- Easily Expandable
- High-Density 20-Pin Package

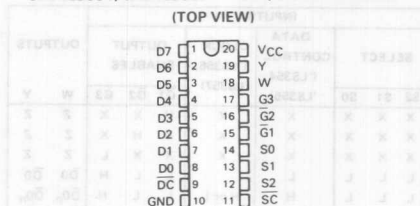
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select address is stored in transparent latches that are enabled by a low level on pin 11, SC. On the 'LS354 and 'LS355 a similar enable for data is obtained by a low level on pin 9, DC. The edge-triggered data registers of the 'LS356 and 'LS357 are clocked by a low-to-high transition on pin 9, CLK. Complementary outputs are available in either three-state versions ('LS354 and 'LS356) or open-collector versions ('LS355 and 'LS357).

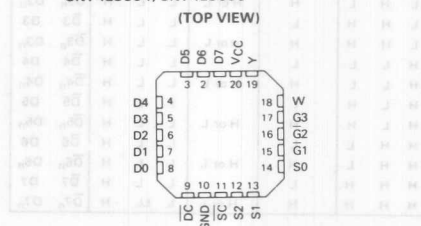
The SN54LS354 through SN54LS357 are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS354 through SN74LS357 are characterized for operation from 0°C to 70°C .



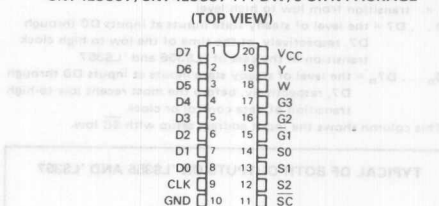
SN54LS354, SN54LS355 ... J PACKAGE
SN74LS354, SN74LS355 ... DW, J OR N PACKAGE



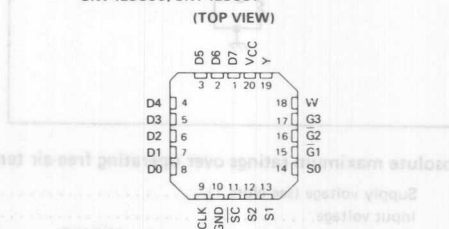
SN54LS354, SN54LS355 ... FK PACKAGE
SN74LS354, SN74LS355



SN54LS356, SN54LS357 ... J PACKAGE
SN74LS357, SN74LS357 ... DW, J OR N PACKAGE



SN54LS356, SN54LS357 ... FK PACKAGE
SN74LS356, SN74LS357



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**TYPES SN54LS354, SN54LS355, SN54LS356, SN54LS357,
SN74LS354, SN74LS355, SN74LS356, SN74LS357**
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

FUNCTION TABLE

SELECT			DATA CONTROL ('LS354, 'LS355)		CLOCK ('LS356, 'LS357)	OUTPUT ENABLES			OUTPUTS	
S2	S1	S0				G1	G2	G3	W	Y
X	X	X	X		X	H	X	X	Z	Z
X	X	X	X		X	X	H	X	Z	Z
X	X	X	X		X	X	X	L	Z	Z
L	L	L	L			L	L	H	D0	D0
L	L	L	L		H or L	L	L	H	D0 _n	D0 _n
L	L	L	L			L	L	H	D1	D1
L	L	L	L		H or L	L	L	H	D1 _n	D1 _n
L	L	L	L			L	L	H	D2	D2
L	L	L	L		H or L	L	L	H	D2 _n	D2 _n
L	L	L	L			L	L	H	D3	D3
L	L	L	L		H or L	L	L	H	D3 _n	D3 _n
L	L	L	L			L	L	H	D4	D4
L	L	L	L		H or L	L	L	H	D4 _n	D4 _n
L	L	L	L			L	L	H	D5	D5
L	L	L	L		H or L	L	L	H	D5 _n	D5 _n
L	L	L	L			L	L	H	D6	D6
L	L	L	L		H or L	L	L	H	D6 _n	D6 _n
L	L	L	L			L	L	H	D7	D7
L	L	L	L		H or L	L	L	H	D7 _n	D7 _n

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

Z = high-impedance state (off state)

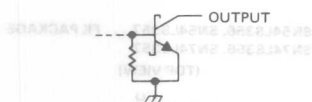
= transition from low to high level

D0...D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'LS356 and 'LS357

D0_n...D7_n = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock

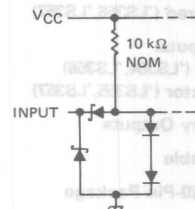
This column shows the input address setup with SC low.

TYPICAL OF BOTH OUTPUTS ON 'LS355 AND 'LS357

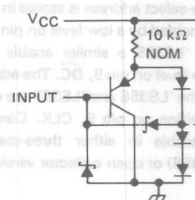


schematics of inputs and outputs

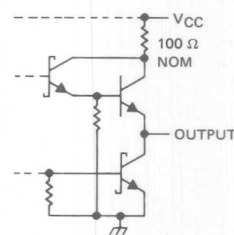
EQUIVALENT OF EACH DATA OR SELECT INPUT



EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF BOTH OUTPUTS ON 'LS354 AND 'LS356



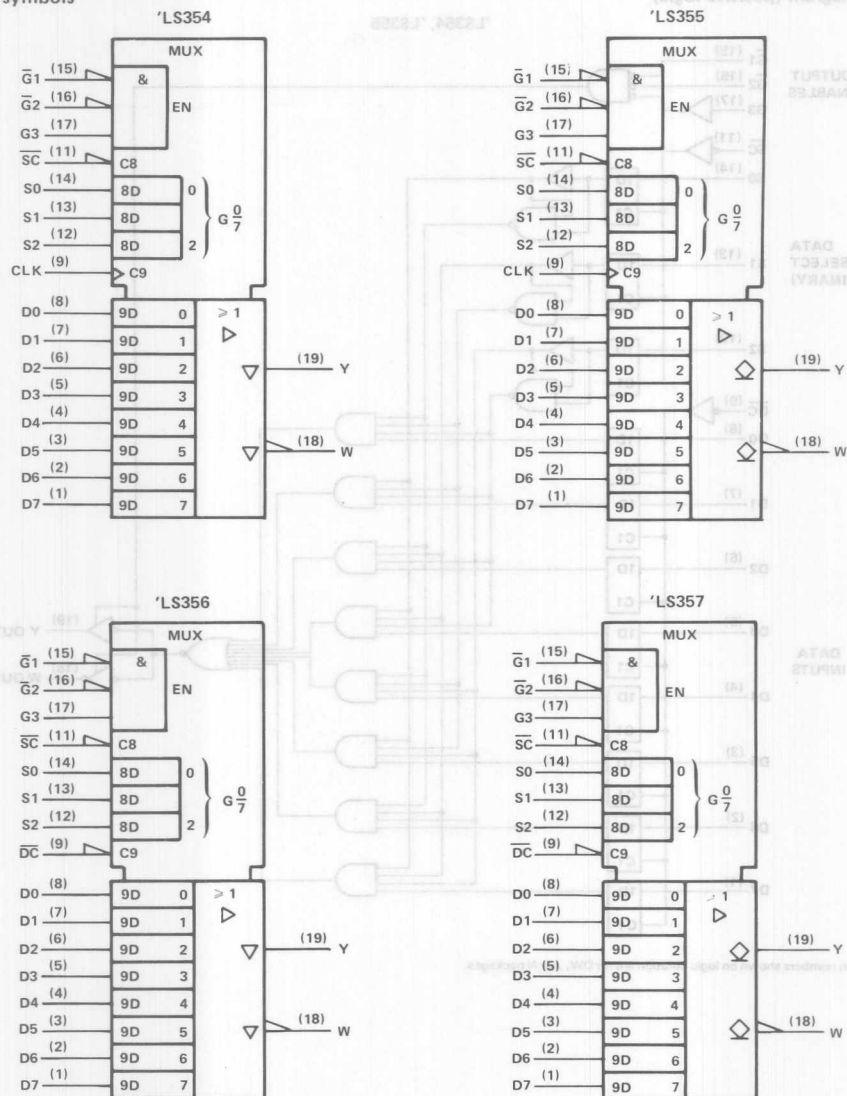
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54LS354, SN54LS355, SN54LS356, SN54LS357,
SN74LS354, SN74LS355, SN74LS356, SN74LS357
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

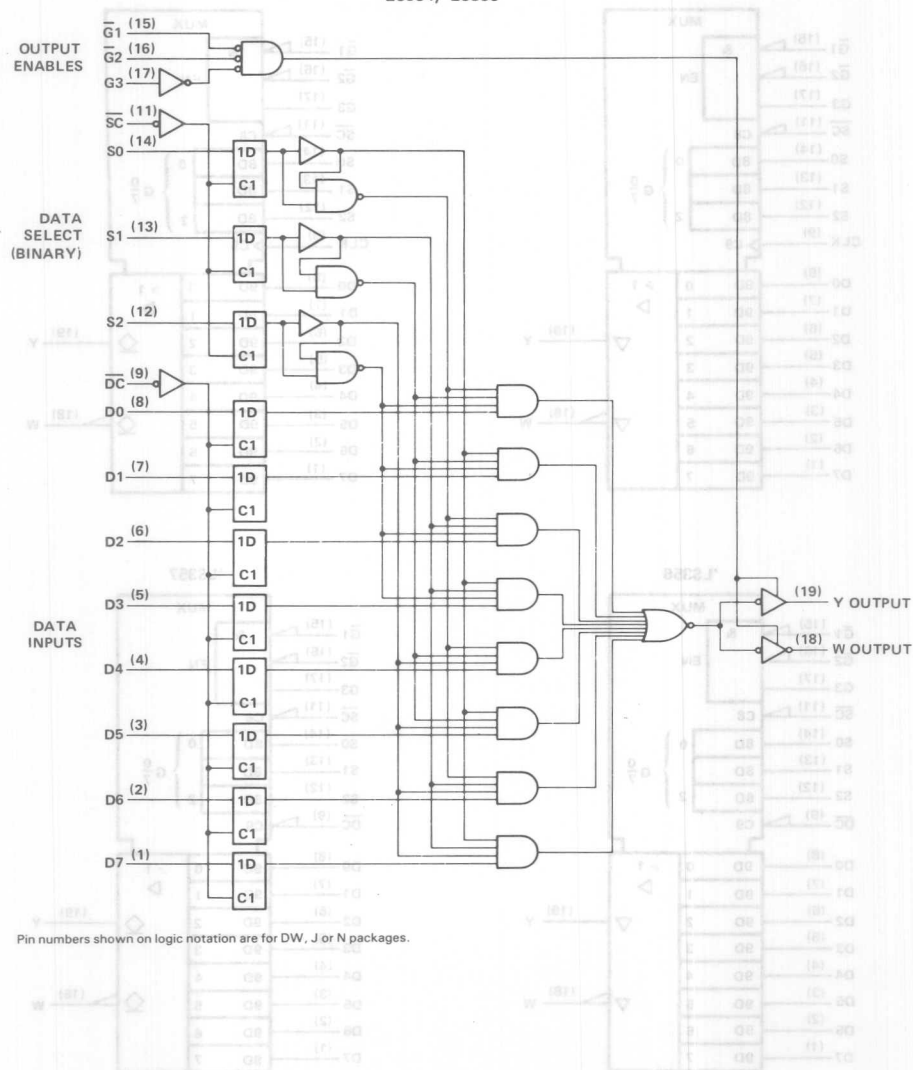
3

TTL DEVICES

TYPES SN54LS354, SN54LS355, SN74LS354, SN74LS355
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

logic diagram (positive logic)

'LS354, 'LS355



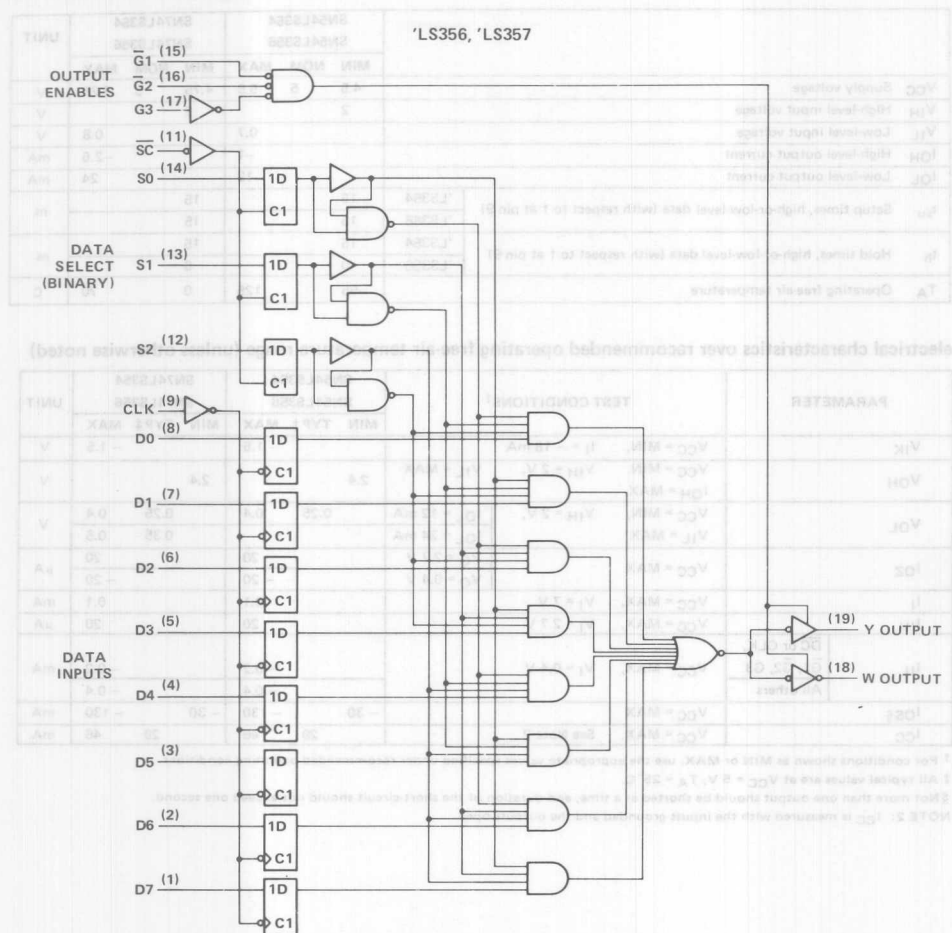
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS356, SN54LS357, SN74LS356, SN74LS357 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

logic diagram (positive logic)



3

TTL DEVICES

TYPES SN54LS354, SN54LS356, SN74LS354, SN74LS356
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS
WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54LS354 SN54LS356			SN74LS354 SN74LS356			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_{su}	Setup times, high-or-low-level data (with respect to t at pin 9)	'LS354	15		15			ns
		'LS356	15		15			
t_h	Hold times, high-or-low-level data (with respect to t at pin 9)	'LS354	15		15			ns
		'LS356	0		0			
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS354 SN54LS356			SN74LS354 SN74LS356			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4			2.4			V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$		$I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	0.25 0.4		0.25 0.35	0.4 0.5	V
I_{OZ}	$V_{CC} = \text{MAX}$		$V_O = 2.7 \text{ V}$ $V_O = 0.4 \text{ V}$	20 -20			20 -20	µA
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	DC or CLK, G1, G2, G3 All others		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.2 -0.4			-0.2 -0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-30		-130	-30		-130	mA
I_{CC}	$V_{CC} = \text{MAX}$, See Note 2		29	46		29	46	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

3

TTL DEVICES

TYPES SN54LS354, SN54LS356, SN74LS354, SN74LS356
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS
WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 667\ \Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS354			'LS356			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D0-D7	Y	$C_L = 45\text{ pF}$, See Note 3	24	36					ns
t_{PHL}				23	35					
t_{PLH}		W		18	27					ns
t_{PHL}	\overline{DC} or CLK	Y		29	44					
t_{PLH}				28	42	18	27			ns
t_{PHL}		W		26	39	33	50			
t_{PLH}	S0, S1 S2	Y		22	33	24	36			ns
t_{PHL}				33	50	18	27			
t_{PLH}		W		29	44	30	45			ns
t_{PHL}	SC	Y		24	45	28	48			
t_{PLH}				28	42	36	54			ns
t_{PHL}		W		34	51	30	45			
t_{PLH}	$\overline{G1}, \overline{G2}$	Y	$C_L = 5\text{ pF}$, See Note 3	34	51	36	54			ns
t_{PHL}				31	47	40	60			
t_{PLH}		W		27	41	32	48			ns
t_{PHL}	G3	Y		40	60	36	54			
t_{PZH}				14	27	14	25			ns
t_{PZL}		W		18	27	17	25			
t_{PHZ}		Y		15	25	16	24			ns
t_{PLZ}				15	25	16	24			
t_{PZH}		W		12	24	14	23			ns
t_{PZL}		Y	$C_L = 45\text{ pF}$, See Note 3	16	24	16	23			ns
t_{PHZ}				15	25	16	23			
t_{PLZ}		W		15	25	16	23			ns
t_{PHZ}		Y		15	29	15	27			ns
t_{PLZ}				19	29	18	27			
t_{PHZ}		W		15	25	16	25			ns
t_{PLZ}		Y	$C_L = 5\text{ pF}$, See Note 3	15	25	16	25			ns
t_{PHZ}				15	25	16	25			
t_{PLZ}		W		13	25	14	25			ns
t_{PHZ}		Y		17	25	16	25			ns
t_{PLZ}				15	25	16	25			
t_{PHZ}		W		15	25	16	25			ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS355, SN54LS357, SN74LS355, SN74LS357
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER		SN54LS355			SN74LS355			UNIT
		SN54LS357			SN74LS357			
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			12			24	mA
t _{su}	Setup times, high-or-low-level data, (with respect to f at pin 9)	'LS355	15		15			ns
		'LS357	15		15			
t _h	Hold times, high-or low-level data (with respect to f at pin 9)	'LS355	15		15			ns
		'LS357	0		0			
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS355			SN74LS355			UNIT
				SN54LS357			SN74LS357			
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA				-1.5			-1.5	V
I _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX V _{OH} = 5.5 V				0.1			0.1	mA
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OL} = 12 mA	0.25	0.4	0.25	0.4		V
				I _{OL} = 24 mA			0.35	0.5		
I _I		V _{CC} = MAX, V _I = 7 V				0.1			0.1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V				20			20	μA
I _{IL}	DC or CLK, G ₁ , G ₂ , G ₃	V _{CC} = MAX, V _I = 0.4 V				-0.2			-0.2	mA
	All others					-0.4			-0.4	
I _{CC}		V _{CC} = MAX, See Note 2			29	46		29	46	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

3

TTL DEVICES

TYPES SN54LS355, SN54LS357, SN74LS355, SN74LS357
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 667\ \Omega$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS355			'LS357			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
tPLH	D0-D7	Y	CL = 45 pF, See Note 3	34	41					ns	
tPHL				26	39						
tPLH		W			30	45					ns
tPHL					33	50					
tPLH	DC or CLK	Y			38	57		27	41	ns	
tPHL				31	47		34	51			
tPLH		W			33	50		32	48	ns	
tPHL					39	59		23	35		
tPLH	S0, S1, S2	Y			39	59		38	57	ns	
tPHL				36	49		40	60			
tPLH		W			32	48		38	57	ns	
tPHL					39	58		35	53		
tPLH	SC	Y			45	68		44	66	ns	
tPHL				42	63		41	62			
tPLH		W			44	66		41	62	ns	
tPHL					45	68		41	62		
tPHL	G1, G2	Y			21	32		18	27	ns	
tPHL				22	33		18	27			
tPLH		W			18	27		20	30	ns	
tPHL					19	29		21	32		
tPLH	G3	Y			24	36		24	36	ns	
tPHL				25	40		24	36			
tPLH		W			19	31		19	31	ns	
tPHL					19	29		19	29		

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS WITH OPEN-COLLECTOR OUTPUTS TYPE5 SN74L335, SN74L336, SN74L337, SN74L338, SN74L339

Switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 80\text{ k}\Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	UNIT
PROP. DELAY	000	Y	See Table 3 $C_L = 45\text{ pF}$	ns
		W		ns
		Y		ns
SETUP TIME	00	Y		ns
		W		ns
		Y		ns
HOLD TIME	00	Y		ns
		W		ns
		Y		ns
PROP. DELAY	01, 02	Y		ns
		W		ns
		Y		ns
SETUP TIME	01	Y		ns
		W		ns
		Y		ns
HOLD TIME	01	Y		ns
		W		ns
		Y		ns
PROP. DELAY	02	Y		ns
		W		ns
		Y		ns
SETUP TIME	02	Y		ns
		W		ns
		Y		ns
HOLD TIME	02	Y		ns
		W		ns
		Y		ns
PROP. DELAY	03	Y		ns
		W		ns
		Y		ns
SETUP TIME	03	Y		ns
		W		ns
		Y		ns
HOLD TIME	03	Y		ns
		W		ns
		Y		ns

NOTE 3: See General Information Section for load circuit and voltage waveforms

TYPES SN54365A THRU SN54368A, SN54LS365A THRU SN54LS368A SN74365A THRU SN74368A, SN74LS365A THRU SN74LS368A HEX BUS DRIVERS WITH 3-STATE OUTPUTS

REVISED DECEMBER 1983

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Choice of True or Inverting Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIP's
- Dependable Texas Instruments Quality and Reliability

'365A, '367A, 'LS365A, 'LS367A True Outputs
'366A, '368A, 'LS366A, 'LS368A Inverting Outputs

description

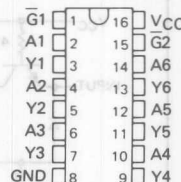
These Hex buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical \bar{G} (active-low control) inputs.

These devices feature high fan-out, improved fan-in, and can be used to drive terminated lines down to 133 ohms.

The SN54365A thru SN54368A and SN54LS365A thru SN54LS368A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74365A thru SN74368A and SN74LS365A thru SN74LS368A are characterized for operation from 0°C to 70°C .

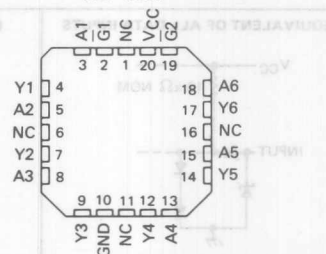
SN54365A, 366A, SN54LS365A, 366A ... J PACKAGE
SN74365A, 366A ... J OR N PACKAGE
SN74LS365A, SN74LS366A ... D, J OR N PACKAGE

(TOP VIEW)



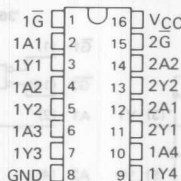
SN54LS365A, SN54LS366A ... FK PACKAGE
SN74LS365A, SN74LS366A

(TOP VIEW)



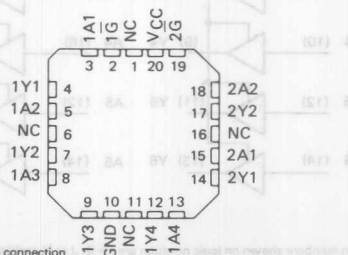
SN54367A, 368A, SN54LS367A, 368A ... J PACKAGE
SN74367A, 368A ... J OR N PACKAGE
SN74LS367A, SN74LS368A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS367A, SN54LS368A ... FK PACKAGE
SN74LS367A, SN74LS368A

(TOP VIEW)



NC - No internal connection

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-863

3

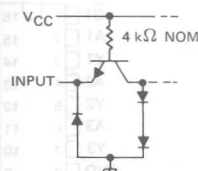
TTL DEVICES

TYPES SN54365A THRU SN54368A, SN54LS365A THRU SN54LS368A SN74365A THRU SN74368A, SN74LS365A THRU SN74LS368A HEX BUS DRIVERS WITH 3-STATE OUTPUTS

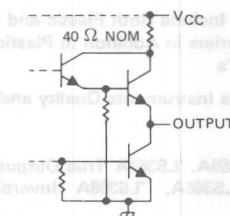
schematics of inputs and outputs

'365A thru '368A

EQUIVALENT OF ALL INPUTS

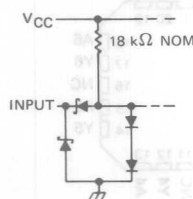


TYPICAL OF ALL OUTPUTS

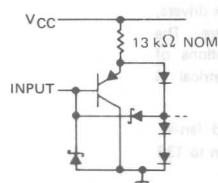


'LS365A thru 'LS368A

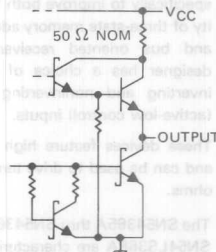
EQUIVALENT OF ALL DATA INPUTS



EQUIVALENT OF ALL G INPUTS



TYPICAL OF ALL OUTPUTS

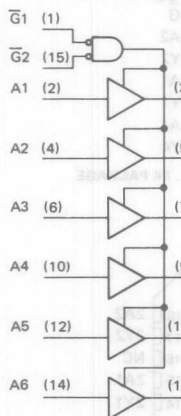


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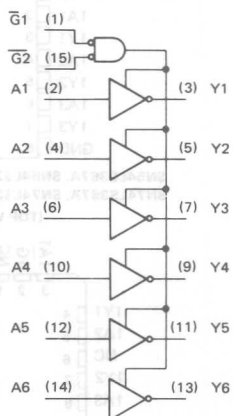
TTL DEVICES

logic diagrams (positive logic)

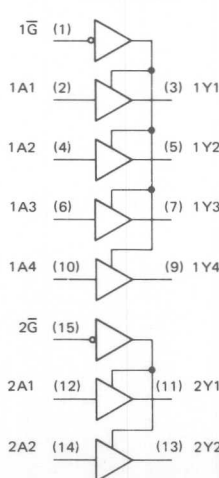
'365A, 'LS365A



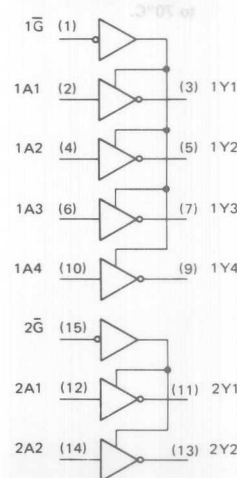
'366A, 'LS366A



'367A, 'LS367A



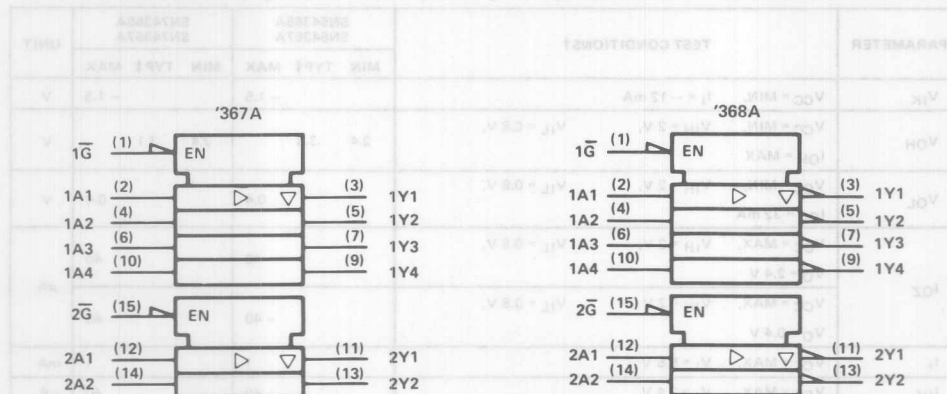
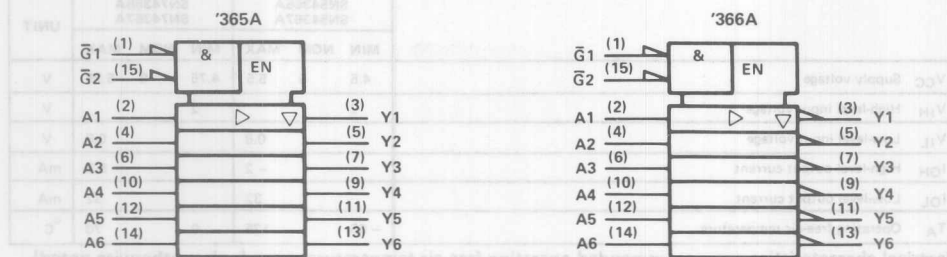
'368A, 'LS368A



Pin numbers shown on logic notation are for D, J or N packages.

**TYPES SN54365A THRU SN54368A, SN54LS365A THRU SN54LS368A
SN74365A THRU SN74368A, SN74LS365A THRU SN74LS368A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS**

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '365A, '366A, '367A, '368A	5.5 V
'LS365A, 'LS366A, 'LS367A, 'LS368A	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54365A, SN54367A
SN74365A, SN74367A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54365A SN54367A			SN74365A SN74367A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-2			-5.2	mA
I_{OL}	Low-level output current			32			32	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54365A SN54367A			SN74365A SN74367A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.3		2.4	3.1		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 32 \text{ mA}$			0.4			0.4	V
I_{OZ}	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 2.4 \text{ V}$			40			40	μA
	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 0.4 \text{ V}$			-40			-40	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	A Inputs $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}, \text{ Either } \bar{G} \text{ input at } 2 \text{ V}$			-40			-40	μA
	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}, \text{ Both } \bar{G} \text{ inputs at } 0.4 \text{ V}$			-1.6			-1.6	
	\bar{G} Inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40		-130	-40		-130	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ Data inputs} = 0 \text{ V}, \text{ Output controls} = 4.5 \text{ V}$	65		85	65		85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 50 \text{ pF}$			16	ns
t_{PHL}						22	ns
t_{PZH}						35	ns
t_{PZL}						37	ns
t_{PHZ}			$R_L = 400 \Omega, C_L = 5 \text{ pF}$			11	ns
t_{PLZ}						27	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

AT8C
A18C
TYPES SN54366A, SN54368A
SN74366A, SN74368A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	DESCRIPTION	SN54366A SN54368A			SN74366A SN74368A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-2			-5.2	mA
I_{OL}	Low-level output current			32			32	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54366A SN54368A			SN74366A SN74368A			UNIT
					MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.3		2.4	3.1		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 32 \text{ mA}$			0.4			0.4	V
I_{OZ}	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 2.4 \text{ V}$			40			40	μA
	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O = 0.4 \text{ V}$			-40			-40	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	A Inputs $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}, \text{Either } \bar{G} \text{ input at } 2 \text{ V}$			-40			-40	μA
	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}, \text{Both } \bar{G} \text{ inputs at } 0.4 \text{ V}$			-1.6			-1.6	
	\bar{G} Inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40	-130		-40	-130		mA
I_{CC}	$V_{CC} = \text{MAX}, \text{Data inputs} = 0 \text{ V}, \text{Output controls} = 4.5 \text{ V}$	59	77		59	77		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 50 \text{ pF}$			17	ns
t_{PHL}						16	ns
t_{PZH}						35	ns
t_{PZL}						37	ns
t_{PHZ}			$R_L = 400 \Omega, C_L = 5 \text{ pF}$			11	ns
t_{PLZ}						27	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

**TYPES SN54LS365A, SN54LS367A
SN74LS365A, SN74LS367A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS**

recommended operating conditions

PARAMETER	DESCRIPTION	SN54LS365A SN54LS367A			SN74LS365A SN74LS367A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS365A SN54LS367A			SN74LS365A SN74LS367A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = \text{MAX}$	2.4	3.3		2.4	3.1		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 24 \text{ mA}$					0.35	0.5	V
	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.4 \text{ V}$			20			20	μA
I_{OZ}	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	A Inputs $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-20			-20	μA
	A Inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
	\bar{G} Inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{Data inputs} = 0 \text{ V}, \text{Output controls} = 4.5 \text{ V}$		14	24		14	24	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

3

TTL DEVICES

**TYPES SN54LS365A, SN54LS367A
SN74LS365A, SN74LS367A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 667\ \Omega$, $C_L = 45\ \text{pF}$	10	16	ns	
t_{PHL}				9	22	ns	
t_{PZH}				19	35	ns	
t_{PZL}				24	40	ns	
t_{PHZ}			$R_L = 667\ \Omega$, $C_L = 5\ \text{pF}$	30	ns		
t_{PLZ}				35	ns		

NOTE 2: See General Information Section for load circuits and voltage waveforms.

**TYPES SN54LS366A, SN54LS368A
SN74LS366A, SN74LS368A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS**

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN74LS366A SN74LS368A			SN54LS366A SN54LS368A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS366A SN54LS368A			SN74LS366A SN74LS368A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.3		2.4	3.1		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_{OZ}	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_O = 2.4 \text{ V}$			20			20	μA
	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_O = 0.4 \text{ V}$			-20			-20	
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	A Inputs $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}, \text{ Either } \bar{G} \text{ input at } 2 \text{ V}$			-20			-20	μA
	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}, \text{ Both } \bar{G} \text{ inputs at } 0.4 \text{ V}$			-0.4			-0.4	
	\bar{G} Inputs $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ Data inputs} = 0 \text{ V}, \text{ Output controls} = 4.5 \text{ V},$		12	21		12	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

3

TTL DEVICES

TYPES SN54LS366A, SN54LS368A
SN74LS366A, SN74LS368A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$		7	15	ns
t_{PHL}					12	18	ns
t_{PZH}					18	35	ns
t_{PZL}					28	45	ns
t_{PHZ}			$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$			32	ns
t_{PLZ}						35	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

HEX BUS DRIVERS WITH 3-STATE OUTPUTS SN74ALS386A, SN74ALS386A TYPES SN74ALS386A, SN74ALS386A

Switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	VDD	Y	$R_L = 600 \Omega$, $C_L = 50 pF$	1	15	ns	
t_{PHL}				13	18	ns	
t_{FZH}				18	28	ns	
t_{FZL}			$R_L = 600 \Omega$, $C_L = 50 pF$	28	48	ns	
t_{RZL}				33	55	ns	
t_{RZH}				38	58	ns	

NOTE 2: See General Information section for load circuitry and voltage waveform.

3

TTL DEVICES

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975—REVISED APRIL 1985

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

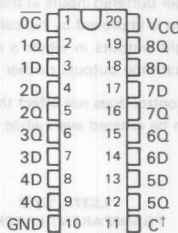
description

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

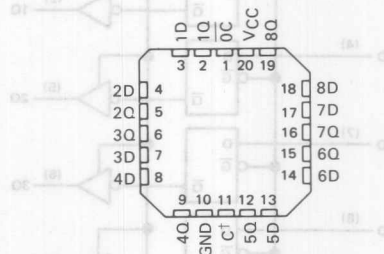
SN54LS373, SN54LS374, SN54S373,
SN54S374 ... J PACKAGE
SN74LS373, SN74LS374, SN74S373,
SN74S374 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS373, SN54LS374, SN54S373,
SN54S374, SN74LS373, SN74LS374,
SN74S373, SN74S374 ... FK PACKAGE

(TOP VIEW)



'C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

3

TTL DEVICES

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-873

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

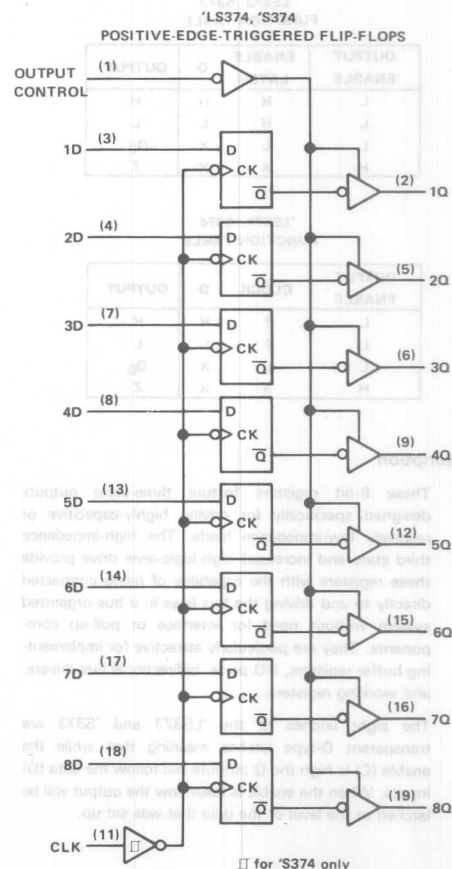
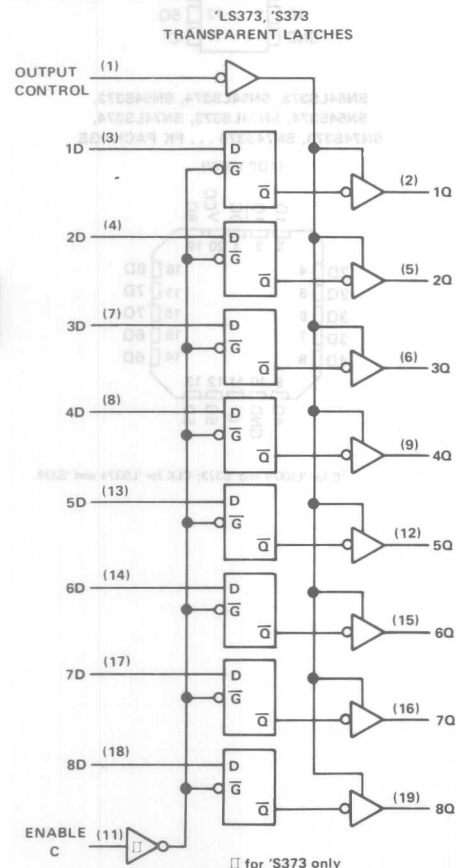
description (continued)

The eight flip flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

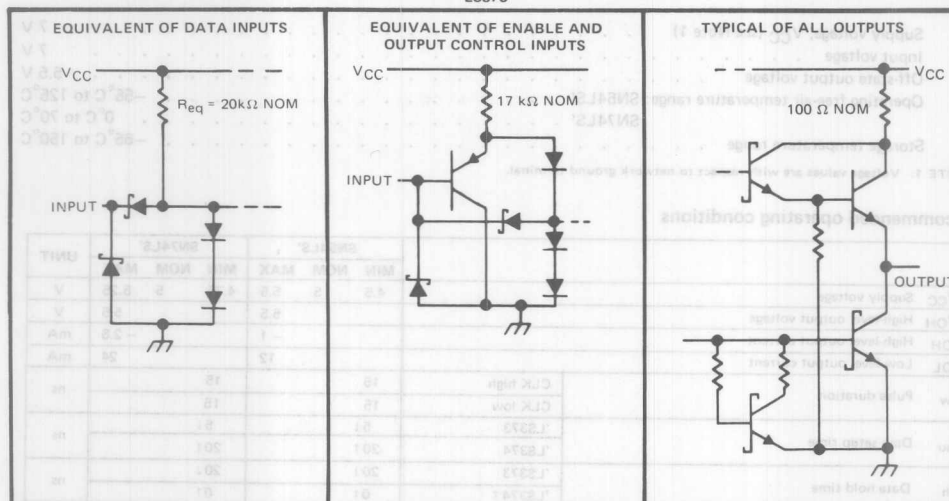
logic diagrams



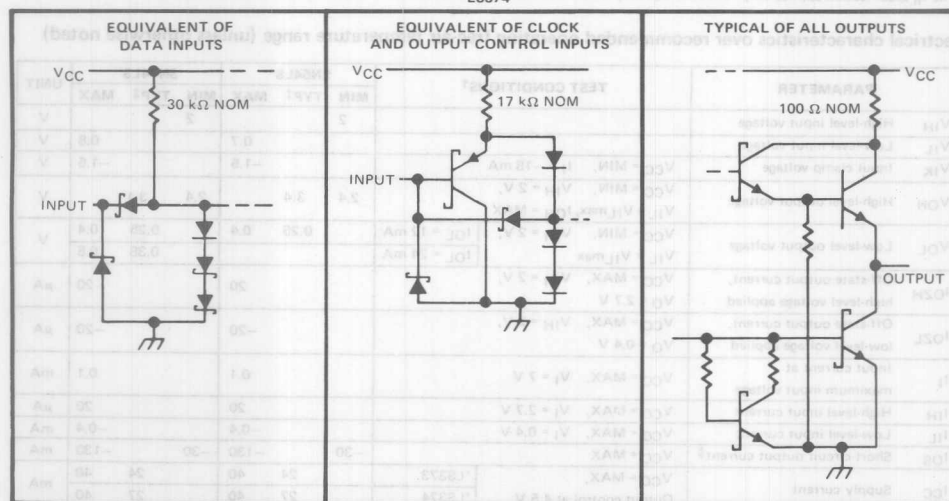
TYPES SN54LS373, SN54LS374, SN74LS373, SN74LS374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

schematic of inputs and outputs

'LS373



'LS374



3

TTL DEVICES

TYPES SN54LS373, SN54LS374, SN74LS373, SN74LS374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OH}	High-level output current			— 1			— 2.6	mA
I _{OL}	Low-level output current			12			24	mA
t _w	Pulse duration	CLK high		15	15			ns
		CLK low		15	15			
t _{su}	Data setup time	'LS373		5↓	5↓			ns
		'LS374		20†	20†			
t _h	Data hold time	'LS373		20↓	20↓			ns
		'LS374†		0†	0†			
T _A	Operating free-air temperature	— 55		125	0		70	°C

† The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage	0.7			0.8			V		
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5 V		
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OH} = MAX			2.4	3.4		2.4	3.1	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax}		I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
			I _{OL} = 24 mA			0.35	0.5			
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V			20			20 μA		
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-20			-20 μA		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1 mA		
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20 μA		
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4 mA		
I _{OS}	Short-circuit output current§	V _{CC} = MAX			-30	-130	-30	-130	mA	
I _{CC}	Supply current	V _{CC} = MAX,			'LS373	24	40	24	40	mA
		Output control at 4.5 V			'LS374	27	40	27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

3
TTL DEVICES

TYPES SN54LS373, SN54LS374, SN74LS373, SN74LS374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			'LS373			'LS374			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}			C _L = 45 pF, R _L = 667 Ω See Notes 2 and 3						35	50		MHz
t _{PLH}	Data	Any Q				12	18					
t _{PHL}						12	18					ns
t _{PLH}	Clock or enable	Any Q				20	30			15	28	
t _{PHL}						18	30			19	28	ns
t _{PZH}	Output	Any Q				15	28			20	26	
t _{PZL}	Control					25	36			21	28	ns
t _{PHZ}	Output Control	Any Q	C _L = 5 pF, R _L = 667 Ω See Note 3			SN54	28	32		28	32	
						SN74	15	25			15	28
t _{PLZ}	Output Control	Any Q					12	20		12	20	ns

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 t_{PZH} = output enable time to high level
 t_{PZL} = output enable time to low level
 t_{PHZ} = output disable time from high level
 t_{PLZ} = output disable time from low level

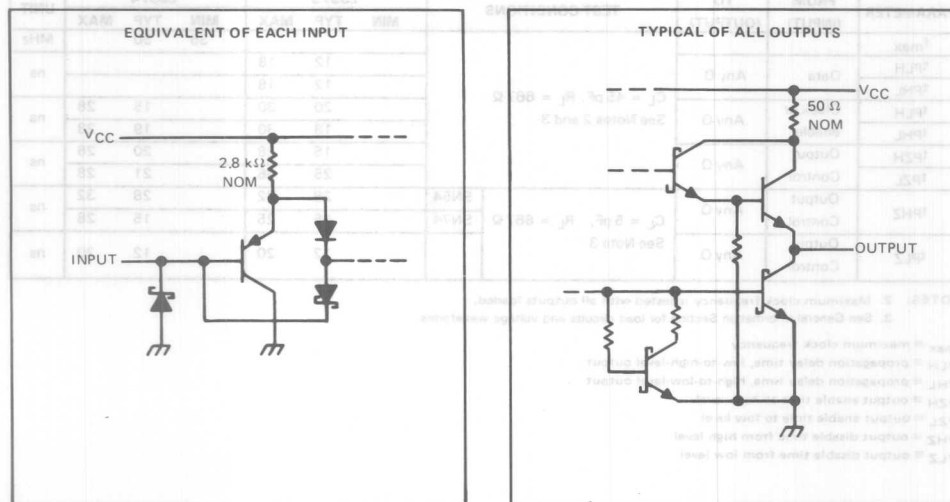
3

TTL DEVICES

UNIT	SN54LS373			SN54LS374			TEST CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage, V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	
Input voltage, V_{IH}	2.0	2.0	2.0	2.0	2.0	2.0	
Output voltage, V_{OH}	2.7	2.7	2.7	2.7	2.7	2.7	
Output current, I_{OH}	10	10	10	10	10	10	
Width of clock-enable pulse, t_{WE}	10	10	10	10	10	10	
Data setup time, t_{SU}	10	10	10	10	10	10	
Data hold time, t_{H}	10	10	10	10	10	10	
Operating temperature, T_A	-55	0	125	-55	0	125	

TYPES SN54S373, SN54S374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

schematic of inputs and outputs



3

TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S'	-55°C to 125°C
SN74S'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				-2			-6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{SU}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_H	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		-55		125	0		70	°C

TYPES SN54S373, SN54S374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT	
V _{IH}							2		V	
V _{IL}								0.8	V	
V _{IK}		V _{CC} = MIN, I _I = − 18 mA						− 1.2	V	
V _{OH}	SN54S'	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX				2.4	3.4		V	
	SN74S'					2.4	3.1			
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA						0.5	V	
I _{OZH}		V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V						50	μA	
I _{OZL}		V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V						− 50	μA	
I _I		V _{CC} = MAX, V _I = 5.5 V						1	mA	
I _{IH}		V _{CC} = MAX, V _I = 2.7 V						50	μA	
I _{IL}		V _{CC} = MAX, V _I = 0.5 V						− 250	μA	
I _{OS} §		V _{CC} = MAX						− 40	− 100	mA
I _{CC}	V _{CC} = MAX	'S373	outputs high						160	mA
			outputs low						160	
			outputs disabled						190	
		'S374	outputs high						110	
			outputs low						140	
			outputs disabled						160	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
f _{max}			C _L = 15 pF, R _L = 280 Ω, See Notes 2 and 4				75	100		MHz	
t _{PLH}	Data	Any Q			7	12					ns
t _{PHL}					7	12					
t _{PLH}	Clock or enable	Any Q			7	14		8	15		ns
t _{PHL}					12	18		11	17		
t _{PZH}	Output	Any Q	C _L = 5 pF, R _L = 280 Ω, See Note 3		8	15		8	15	ns	
t _{PZL}	Control				11	18		11	18		
t _{PHZ}	Output	Any Q			6	9		5	9	ns	
t _{PLZ}	Control				8	12		7	12		

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.

4. See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

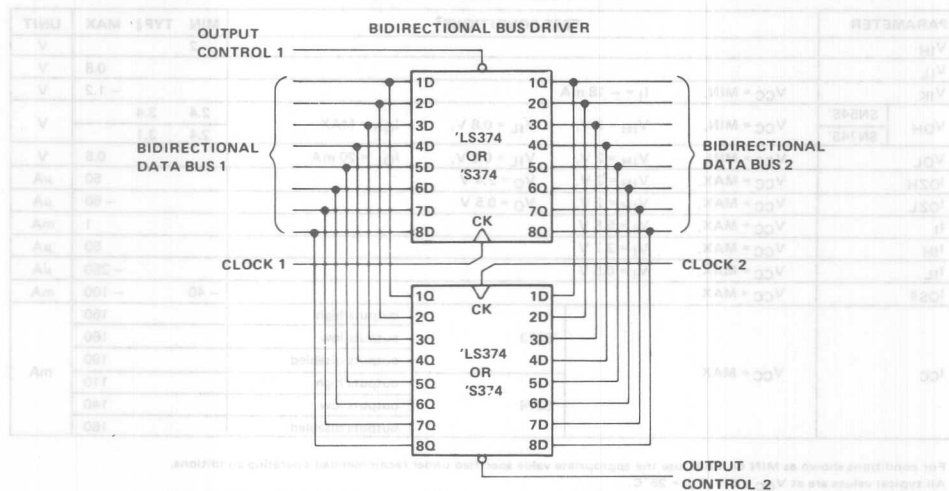
t_{PLZ} = output disable time from low level

3

TTL DEVICES

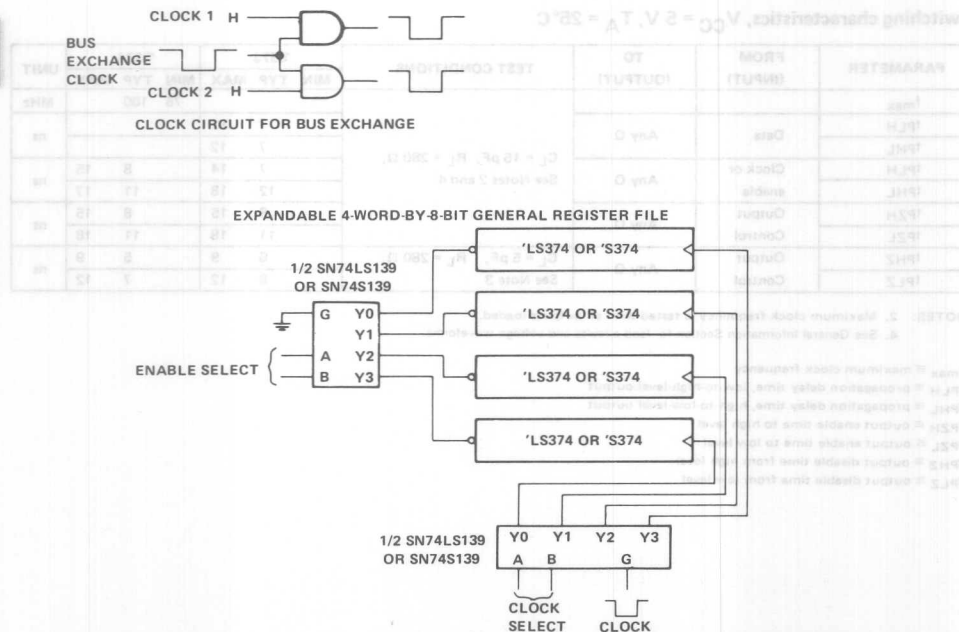
**TYPES SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

TYPICAL APPLICATION DATA



3

TTL DEVICES



TYPES SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

OCTOBER 1976—REVISED DECEMBER 1983

- Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

logic

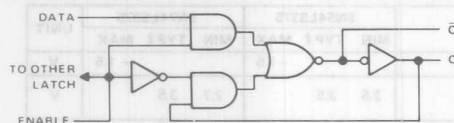
FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = high level, L = low level, X = irrelevant

Q_0 = the level of Q before the high-to-low transition of C.

logic diagram (each latch)



description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of -55°C to 125°C ; SN74LS375 is characterized for operation from 0°C to 70°C .

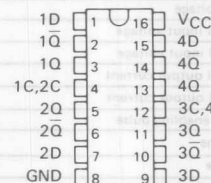
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS375	-55°C to 125°C
SN74LS375	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

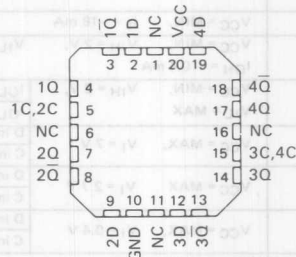
SN54LS375 ... J OR W PACKAGE
SN74LS375 ... D, J OR N PACKAGE

(TOP VIEW)



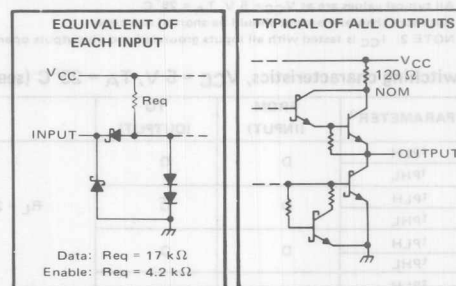
SN54LS375 ... FK PACKAGE
SN74LS375

(TOP VIEW)



NC = No internal connection

schematics of inputs and outputs



PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

recommended operating conditions

		SN54LS375			SN74LS375			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
t _w	Width of enabling pulse	20			20			ns
t _{setup}	Setup time	20			20			ns
t _{hold}	Hold time	0			0			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS375			SN74LS375			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX I _{OH} = -0.4 mA	2.5	3.5		2.7	3.5		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX I _{OL} = 4 mA		0.25	0.4		0.25	0.5	V
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS}	V _{CC} = MAX	-20		-100	-20		-100	mA
I _{CC}	V _{CC} = MAX, See Note 2	6.3	12		6.3	12		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER [◇]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	D	Q	R _L = 2 kΩ, C _L = 15 pF	15	27		ns
t _{PHL}	D	Q		9	17		
t _{PLH}	D	Q̄		12	20		ns
t _{PHL}	D	Q̄		7	15		
t _{PLH}	D	Q		15	27		ns
t _{PHL}	D	Q		14	25		
t _{PLH}	C	Q		16	30		ns
t _{PHL}	C	Q̄		7	15		

◇ t_{PLH} = propagation delay time, low-to-high-level output

◇ t_{PHL} = propagation delay time, high-to-low-level output

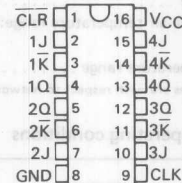
NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54376, SN74376 QUADRUPLE J-K FLIP-FLOPS

OCTOBER 1976—REVISED DECEMBER 1983

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Common Positive-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Fully Buffered Outputs
- Typical Clock Input Frequency . . . 45 MHz

SN54376 . . . J OR W PACKAGE
SN74376 . . . J OR N PACKAGE
(TOP VIEW)



description

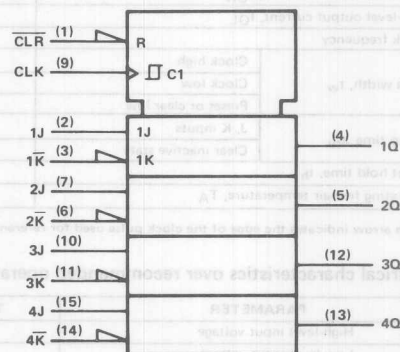
These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by as much as 50%. They feature hysteresis at the clock input, fully buffered outputs, and direct clear capability. The positive-edge-triggered SN54376 and SN74376 are directly compatible with most Series 54/74 MSI registers.

The SN54376 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74376 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE (EACH FLIP-FLOP)

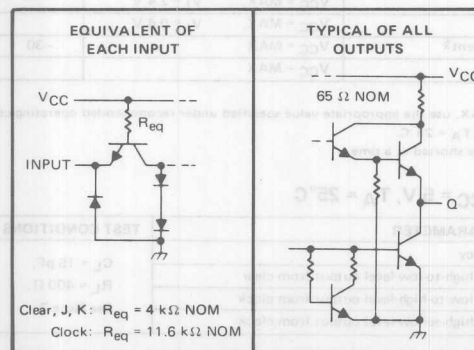
COMMON INPUTS		INPUTS		OUTPUT
CLEAR	CLOCK	J	\bar{K}	Q
L	X	X	X	L
H	↑	L	H	Q_0
H	↑	H	H	H
H	↑	L	L	L
H	↑	H	L	TOGGLE
H	L	X	X	Q_0

logic symbol†



Pin numbers shown on logic notation are for J or N packages.

schematics of inputs and outputs



Resistor values shown are nominal.

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TEXAS
INSTRUMENTS

TYPES SN54376, SN74376 QUADRUPLE J-K FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54376	–55°C to 125°C
SN74376	–0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54376			SN74376			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–800			–800	μ A
Low-level output current, I_{OL}				16			16	mA
Clock frequency		0		30	0		30	MHz
Pulse width, t_W	Clock high	22			22			ns
	Clock low	12			12			
	Preset or clear low	12			12			
Setup time, t_{SU}	J, K inputs	0†			0†			ns
	Clear inactive state	10†			10†			
Input hold time, t_H		20†			20†			ns
Operating free-air temperature, T_A		55		125	0		70	°C

† The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$				40	μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$				–1.6	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		–30		–85	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			52	74	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency			30	45		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$,			17	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	See Note 2			22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock				24	35	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

OCTOBER 1976—REVISED APRIL 1985

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
Buffer/Storage Registers
Shift Registers
Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

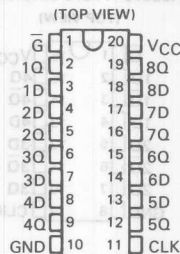
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input \bar{G} is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the \bar{G} input.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

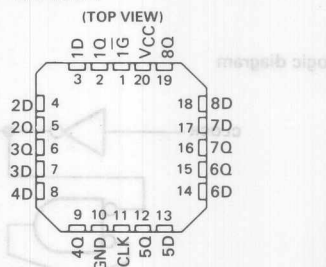
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
\bar{G}	CLOCK	DATA	Q	\bar{Q}
H	X	X	Q_0	\bar{Q}_0
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	\bar{Q}_0

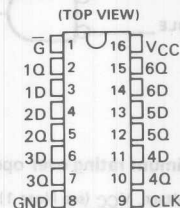
SN54LS377 ... J PACKAGE
SN74LS377 ... DW, J OR N PACKAGE



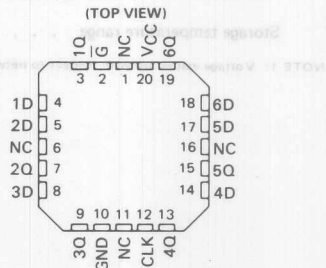
SN54LS377 ... FK PACKAGE
SN74LS377



SN54LS378 ... J OR W PACKAGE
SN74LS378 ... D, J OR N PACKAGE



SN54LS378 ... FK PACKAGE
SN74LS378



NC — No internal connection

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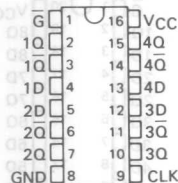
TEXAS
INSTRUMENTS

3

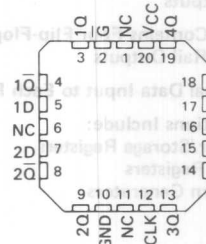
TTL DEVICES

TYPES SN54LS377, SN54LS378, SN54LS379 SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

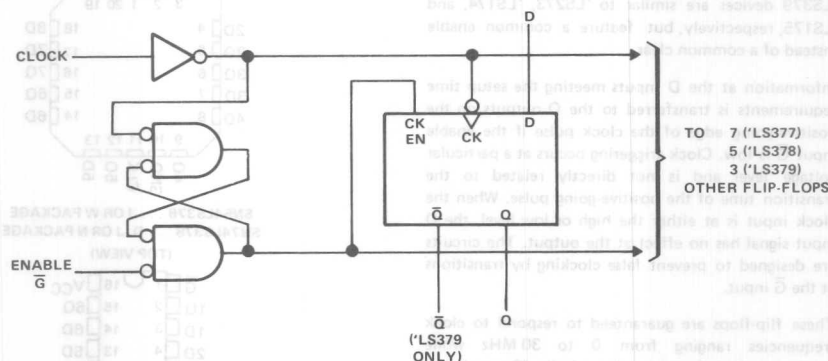
SN54LS379 ... J OR W PACKAGE
SN74LS379 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS379 ... FK PACKAGE
SN74LS379 ... FN PACKAGE
(TOP VIEW)



logic diagram



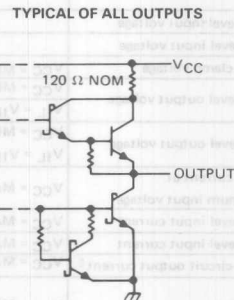
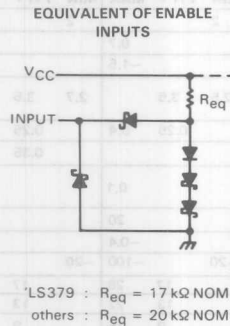
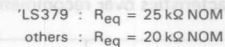
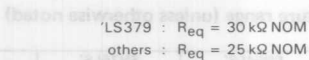
absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS*	-55°C to 125°C
SN74LS*	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

INPUTS	OUTPUTS
1 Q	1 Q
2 Q	2 Q
3 Q	3 Q
4 Q	4 Q
5 Q	5 Q
6 Q	6 Q
7 Q	7 Q
8 Q	8 Q

PHOTOGRAPH BY STEVE BRONSTEIN



LS379 : $R_{eq} = 17 \text{ k}\Omega \text{ NOM}$
others : $R_{eq} = 20 \text{ k}\Omega \text{ NOM}$

1A	39V	<i>m</i>	7580V3
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**TYPES SN54LS377, SN54LS378, SN54LS379,
SN74LS377, SN74LS378, SN74LS379
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE**

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μ A
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, t_W			20			20		ns
Setup time, t_{SU}	Data input		20†			20†		ns
	Enable active-state		25†			25†		
	Enable inactive-state		10†			10†		
Hold time, t_H	Data and enable		5†			5†		ns
Operating free-air temperature, T_A		-55		125	0		70	°C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	SN54LS'			SN74LS'			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS377	17	28	'LS377	17	28	mA
		'LS378	13	22	'LS378	13	22	mA
		'LS379	9	15	'LS379	9	15	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and ground applied to all data and enable inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$	30	40		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clock	$R_L = 2 \text{ k}\Omega$		17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS381A, SN54LS382A, SN54S381, SN74LS381A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D2430, JANUARY 1981—REVISED DECEMBER 1983

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED
		CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
\bar{P} ('LS381A 'S381 ONLY)	14	ACTIVE-LOW CARRY PROPAGATE OUTPUT
\bar{G} ('LS381A 'S381 ONLY)	13	ACTIVE-LOW CARRY GENERATE OUTPUT
$C_n + 4$ ('LS382 ONLY)	14	RIPPLE-CARRY OUTPUT
OVR ('LS382 ONLY)	13	OVERFLOW OUTPUT
VCC	20	SUPPLY VOLTAGE
GND	10	GROUND

- Fully Parallel 4-Bit ALU's in 20-Pin Package for 0.300-Inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- 'LS381A and 'S381 Feature \bar{G} and \bar{P} Outputs for Look-Ahead Carry Cascading
- 'LS382A Features Ripple Carry ($C_n + 4$) and Overflow (OVR) Outputs
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
 - A Minus B
 - B Minus A
 - A Plus B
 - and Five Other Functions

description

The 'LS381A, 'S381 and 'LS382A are low-power Schottky and Schottky TTL arithmetic logic units (ALUs)/function generators that perform eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, or OR function of the two Boolean variables is provided without the use of external circuitry. Also, the outputs can be cleared (low) or preset (high) as desired. The 'LS381A and 'S381 provide two cascade outputs (\bar{P} and \bar{G}) for expansion utilizing SN54S182/SN74S182 look-ahead carry generators. The 'LS382A provides a $C_n + 4$ output to ripple the carry to the C_n input of the next stage. The 'LS382A detects and indicates two's complement overflow condition via the OVR output. The overflow output is logically equivalent to $C_n + 3 \oplus C_n + 4$. When the 'LS382A is cascaded to handle word lengths longer than four bits in length, only the most significant overflow (OVR) output is used.

The SN54' Family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

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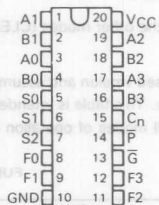
SN54LS381A, SN54S381

... J PACKAGE

SN74LS381A, SN74S381

... DW, J OR N PACKAGE

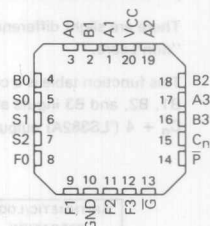
(TOP VIEW)



SN54LS381A, SN54S381

... FK PACKAGE

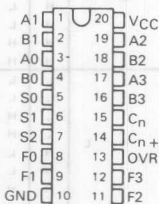
(TOP VIEW)



SN54LS382A ... J PACKAGE SN74LS382A

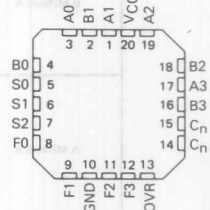
DW, J OR N PACKAGE

(TOP VIEW)



SN54LS382A ... FK PACKAGE SN74LS382A

(TOP VIEW)



FUNCTION TABLE

SELECTION	ARITHMETIC/LOGIC
S2 S1 S0	OPERATION
L L L	CLEAR
L L H	B MINUS A
L H L	A MINUS B
L H H	A PLUS B
H L L	$A \oplus B$
H L H	$A + B$
H H L	AB
H H H	PRESET

H = high level, L = low level

3

TTL DEVICES

TYPES SN54LS381A, SN54LS382A, SN54S381, SN74LS381A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

function table

Certain differences exist in the \bar{G} , \bar{P} ('LS381A, 'S381) and OVR, $C_n + 4$ ('LS382A) function table compared with similar parts from other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B), where these outputs perform valuable cascade functions.

There are slight differences in the other modes (CLEAR, A + B, $A \oplus B$, AB, and PRESET), where these outputs are strictly "don't care."

This function table is a condensed version and assumes for A_n that A0, A1, A2, and A3 inputs all agree and for B_n that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these \bar{G} , \bar{P} ('LS381A, 'S381) and OVR, $C_n + 4$ ('LS382A) outputs in all modes of operation to facilitate incoming inspection.

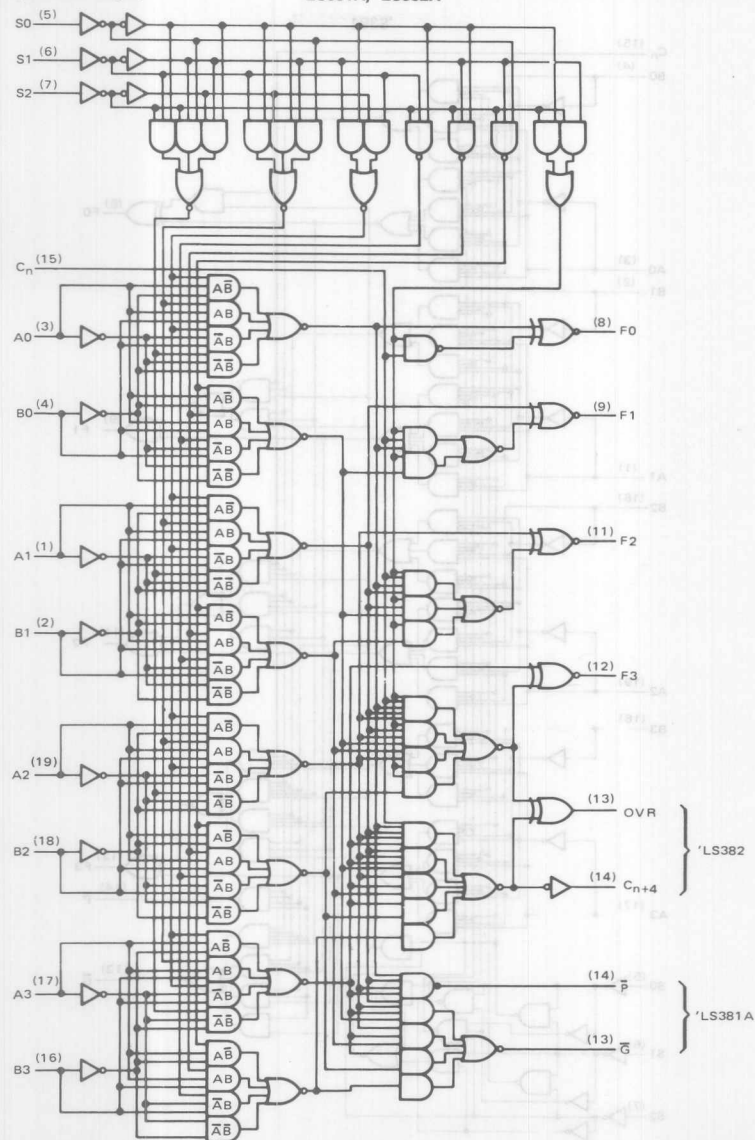
FUNCTION TABLE

ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				('LS381A, 'S381)		('LS382A)	
	S2	S1	S0	C_n	A_n	B_n	F3	F2	F1	F0	\bar{G}	\bar{P}	OVR	$C_n + 4$
CLEAR	L	L	L	X	X	X	L	L	L	L	H	H	L	L
B MINUS A	L	L	H	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	H	H	H	H	H	L	L	H
				L	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	H
				H	L	L	L	L	L	L	H	L	L	H
A MINUS B	L	H	L	L	L	L	L	L	L	L	H	L	L	L
				L	L	H	L	L	L	L	H	L	L	H
				L	H	L	L	L	L	L	H	L	L	L
				L	H	H	H	H	H	H	H	L	L	H
				H	L	L	L	L	L	L	H	L	L	H
A PLUS B	L	L	H	L	L	L	L	L	L	L	H	L	L	L
				L	L	H	H	H	H	H	H	L	L	H
				L	H	L	L	L	L	L	H	L	L	L
				L	H	H	H	H	H	H	H	L	L	H
				H	L	L	L	L	L	L	H	L	L	H
$A \oplus B$	L	H	L	X	L	L	L	L	L	L	H	L	L	L
				L	L	L	H	H	H	H	H	L	L	H
				L	L	H	H	H	H	H	H	L	L	H
				L	H	L	L	L	L	L	H	L	L	L
				L	H	H	H	H	H	H	H	L	L	H
AB	L	H	H	X	L	L	L	L	L	L	H	L	L	L
				L	L	L	H	H	H	H	H	L	L	H
				L	L	H	H	H	H	H	H	L	L	H
				L	H	L	L	L	L	L	H	L	L	L
				L	H	H	H	H	H	H	H	L	L	H
PRESET	H	H	H	L	X	X	H	H	H	H	H	L	L	L
				H	X	X	H	H	H	H	H	L	L	H

TYPES SN54LS381A, SN54LS382A, SN74LS381A, SN74LS382A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)

'LS381A, 'LS382A



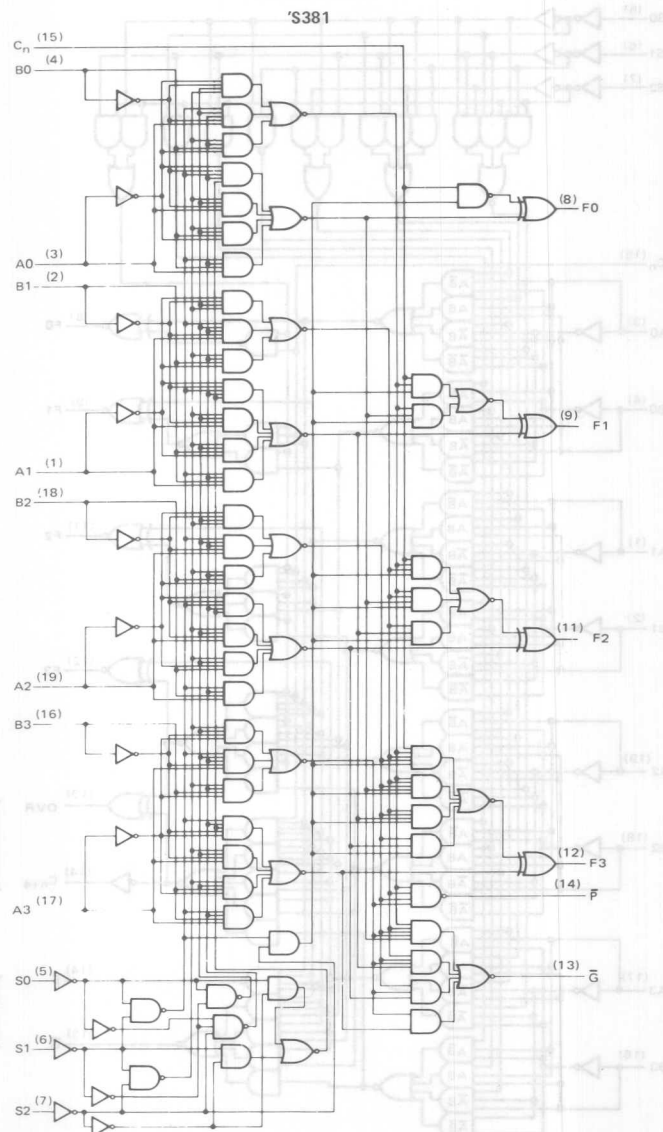
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54S381, SN74S381
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram and schematics of inputs and outputs

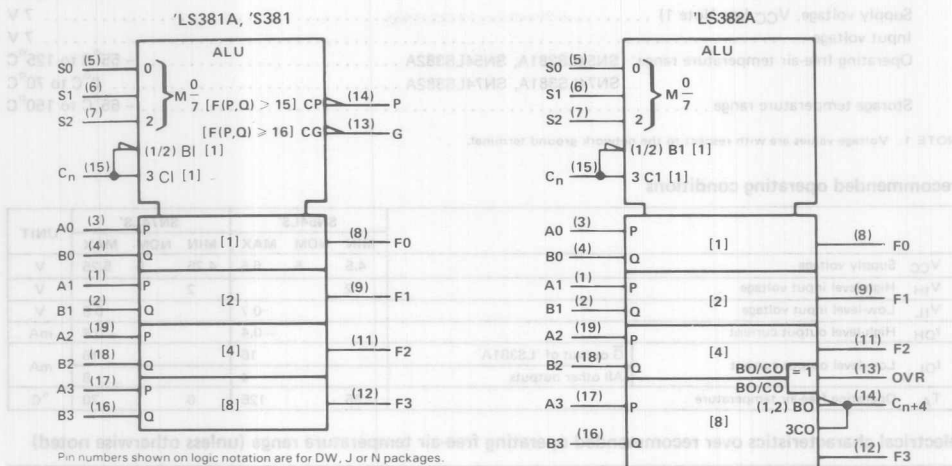


Pin numbers shown on logic notation are for DW, J or N packages.

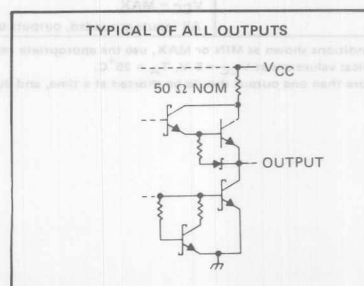
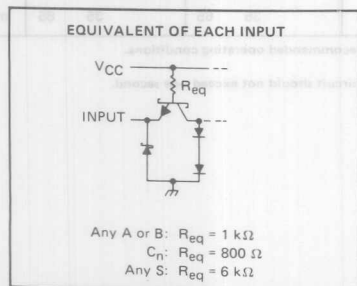
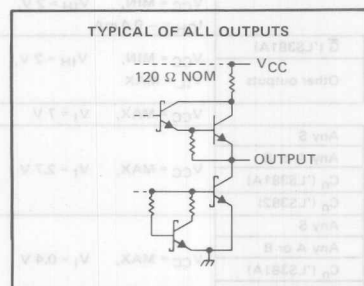
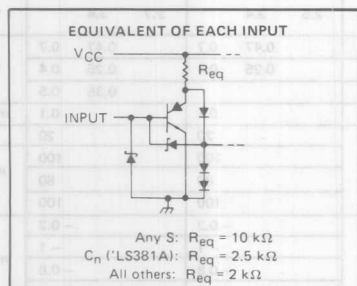
3 TTL DEVICES

TYPES SN54LS381A, SN54LS382A, SN54S381, SN74LS381A, SN74LS382A, SN74S381 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic symbols



schematics of inputs and outputs



3
TTL DEVICES

TYPES SN54LS381A, SN54LS382A, SN74LS381A, SN74LS382A **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS381A, SN54LS382A	–55°C to 125°C
SN74LS381A, SN74LS382A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS*			SN74LS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			− 0.4			− 0.4	mA
I _{OL}	Low-level output current	G output of 'LS381A			16			mA
		All other outputs			4			
T _A	Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	\bar{G} ('LS381A)			0.47			0.47	V
	Other outputs	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 16 \text{ mA}$	0.25			0.25	
			$I_{OL} = 4 \text{ mA}$	0.4			0.4	
I_I	Any S Any A or B C_n ('LS381A) C_n ('LS382)	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1	mA
				20			20	
		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		100			100	
				80			80	
I_{IH}	Any S Any A or B C_n ('LS381A) C_n ('LS382)			100			100	μA
				–0.2			–0.2	
				–1			–1	
				–0.8			–0.8	
I_{IL}	Any S Any A or B C_n ('LS381A) C_n ('LS382)	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		–0.8			–0.8	mA
				–0.8			–0.8	
				–20			–20	
				–100			–100	
$I_{OS}§$	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC}	$V_{CC} = \text{MAX},$ All inputs grounded, outputs open	35	65		35	65		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

TYPES SN54LS381A, SN54LS382A, SN74LS381A, SN74LS382A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS381A			'LS382A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	C_n	Any F			18	27		18	27	ns
t_{PHL}					14	21		14	21	
t_{PLH}	Any A or B	\bar{G}			20	30				ns
t_{PHL}					21	33				
t_{PLH}	Any A or B	P			21	33				ns
t_{PHL}					23	33				
t_{PLH}	A_i or B_i	F_i			20	30		20	30	ns
t_{PHL}					15	23		15	23	
t_{PLH}	S0, S1, S2	F_i			35	53		35	53	ns
t_{PHL}					34	51		34	51	
t_{PLH}	S0, S1, S2	\bar{G} or \bar{P}	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$		31	47				ns
t_{PHL}					32	48				
t_{PLH}	Any A or B	C_{n+4}						28	42	ns
t_{PHL}								26	39	
t_{PLH}	Any A or B	OVR						23	35	ns
t_{PHL}								27	41	
t_{PLH}	S0, S1, S2	C_{n+4} or OVR						38	57	ns
t_{PHL}								36	54	
t_{PLH}	C_n	OVR						10	15	ns
t_{PHL}								13	23	
t_{PLH}	C_n	C_{n+4}						13	21	ns
t_{PHL}								11	20	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

I_{CC}	Supply current	$V_{CC} = 5\text{ V}$	100	20	100	20
I_{OC}	Short-circuit output current	$V_{CC} = 5\text{ V}$	-40	-100	-40	-100
I_{OL}	Low-level input current	$V_{CC} = 5\text{ V}$	-1	-1	-1	-1
I_{OH}	High-level input current	$V_{CC} = 5\text{ V}$	1	1	1	1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	Any F			18	27	ns
t_{PHL}					14	21	
t_{PLH}	Any A or B	\bar{G}			20	30	ns
t_{PHL}					21	33	
t_{PLH}	Any A or B	P			21	33	ns
t_{PHL}					23	33	
t_{PLH}	A_i or B_i	F_i			20	30	ns
t_{PHL}					15	23	
t_{PLH}	S0, S1, S2	F_i			35	53	ns
t_{PHL}					34	51	
t_{PLH}	S0, S1, S2	\bar{G} or \bar{P}	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$		31	47	ns
t_{PHL}					32	48	
t_{PLH}	Any A or B	C_{n+4}					ns
t_{PHL}							
t_{PLH}	Any A or B	OVR					ns
t_{PHL}							
t_{PLH}	S0, S1, S2	C_{n+4} or OVR					ns
t_{PHL}							
t_{PLH}	C_n	OVR					ns
t_{PHL}							
t_{PLH}	C_n	C_{n+4}					ns
t_{PHL}							

TYPES SN54S381, SN74S381

ARITHMETIC LOGIC UNIT/FUNCTION GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S381	-55°C to 125°C
SN74S381	0°C to 70°C
Storage free-air temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with its respective B input; for example A0 with B0, etc.

recommended operating conditions

	SN54S381			SN74S381			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55	125	0	70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	High-level output voltage	SN54S381 $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$		2.4	3.4		V
		SN74S381 $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		mA
I_{IH}	High-level input current	Any S input			50		
		C_n	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		250		μA
		All others			200		
I_{IL}	Low-level input current	Any S input	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2		
		C_n			-8		mA
		All others			-6		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			105	160	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	Cn	Any F	CL = 15 pF, See Note 3	RL = 280 Ω,	10	17		ns
tPHL					10	17		
tPLH	Any A or B	G			12	20		ns
tPHL					12	20		
tPLH	Any A or B	P			11	18		ns
tPHL					11	18		
tPLH	Ai or Bi	Fi			18	27		ns
tPHL					16	25		
tPLH	Any S	Any			18	30		ns
tPHL					18	30		

¶ t_{PLH} propagation delay time, low to high-level output

t_{PHL} propagation delay time, high to low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS384, SN74LS384

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

D2419, JANUARY 1981 — REVISED DECEMBER 1983

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency

description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the PROD output, least significant bit first.

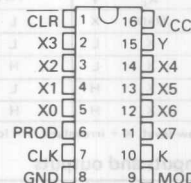
The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The PROD output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

The SN54LS384 will be characterized for operation over the full military temperature range from -55°C to 125°C. The SN74LS384 will be characterized for operation from 0°C to 70°C.

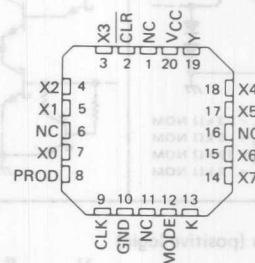
SN54LS384 ... J PACKAGE
SN74LS384 ... J OR N PACKAGE

(TOP VIEW)



SN54LS384 ... FK PACKAGE
SN74LS384

(TOP VIEW)



NC — No internal connection

3

TTL DEVICES

PRODUCTION DATA

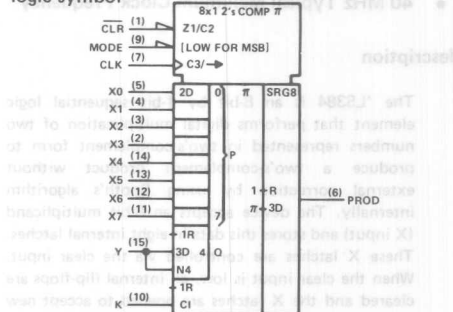
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3-897

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logic symbol



ages.

logic diagram (positive logic)

7 V

5.5 V

5.5 V

25°C

70°C

50°C

50°C

50°C

TYPES SN54LS384, SN74LS384 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

recommended operating conditions

		SN54LS384			SN74LS384			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μ A
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Setup time, t_{SU}	Y before Clock \uparrow	45			38			ns
	K before Clock \uparrow	30			24			
	X before Clear \uparrow	23			19			
Clear inactive-state set up time before Clock \uparrow		30			20			
Hold time, t_H	Y after Clock \uparrow	0			0			ns
	K after Clock \uparrow	0			0			
	X after Clear \uparrow	2			2			
Pulse width, t_W	Clock high	20			20			ns
	Clock low	20			20			
	Clear low	38			33			
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS384			SN74LS384			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = -400 \mu\text{A}$		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$			0.25	0.4		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$						0.35	0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
I_{IH}	High-level input current	X, Mode				20			20	μ A
		K, Clear	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			30			30	
		Clock				40			40	
		Y				80			80	
I_{IL}	Low-level input current	X, Mode	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.48			-0.48	mA
		K, Clear				-1.2			-1.2	
		Clock				-1.6			-1.6	
		Y				-3.2			-3.2	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3			91	132		91	132	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		25	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF},$		15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	$R_L = 2 \text{ k}\Omega,$		15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear	See Note 4		17	25	ns

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS384, SN74LS384 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

TYPICAL APPLICATION DATA

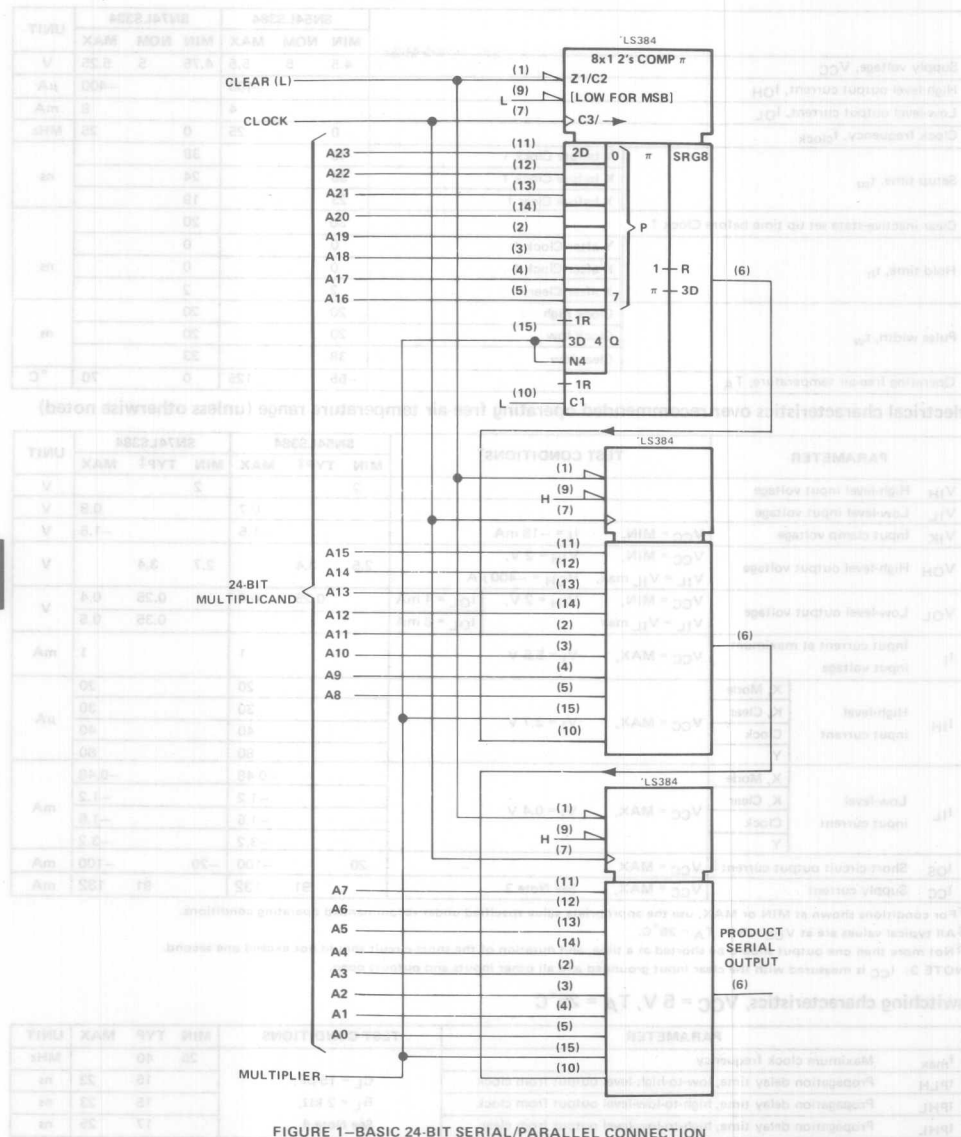


FIGURE 1—BASIC 24-BIT SERIAL/PARALLEL CONNECTION

3 TTL DEVICES

TYPES SN54LS384, SN74LS384 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

TYPICAL APPLICATION DATA

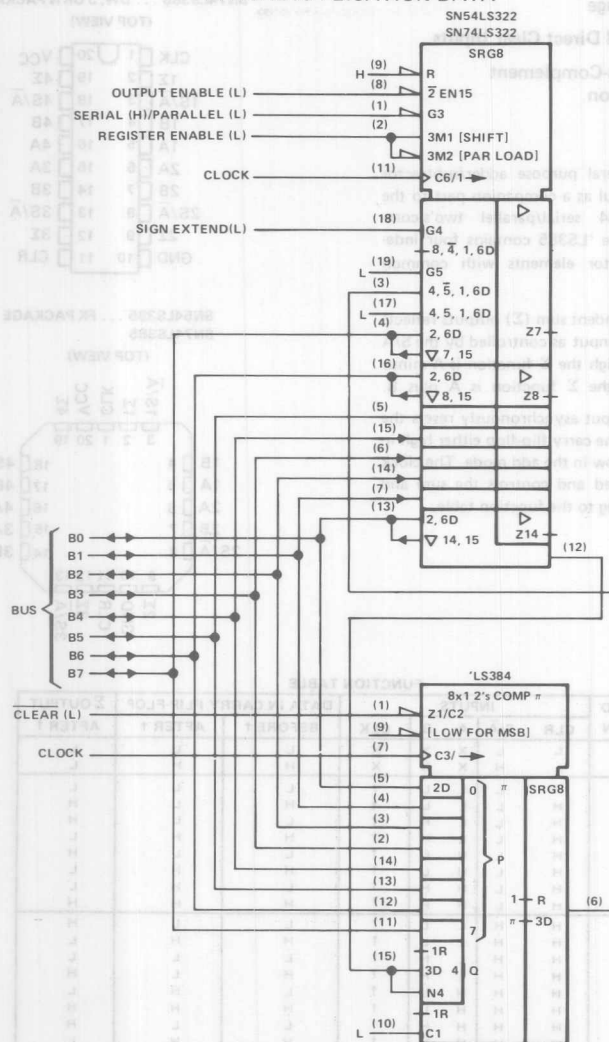


FIGURE 2—8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED,
WITH 8-BIT TRUNCATED PRODUCT

3

TTL DEVICES

TYPES SN54LS385, SN74LS385 QUADRUPLE SERIAL ADDERS/SUBTRACTORS

D2412, NOVEMBER 1977—REVISED APRIL 1985

- Four Synchronous Elements in a Single 20-Pin Package
- Buffered Clock and Direct Clear Inputs
- Independent Two's-Complement Addition/Subtraction

description

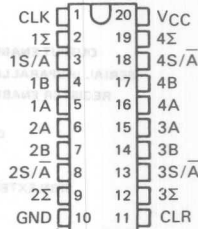
The 'LS385 is a general purpose adder/subtractor and is particularly useful as a companion part to the SN54LS384/SN74LS384 serial/parallel two's-complement multiplier. The 'LS385 contains four independent adder/subtractor elements with common clock and clear.

Each of the four independent sum (Σ) outputs reflects its respective A and B input as controlled by the S/ \bar{A} control. When S/ \bar{A} is high the Σ function is A minus B. When S/ \bar{A} is low the Σ function is A plus B.

When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops according to the function table.

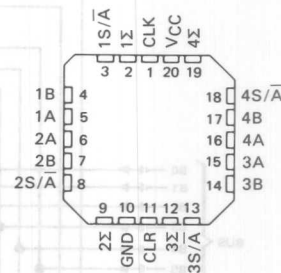
SN54LS385 ... J PACKAGE
SN74LS385 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS385 ... FK PACKAGE
SN74LS385

(TOP VIEW)



FUNCTION TABLE

SELECTED FUNCTION	INPUTS					DATA IN CARRY FLIP-FLOP		Σ OUTPUT AFTER ↑
	CLR	S/ \bar{A}	A	B	CLK	BEFORE ↑	AFTER ↑	
Clear	L	L	X	X	X	L	L	L
	L	H	X	X	X	H	H	L
Add	H	L	L	L	↑	L	L	L
	H	L	L	L	↑	H	L	H
	H	L	L	H	↑	L	L	H
	H	L	L	H	↑	H	L	L
	H	L	H	L	↑	L	H	L
	H	L	H	L	↑	H	H	L
	H	L	H	H	↑	L	H	H
Subtract	H	H	L	L	↑	L	L	H
	H	H	L	L	↑	H	H	L
	H	H	L	H	↑	L	L	L
	H	H	L	H	↑	H	L	L
	H	H	H	L	↑	L	H	L
	H	H	H	L	↑	H	H	L
	H	H	H	H	↑	L	L	H

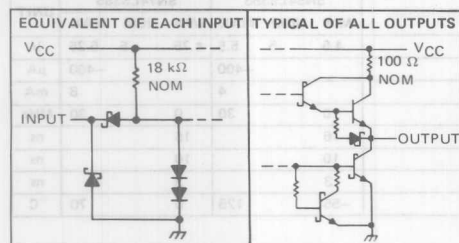
H = high level, L = low level, X = irrelevant,
↑ = transition from low to high level at the clock input

PRODUCTION DATA

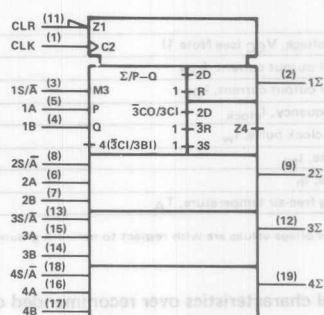
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TYPES SN54LS385, SN74LS385 QUADRUPLE SERIAL ADDERS/SUBTRACTORS

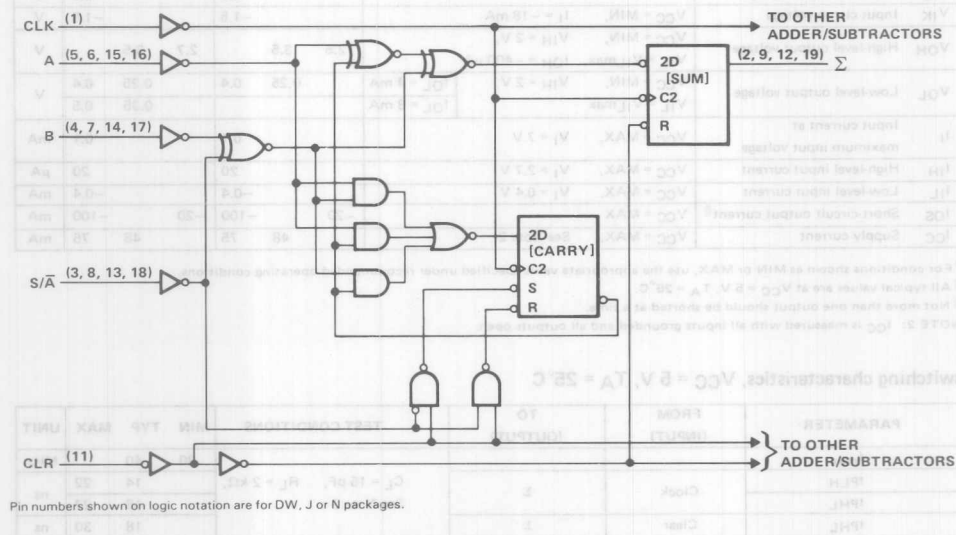
schematics of inputs and outputs



logic symbol



logic diagram (each adder/subtractor, positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS385, SN74LS385

QUADRUPLE SERIAL ADDERS/SUBTRACTORS

recommended operating conditions

	SN54LS385			SN74LS385			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	16		16				ns
Setup time, t_{SU}	10		10				ns
Hold time, t_H	3		3				ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS385			SN74LS385			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	48		75	48		75	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				30	40		MHz
t_{PLH}	Clock	Σ	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 3		14	22	ns
t_{PHL}		Σ			18	27	ns
t_{PHL}	Clear	Σ			18	30	ns

† f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

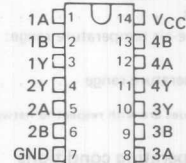
TYPES SN54LS386A, SN74LS386A QUADRUPE 2-INPUT EXCLUSIVE-OR GATES

MARCH 1974 - REVISED DECEMBER 1983

- Electrically Identical to SN54LS86A/SN74LS86A
- Mechanically Identical to SN54LS86/SN74LS86
- Total Average Propagation Delay Times . . . 10 ns
- Typical Total Power Dissipation . . . 30.5 mW

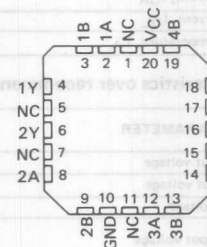
SN54LS386A . . . J OR W PACKAGE
SN74LS386A . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS386A . . . FK PACKAGE
SN74LS386A

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE
(EACH GATE)

INPUTS	OUTPUT
A B	
L L	L
L H	H
H L	H
H H	L

H = high level
L = low level

logic diagram (each gate)

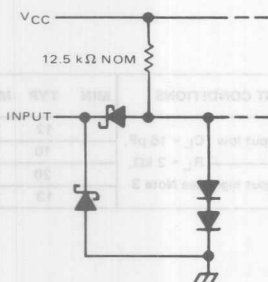


positive logic

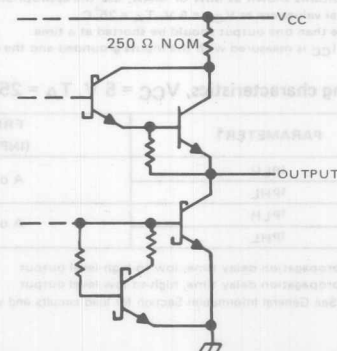
$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-905

3

TTL DEVICES

TYPES SN54LS386A, SN74LS386A QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS386A	-55°C to 125°C
SN74LS386A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS386A			SN74LS386A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS386A			SN74LS386A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}, I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.2			0.2	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			40			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8			-0.8	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	6.1		10	6.1		10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low $C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 3	12	23		ns
t_{PHL}			10	17		
t_{PLH}	A or B	Other input high	20	30		ns
t_{PHL}			13	22		

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54390, SN54LS390, SN54393, SN54LS393, SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

OCTOBER 1976—REVISED DECEMBER 1983

- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual $\div 2$ and $\div 5$ Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

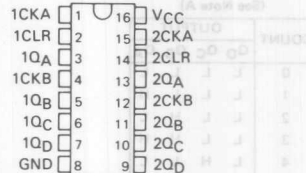
description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C .

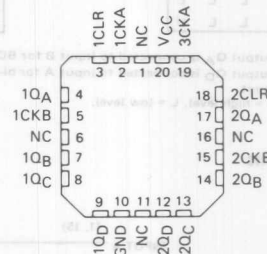
SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390 . . . J OR N PACKAGE
SN74LS390 . . . D, J OR N PACKAGE

(TOP VIEW)



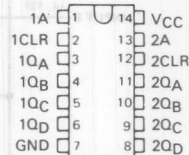
SN54LS390 . . . FK PACKAGE
SN74LS390

(TOP VIEW)



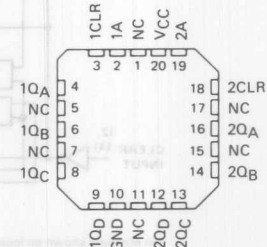
SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393 . . . J OR N PACKAGE
SN74LS393 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS393 . . . FK PACKAGE
SN74LS393

(TOP VIEW)



NC - No internal connection

PRODUCTION DATA
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TEXAS
INSTRUMENTS

3-907

3

TTL DEVICES

TYPES SN54390, SN54LS390, SN54393, SN54LS393, SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

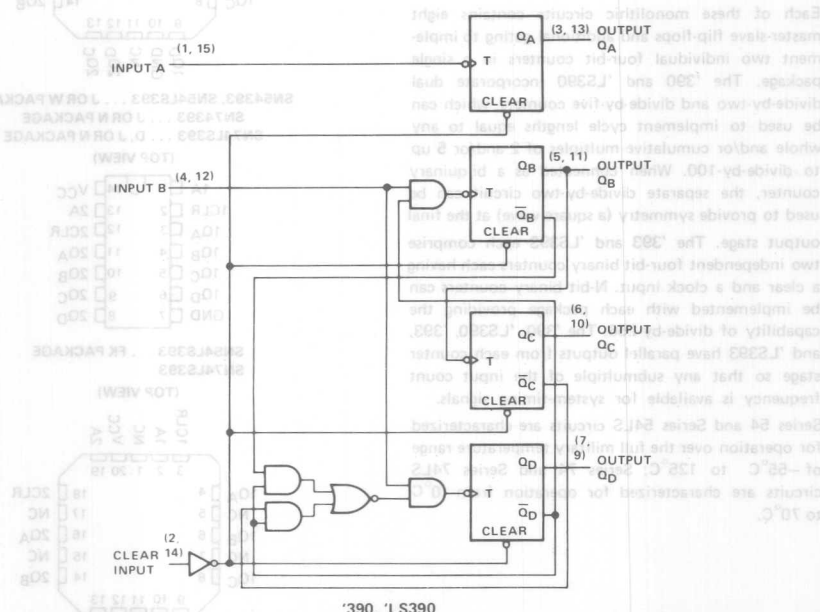
FUNCTION TABLES				
'390, 'LS390				
BCD COUNT SEQUENCE (EACH COUNTER)				
(See Note A)				
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'390, 'LS390				
BI-QUINARY (5-2) (EACH COUNTER)				
(See Note B)				
COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'393, 'LS393				
COUNT SEQUENCE (EACH COUNTER)				
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

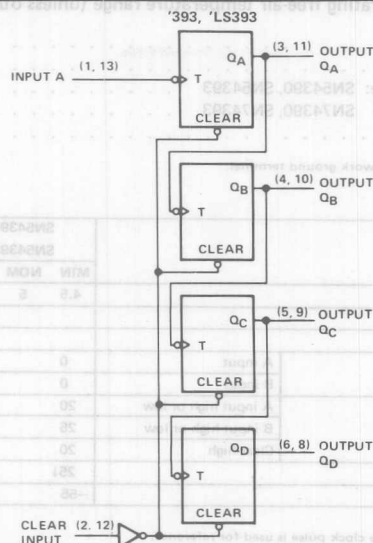
logic diagrams



Pin numbers shown on logic notation are for D, J or N packages.

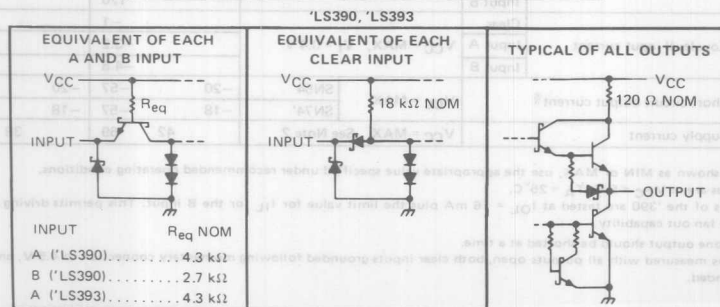
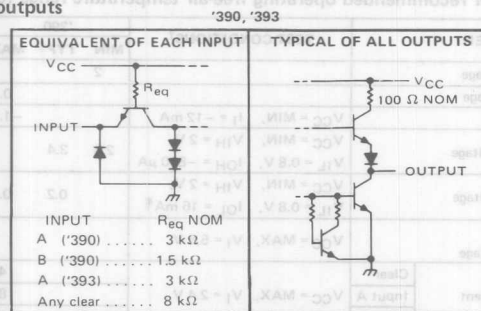
3 TTL DEVICES

logic diagrams (continued)



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



TYPES SN54390, SN54393, SN74390, SN74393 DUAL 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	-55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54390 SN54393			SN74390 SN74393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		20	0		20	
Pulse width, t_W	A input high or low	20			20			ns
	B input high or low	25			25			
	Clear high	20			20			
Clear inactive-state setup time, t_{SU}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

† The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'390			'393			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$ ¶		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	Clear			40			40	μ A
	Input A	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		80			80	
	Input B			120				
I_{IL} Low-level input current	Clear			-1			-1	mA
	Input A	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-3.2			-3.2	
	Input B			-4.8				
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54*	-20	-57	-20	-57		mA
		SN74*	-18	-57	-18	-57		
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		42	69		38	64	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

¶ The O_A outputs of the '390 are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

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TTL DEVICES

TYPES SN54390, SN54393, SN74390, SN74393 DUAL 4-BIT DECADE AND BINARY COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Note 3 and Figure 1	25	35		25	35		MHz
	B	Q_B		20	30					
t_{PLH}	A	Q_A			12	20		12	20	ns
t_{PHL}	A	Q_C of '390 Q_D of '393			13	20		13	20	
t_{PLH}	A	Q_C of '390 Q_D of '393			37	60		40	60	ns
t_{PHL}	A	Q_C of '390 Q_D of '393			39	60		40	60	
t_{PLH}	B	Q_B			13	21				ns
t_{PHL}	B	Q_B			14	21				
t_{PLH}	B	Q_C			24	39				ns
t_{PHL}	B	Q_C			26	39				
t_{PLH}	B	Q_D			13	21				ns
t_{PHL}	B	Q_D			14	21				
t_{PHL}	Clear	Any			24	39		24	39	ns

[†] f_{max} = maximum count frequency

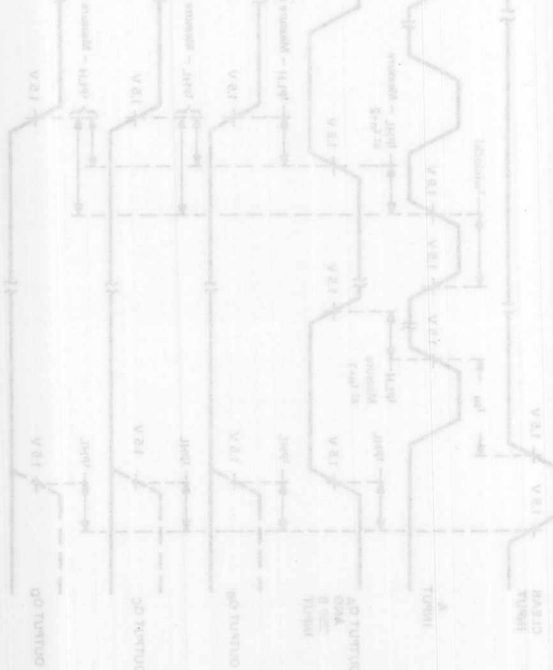
t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

FIGURE 1

AC TYPICAL WAVEFORMS



3

TTL DEVICES

TYPES SN54390, SN54393, SN74390, SN74393 DUAL 4-BIT DECADE AND BINARY COUNTERS

PARAMETER MEASUREMENT INFORMATION

TIME	STATE	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23	Q24	Q25	Q26	Q27	Q28	Q29	Q30	Q31	Q32	Q33	Q34	Q35	Q36	Q37	Q38	Q39	Q40	Q41	Q42	Q43	Q44	Q45	Q46	Q47	Q48	Q49	Q50	Q51	Q52	Q53	Q54	Q55	Q56	Q57	Q58	Q59	Q60	Q61	Q62	Q63	Q64	Q65	Q66	Q67	Q68	Q69	Q70	Q71	Q72	Q73	Q74	Q75	Q76	Q77	Q78	Q79	Q80	Q81	Q82	Q83	Q84	Q85	Q86	Q87	Q88	Q89	Q90	Q91	Q92	Q93	Q94	Q95	Q96	Q97	Q98	Q99	Q100	Q101	Q102	Q103	Q104	Q105	Q106	Q107	Q108	Q109	Q110	Q111	Q112	Q113	Q114	Q115	Q116	Q117	Q118	Q119	Q120	Q121	Q122	Q123	Q124	Q125	Q126	Q127	Q128	Q129	Q130	Q131	Q132	Q133	Q134	Q135	Q136	Q137	Q138	Q139	Q140	Q141	Q142	Q143	Q144	Q145	Q146	Q147	Q148	Q149	Q150	Q151	Q152	Q153	Q154	Q155	Q156	Q157	Q158	Q159	Q160	Q161	Q162	Q163	Q164	Q165	Q166	Q167	Q168	Q169	Q170	Q171	Q172	Q173	Q174	Q175	Q176	Q177	Q178	Q179	Q180	Q181	Q182	Q183	Q184	Q185	Q186	Q187	Q188	Q189	Q190	Q191	Q192	Q193	Q194	Q195	Q196	Q197	Q198	Q199	Q200	Q201	Q202	Q203	Q204	Q205	Q206	Q207	Q208	Q209	Q210	Q211	Q212	Q213	Q214	Q215	Q216	Q217	Q218	Q219	Q220	Q221	Q222	Q223	Q224	Q225	Q226	Q227	Q228	Q229	Q230	Q231	Q232	Q233	Q234	Q235	Q236	Q237	Q238	Q239	Q240	Q241	Q242	Q243	Q244	Q245	Q246	Q247	Q248	Q249	Q250	Q251	Q252	Q253	Q254	Q255	Q256	Q257	Q258	Q259	Q260	Q261	Q262	Q263	Q264	Q265	Q266	Q267	Q268	Q269	Q270	Q271	Q272	Q273	Q274	Q275	Q276	Q277	Q278	Q279	Q280	Q281	Q282	Q283	Q284	Q285	Q286	Q287	Q288	Q289	Q290	Q291	Q292	Q293	Q294	Q295	Q296	Q297	Q298	Q299	Q300	Q301	Q302	Q303	Q304	Q305	Q306	Q307	Q308	Q309	Q310	Q311	Q312	Q313	Q314	Q315	Q316	Q317	Q318	Q319	Q320	Q321	Q322	Q323	Q324	Q325	Q326	Q327	Q328	Q329	Q330	Q331	Q332	Q333	Q334	Q335	Q336	Q337	Q338	Q339	Q340	Q341	Q342	Q343	Q344	Q345	Q346	Q347	Q348	Q349	Q350	Q351	Q352	Q353	Q354	Q355	Q356	Q357	Q358	Q359	Q360	Q361	Q362	Q363	Q364	Q365	Q366	Q367	Q368	Q369	Q370	Q371	Q372	Q373	Q374	Q375	Q376	Q377	Q378	Q379	Q380	Q381	Q382	Q383	Q384	Q385	Q386	Q387	Q388	Q389	Q390	Q391	Q392	Q393	Q394	Q395	Q396	Q397	Q398	Q399	Q400	Q401	Q402	Q403	Q404	Q405	Q406	Q407	Q408	Q409	Q410	Q411	Q412	Q413	Q414	Q415	Q416	Q417	Q418	Q419	Q420	Q421	Q422	Q423	Q424	Q425	Q426	Q427	Q428	Q429	Q430	Q431	Q432	Q433	Q434	Q435	Q436	Q437	Q438	Q439	Q440	Q441	Q442	Q443	Q444	Q445	Q446	Q447	Q448	Q449	Q450	Q451	Q452	Q453	Q454	Q455	Q456	Q457	Q458	Q459	Q460	Q461	Q462	Q463	Q464	Q465	Q466	Q467	Q468	Q469	Q470	Q471	Q472	Q473	Q474	Q475	Q476	Q477	Q478	Q479	Q480	Q481	Q482	Q483	Q484	Q485	Q486	Q487	Q488	Q489	Q490	Q491	Q492	Q493	Q494	Q495	Q496	Q497	Q498	Q499	Q500	Q501	Q502	Q503	Q504	Q505	Q506	Q507	Q508	Q509	Q510	Q511	Q512	Q513	Q514	Q515	Q516	Q517	Q518	Q519	Q520	Q521	Q522	Q523	Q524	Q525	Q526	Q527	Q528	Q529	Q530	Q531	Q532	Q533	Q534	Q535	Q536	Q537	Q538	Q539	Q540	Q541	Q542	Q543	Q544	Q545	Q546	Q547	Q548	Q549	Q550	Q551	Q552	Q553	Q554	Q555	Q556	Q557	Q558	Q559	Q560	Q561	Q562	Q563	Q564	Q565	Q566	Q567	Q568	Q569	Q570	Q571	Q572	Q573	Q574	Q575	Q576	Q577	Q578	Q579	Q580	Q581	Q582	Q583	Q584	Q585	Q586	Q587	Q588	Q589	Q590	Q591	Q592	Q593	Q594	Q595	Q596	Q597	Q598	Q599	Q600	Q601	Q602	Q603	Q604	Q605	Q606	Q607	Q608	Q609	Q610	Q611	Q612	Q613	Q614	Q615	Q616	Q617	Q618	Q619	Q620	Q621	Q622	Q623	Q624	Q625	Q626	Q627	Q628	Q629	Q630	Q631	Q632	Q633	Q634	Q635	Q636	Q637	Q638	Q639	Q640	Q641	Q642	Q643	Q644	Q645	Q646	Q647	Q648	Q649	Q650	Q651	Q652	Q653	Q654	Q655	Q656	Q657	Q658	Q659	Q660	Q661	Q662	Q663	Q664	Q665	Q666	Q667	Q668	Q669	Q670	Q671	Q672	Q673	Q674	Q675	Q676	Q677	Q678	Q679	Q680	Q681	Q682	Q683	Q684	Q685	Q686	Q687	Q688	Q689	Q690	Q691	Q692	Q693	Q694	Q695	Q696	Q697	Q698	Q699	Q700	Q701	Q702	Q703	Q704	Q705	Q706	Q707	Q708	Q709	Q710	Q711	Q712	Q713	Q714	Q715	Q716	Q717	Q718	Q719	Q720	Q721	Q722	Q723	Q724	Q725	Q726	Q727	Q728	Q729	Q730	Q731	Q732	Q733	Q734	Q735	Q736	Q737	Q738	Q739	Q740	Q741	Q742	Q743	Q744	Q745	Q746	Q747	Q748	Q749	Q750	Q751	Q752	Q753	Q754	Q755	Q756	Q757	Q758	Q759	Q760	Q761	Q762	Q763	Q764	Q765	Q766	Q767	Q768	Q769	Q770	Q771	Q772	Q773	Q774	Q775	Q776	Q777	Q778	Q779	Q780	Q781	Q782	Q783	Q784	Q785	Q786	Q787	Q788	Q789	Q790	Q791	Q792	Q793	Q794	Q795	Q796	Q797	Q798	Q799	Q800	Q801	Q802	Q803	Q804	Q805	Q806	Q807	Q808	Q809	Q810	Q811	Q812	Q813	Q814	Q815	Q816	Q817	Q818	Q819	Q820	Q821	Q822	Q823	Q824	Q825	Q826	Q827	Q828	Q829	Q830	Q831	Q832	Q833	Q834	Q835	Q836	Q837	Q838	Q839	Q840	Q841	Q842	Q843	Q844	Q845	Q846	Q847	Q848	Q849	Q850	Q851	Q852	Q853	Q854	Q855	Q856	Q857	Q858	Q859	Q860	Q861	Q862	Q863	Q864	Q865	Q866	Q867	Q868	Q869	Q870	Q871	Q872	Q873	Q874	Q875	Q876	Q877	Q878	Q879	Q880	Q881	Q882	Q883	Q884	Q885	Q886	Q887	Q888	Q889	Q890	Q891	Q892	Q893	Q894	Q895	Q896	Q897	Q898	Q899	Q900	Q901	Q902	Q903	Q904	Q905	Q906	Q907	Q908	Q909	Q910	Q911	Q912	Q913	Q914	Q915	Q916	Q917	Q918	Q919	Q920	Q921	Q922	Q923	Q924	Q925	Q926	Q927	Q928	Q929	Q930	Q931	Q932	Q933	Q934	Q935	Q936	Q937	Q938	Q939	Q940	Q941	Q942	Q943	Q944	Q945	Q946	Q947	Q948	Q949	Q950	Q951	Q952	Q953	Q954	Q955	Q956	Q957	Q958	Q959	Q960	Q961	Q962	Q963	Q964	Q965	Q966	Q967	Q968	Q969	Q970	Q971	Q972	Q973	Q974	Q975	Q976	Q977	Q978	Q979	Q980	Q981	Q982	Q983	Q984	Q985	Q986	Q987	Q988	Q989	Q990	Q991	Q992	Q993	Q994	Q995	Q996	Q997	Q998	Q999	Q1000	Q1001	Q1002	Q1003	Q1004	Q1005	Q1006	Q1007	Q1008	Q1009	Q1010	Q1011	Q1012	Q1013	Q1014	Q1015	Q1016	Q1017	Q1018	Q1019	Q1020	Q1021	Q1022	Q1023	Q1024	Q1025	Q1026	Q1027	Q1028	Q1029	Q1030	Q1031	Q1032	Q1033	Q1034	Q1035	Q1036	Q1037	Q1038	Q1039	Q1040	Q1041	Q1042	Q1043	Q1044	Q1045	Q1046	Q1047	Q1048	Q1049	Q1050	Q1051	Q1052	Q1053	Q1054	Q1055	Q1056	Q1057	Q1058	Q1059	Q1060	Q1061	Q1062	Q1063	Q1064	Q1065	Q1066	Q1067	Q1068	Q1069	Q1070	Q1071	Q1072	Q1073	Q1074	Q1075	Q1076	Q1077	Q1078	Q1079	Q1080	Q1081	Q1082	Q1083	Q1084	Q1085	Q1086	Q1087	Q1088	Q1089	Q1090	Q1091	Q1092	Q1093	Q1094	Q1095	Q1096	Q1097	Q1098	Q1099	Q1100	Q1101	Q1102	Q1103	Q1104	Q1105	Q1106	Q1107	Q1108	Q1109	Q1110	Q1111	Q1112	Q1113	Q1114	Q1115	Q1116	Q1117	Q1118	Q1119	Q1120	Q1121	Q1122	Q1123	Q1124	Q1125	Q1126	Q1127	Q1128	Q1129	Q1130	Q1131	Q1132	Q1133	Q1134	Q1135	Q1136	Q1137	Q1138	Q1139	Q1140	Q1141	Q1142	Q1143	Q1144	Q1145	Q1146	Q1147	Q1148	Q1149	Q1150	Q1151	Q1152	Q1153	Q1154	Q1155	Q1156	Q1157	Q1158	Q1159	Q1160	Q1161	Q1162	Q1163	Q1164	Q1165	Q1166	Q1167	Q1168	Q1169	Q1170	Q1171	Q1172	Q1173	Q1174	Q1175	Q1176	Q1177	Q1178	Q1179	Q1180	Q1181	Q1182	Q1183	Q1184	Q1185	Q1186	Q1187	Q1188	Q1189	Q1190	Q1191	Q1192	Q1193	Q1194	Q1195	Q1196	Q1197	Q1198	Q1199	Q1200	Q1201	Q1202	Q1203	Q1204	Q1205	Q1206	Q1207	Q1208	Q1209	Q1210	Q1211	Q1212	Q1213	Q1214	Q1215	Q1216	Q1217	Q1218	Q1219	Q1220	Q1221	Q1222	Q1223	Q1224	Q1225	Q1226	Q1227	Q1228	Q1229	Q1230	Q1231	Q1232	Q1233	Q1234	Q1235	Q1236	Q1237	Q1238	Q1239	Q1240	Q1241	Q1242	Q1243	Q1244	Q1245	Q1246	Q1247	Q1248	Q1249	Q1250	Q1251	Q1252	Q1253	Q1254	Q1255	Q1256	Q1257	Q1258	Q1259	Q1260	Q1261	Q1262	Q1263	Q1264	Q1265	Q1266	Q1267	Q1268	Q1269	Q1270	Q1271	Q1272	Q1273	Q1274	Q1275	Q1276	Q1277	Q1278	Q1279	Q1280	Q1281	Q1282	Q1283	Q1284	Q1285	Q1286	Q1287	Q1288	Q1289	Q1290	Q1291	Q1292	Q1293	Q1294	Q1295	Q1296	Q1297	Q1298	Q1299	Q1300	Q1301	Q1302	Q1303	Q1304	Q1305	Q1306	Q1307	Q1308	Q1309	Q1310	Q1311	Q1312	Q1313	Q1314	Q1315	Q1316	Q1317	Q1318	Q1319	Q1320	Q1321	Q1322	Q1323	Q1324	Q1325	Q1326	Q1327	Q1328	Q1329	Q
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TYPES SN54LS390, SN54LS393, SN74LS390, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Clear input voltage	7 V
Any A or B clock input voltage	5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393	-55°C to 125°C
SN74LS390, SN74LS393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μ A
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		12.5	0		12.5	
Pulse width, t_W	A input high or low	20			20			ns
	B input high or low	40			40			
	Clear high	20			20			
Clear inactive-state setup time, t_{SU}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

† The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$	$I_{OL} = 4 \text{ mA}^\S$		0.25	0.4	0.25		0.4
			$I_{OL} = 8 \text{ mA}^\S$				0.35		0.5
I_I	Input current at maximum input voltage	Clear			0.1			0.1	mA
		Input A	$V_{CC} = \text{MAX}$		0.2			0.2	
		Input B	$V_I = 5.5 \text{ V}$		0.4			0.4	
		Clear			0.02			0.02	
I_{IH}	High-level input current	Input A	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		0.1			0.1	mA
		Input B			0.2			0.2	
		Clear			-0.4			-0.4	
I_{IL}	Low-level input current	Input A	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-1.6			-1.6	mA
		Input B			-2.4			-2.4	
		Clear							
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$,		15	26		15	26	mA
		See Note 2		15	26		15	26	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ The Q_A outputs of the 'LS390 are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

TYPES SN54LS390, SN54LS393, SN74LS390, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Note 4 and Figure 2	25	35		25	35		MHz
	B	Q_B		12.5	20					
t_{PLH}	A	Q_A			12	20		12	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	A	Q_C of 'LS390			37	60		40	60	ns
t_{PHL}		Q_D of 'LS393			39	60		40	60	
t_{PLH}	B	Q_B			13	21				ns
t_{PHL}					14	21				
t_{PLH}	B	Q_C			24	39				ns
t_{PHL}					26	39				
t_{PLH}	B	Q_D			13	21				ns
t_{PHL}					14	21				
t_{PHL}	Clear	Any			24	39		24	39	ns

f_{\max} maximum count frequency

t_{PLH} propagation delay time, low-to-high-level output

t_{PHL} propagation delay time, high-to-low-level output

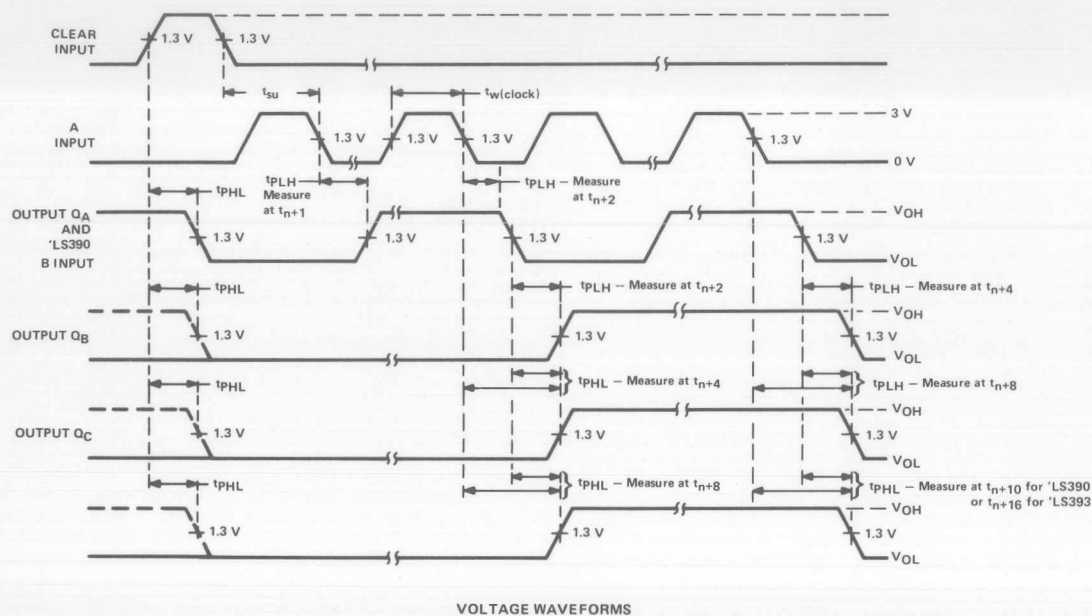
NOTE 4: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

PARAMETER	TEST CONDITIONS	SN54LS390		SN54LS393		SN74LS390		SN74LS393	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
V_{IH} High-level input voltage	$V_{CC} = 5\text{ V}$	2.0		2.0		2.0		2.0	
V_{IL} Low-level input voltage	$V_{CC} = 5\text{ V}$		0.8		0.8		0.8		0.8
V_{IK} Input clamp voltage	$V_{CC} = 5\text{ V}$, $I_K = -1\text{ mA}$		-1.5		-1.5		-1.5		-1.5
V_{OH} High-level output voltage	$V_{CC} = 5\text{ V}$, $I_{OH} = -40\text{ }\mu\text{A}$	2.0		2.0		2.0		2.0	
V_{OL} Low-level output voltage	$V_{CC} = 5\text{ V}$, $I_{OL} = 40\text{ }\mu\text{A}$		0.4		0.4		0.4		0.4
I_C Input current at maximum input voltage	$V_{CC} = 5\text{ V}$, $V_I = V_{OH}$		0.1		0.1		0.1		0.1
I_C Input current at minimum input voltage	$V_{CC} = 5\text{ V}$, $V_I = V_{OL}$		0.1		0.1		0.1		0.1
I_{IH} High-level input current	$V_{CC} = 5\text{ V}$, $V_I = V_{OH}$		0.1		0.1		0.1		0.1
I_{IL} Low-level input current	$V_{CC} = 5\text{ V}$, $V_I = V_{OL}$		0.1		0.1		0.1		0.1
I_{OZ} Standby output current	$V_{CC} = 5\text{ V}$, $V_O = V_{OL}$		0.1		0.1		0.1		0.1
I_{CC} Supply current	$V_{CC} = 5\text{ V}$, $V_I = V_{OH}$		0.1		0.1		0.1		0.1

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR = 1 MHz, duty cycle = 50 %, $Z_{out} \approx 50$ ohms.

FIGURE 2

3 TTL DEVICES

TYPES SN54LS395A, SN74LS395A

4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

OCTOBER 1976—REVISED DECEMBER 1983

- Three-State, 4 Bit, Cascadable, Parallel-In, Parallel-Out Registers
- 'LS395A Offers Three Times the Sink-Current Capability of 'LS395
- Low Power Dissipation . . . 75 mW Typical (Enabled)
- Applications:
 - N-Bit Serial-To-Parallel Converter
 - N-Bit Parallel-To-Serial Converter
 - N-Bit Storage Register

description

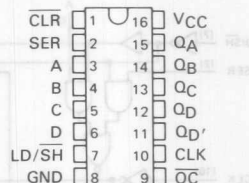
These 4-bit registers feature parallel inputs, parallel outputs, and clock (CLK), serial (SER), load shift (LD/SH), output control (OC) and direct overriding clear (CLR) inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at Q_D' is still available for cascading.

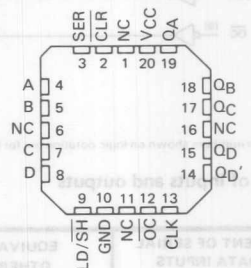
SN54LS395A . . . J OR W PACKAGE
SN74LS395A . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS395A . . . FK PACKAGE
SN74LS395A

(TOP VIEW)



NC - No internal connection

3
TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-917

Pin numbers shown on logic notation are for D, J or N packages

TTL DEVICES



TYPES SN54LS395A, SN74LS395A 4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

TIME	INPUTS				3-STATE OUTPUTS				CASCADE
	CLR	LD/SH	CLK	SER	PARALLEL A B C D	Q _A	Q _B	Q _C	Q _D
V _{CC}	L	X	X	X	X X X X	L	L	L	L
V _{CC}	H	H	H	X	X X X X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
V _{CC}	H	H	L	X	a b c d	a	b	c	d
V _{CC}	H	L	H	X	X X X X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
V _{CC}	H	L	L	H	X X X X	H	Q _{An}	Q _{Bn}	Q _{Cn}
V _{CC}	H	L	L	L	X X X X	L	Q _{An}	Q _{Bn}	Q _{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_{D'} are not affected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS395A	–55°C to 125°C
SN74LS395A	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS395A			SN74LS395A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	Q _A , Q _B , Q _C , Q _D	-1			-2.6			mA
	Q _{D'}	-400			-400			μA
Low-level output current, I _{OL}	Q _A , Q _B , Q _C , Q _D	12			24			mA
	Q _{D'}	4			8			mA
Clock frequency, f _{clock}		0	30		0	30		MHz
Width of clock pulse, t _{w(clock)}		16			16			ns
Setup time, high-level or low-level data, t _{su}	LD/SH	40			40			ns
	All other inputs	20			20			ns
Hold time, high-level or low-level data, t _h		10			10			ns
Operating free-air temperature, T _A		-55	125		0	70		°C

3

TTL DEVICES

TYPES SN54LS395A, SN74LS395A

4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS395A			SN74LS395A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX		Q _A , Q _B , Q _C , Q _D	2.4	3.4		V
				Q _D	2.5	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max, V _{IH} = 2 V		Q _A , Q _B , Q _C , Q _D	I _{OL} = 12 mA	0.25	0.4	V
				Q _C , Q _D	I _{OL} = 24 mA		0.35	0.5
				Q _D	I _{OL} = 4 mA	0.25	0.4	V
				Q _D	I _{OL} = 8 mA		0.35	0.5
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _O = 2.7 V		Q _A , Q _B , Q _C , Q _D		20		μA
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _O = 0.4 V		Q _A , Q _B , Q _C , Q _D		-20		μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1		mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				20		μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V				-0.4		mA
I _{OS}	Short-circuit output current§	V _{CC} = MAX		Q _A , Q _B , Q _C , Q _D	-30	-130	-30	mA
				Q _D	-20	-100	-20	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2		Condition A	22	34	22	mA
				Condition B	21	31	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:

- A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
- B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum clock frequency	30	45		MHz
t _{PHL}	Propagation delay time, high-to-low-level output from clear	See Note 3, Q _A , Q _B , Q _C , Q _D outputs:			
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 667 Ω, C _L = 45 pF			
t _{PHL}	Propagation delay time, high-to-low-level output	Q _D output:			
t _{PZH}	Output enable time to high level	R _L = 2 kΩ, C _L = 15 pF			
t _{PZL}	Output enable time to low level				
t _{PHZ}	Output disable time from high level	C _L = 5 pF,			
t _{PLZ}	Output disable time from low level	See Note 3			

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS396, SN74LS396 OCTAL STORAGE REGISTERS

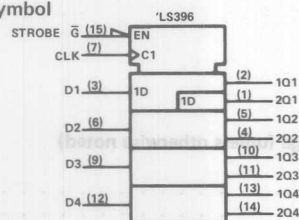
D2329, MARCH 1977—PREVISED DECEMBER 1983

- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:
N-Bit Storage Files
Hex/BCD Serial-To-Parallel Converters

description

These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

FUNCTION TABLE

STROBE \bar{G}	CLOCK	INPUTS				OUTPUTS							
		DATA				BYTE 1				BYTE 2			
		D1	D2	D3	D4	1Q1	1Q2	1Q3	1Q4	2Q1	2Q2	2Q3	2Q4
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	↑	a	b	c	d	a	b	c	d	1Q1 _n	1Q2 _n	1Q3 _n	1Q4 _n

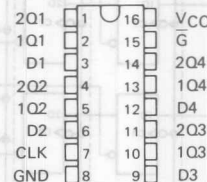
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↑ = transition from low to high level

1Q1_n, 1Q2_n, 1Q3_n, 1Q4_n = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock.

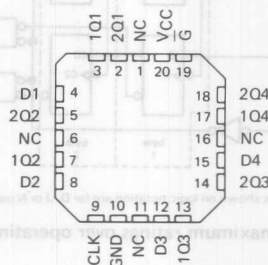
SN54LS396 . . . J OR W PACKAGE
SN74LS396 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS396 . . . FK PACKAGE
SN74LS396

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

PRODUCTION DATA

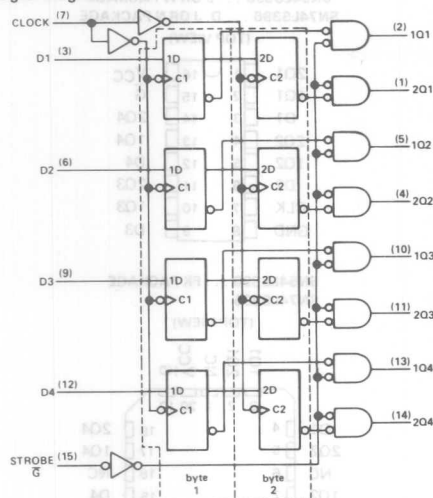
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TEXAS
INSTRUMENTS

3-921

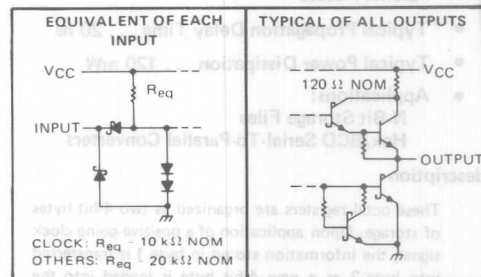
TYPES SN54LS396, SN74LS396 OCTAL STORAGE REGISTERS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



3

ITL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature: SN54LS396	-55°C to 125°C
SN74LS396	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS396			SN74LS396			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_W	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	C

TYPES SN54LS396, SN74LS396

OCTAL STORAGE REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS396			SN74LS396			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage				2			2			V
V _{IL}	Low-level input voltage				0.7			0.8			V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5			V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -400 μA		2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OL} = 4 mA			0.25 0.4			V
			I _{OL} = 8 mA		0.35 0.5						
I _I	Input current at maximum input voltage	Clock input	V _{CC} = MAX, V _I = 7 V		0.2			0.2			mA
		Other inputs				0.1					
I _{IH}	High-level input current	Clock input	V _{CC} = MAX, V _I = 2.7 V		40			40			μA
		Other inputs				20					
I _{IL}	Low-level input current	Clock input	V _{CC} = MAX, V _I = 0.4 V		-0.8			-0.8			mA
		Other inputs				-0.4					
I _{OS}	Short-circuit output current§		V _{CC} = MAX		-20	-100		-20	-100		mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 2		24 40			24 40			mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25° C.

[§] Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25° C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output from clock		20	30		
t _{PHL}	Propagation delay time, high-to-low-level output from clock	C _L = 15 pF, R _L = 2 kΩ,	20	30		ns
t _{PLH}	Propagation delay time, low-to-high-level output from strobe	See Note 3	20	30		ns
t _{PHL}	Propagation delay time, high-to-low-level output from strobe		20	30		

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

SNAL3398, SNAL3399 OCTAL STORAGE REGISTERS

Electrical characteristics over recommended operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SNAL3398		SNAL3399	
		MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage		0.1			V
V_{IS} Input clamp voltage	$V_{CC} = \text{MIN.}$ $V_I = -18 \text{ mA}$	-1.2			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 1 \text{ V}$ $I_{OH} = -450 \mu\text{A}$	2.3	2.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IL} = 2 \text{ V}$ $I_{OL} = 8 \text{ mA}$	0.25	0.3		V
t_P Propagation delay	$V_{CC} = \text{MAX.}$ $V_I = 2 \text{ V}$	0.1			ns
t_{PHL} High-level to low-level propagation delay	$V_{CC} = \text{MAX.}$ $V_I = 2 \text{ V}$	0.1			ns
t_{PLH} Low-level to high-level propagation delay	$V_{CC} = \text{MAX.}$ $V_I = 2 \text{ V}$	0.1			ns
t_{F} Fall time	$V_{CC} = \text{MAX.}$ $V_I = 2 \text{ V}$	0.1			ns
t_{R} Rise time	$V_{CC} = \text{MAX.}$ $V_I = 2 \text{ V}$	0.1			ns
I_{CC} Supply current	$V_{CC} = \text{MAX.}$ See note 1	24	40		mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
3. For more than one output shown as MIN or MAX, the value shown is the maximum of the values shown as MIN or MAX.
NOTE 1: I_{CC} measured with 4.5 V applied to all inputs and all outputs open.

Switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN		TYP		MAX	UNIT
		MIN	TYP	MAX	UNIT		
t_{PHL} Propagation delay time, high-to-low-level output from clock	$C_L = 15 \text{ pF}$	20	30		ns		
t_{PLH} Propagation delay time, low-to-high-level output from clock	$R_L = 2 \text{ k}\Omega$	20	30		ns		
t_{F} Fall time	See note 1	20	30		ns		
t_{R} Rise time		20	30		ns		

NOTE 1: See General Information section for load circuit and voltage conditions.

3 TTL DEVICES

TYPES SN54LS398, SN54LS399 SN74LS398, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

OCTOBER 1976—REVISED DECEMBER 1983

- Double-Rail Outputs on 'LS398
- Single-Rail Outputs on 'LS399
- 'LS398 is Similar to 'LS298, Which Has Inverted Clock
- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

Applications:

Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability

Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54LS157/SN74LS157 and SN54LS175/SN74LS175) in a single 16-pin or 20-pin package.

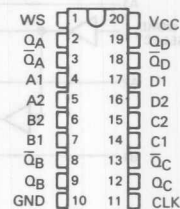
When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the positive-going edge of the clock pulse.

Typical power dissipation is 37 milliwatts. SN54LS398 and SN54LS399 are characterized for operation over the full military range of -55°C to 125°C . SN74LS398 and SN74LS399 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

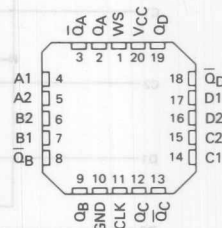
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q _A	Q _B	Q _C	Q _D
L	f	a1	b1	c1	d1
H	f	a2	b2	c2	d2
X	L	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

SN54LS398 ... J OR W PACKAGE
SN74LS398 ... DW, J OR N PACKAGE
(TOP VIEW)



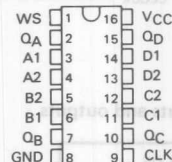
SN54LS398 ... FK PACKAGE
SN74LS398

(TOP VIEW)



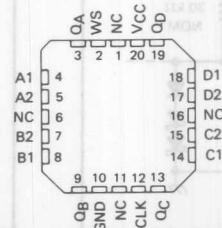
SN54LS399 ... J OR W PACKAGE
SN74LS399 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS399 ... FK PACKAGE
SN74LS399

(TOP VIEW)



NC — No internal connection

PRODUCTION DATA

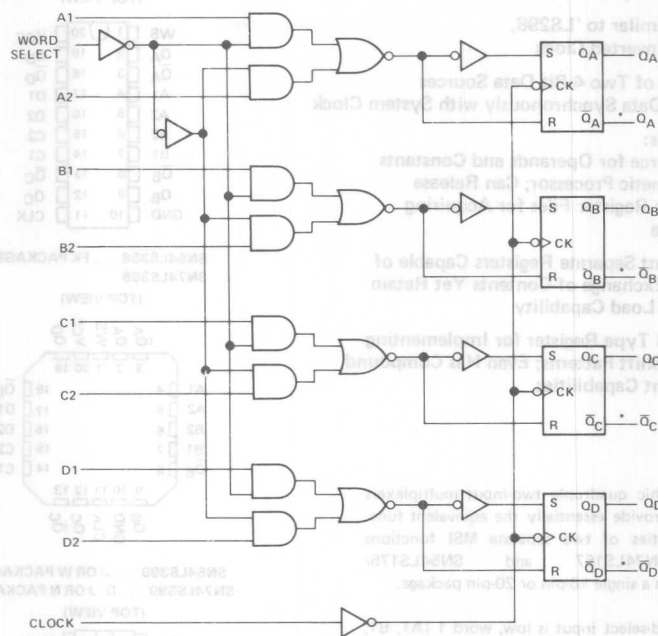
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TEXAS
INSTRUMENTS

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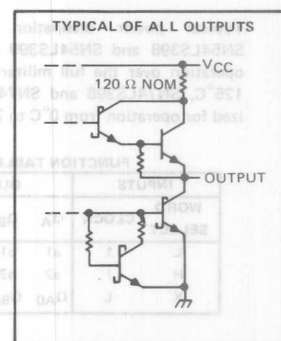
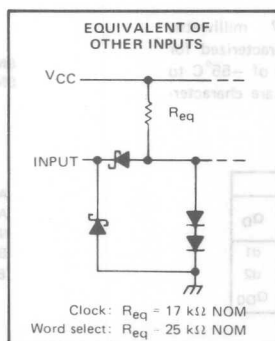
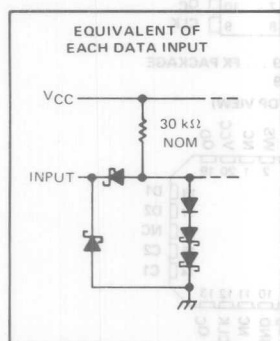
TYPES SN54LS398, SN54LS399, SN74LS398, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

logic diagram



• 'LS398 Only

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54LS398, SN54LS399, SN74LS398, SN74LS399

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS'	–55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–400			–400	μ A
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_W		20			20			ns
Setup time, t_{SU}	Data	25			25			ns
	Word select	45			45			
Hold time, t_H	Data	0			0			ns
	Word select	0			0			
Operating free-air temperature, T_A		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL\text{max}}$, $V_{IH} = 2 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL\text{max}}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4 0.35 0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			–0.4			–0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		7.3	13		7.3	13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$,		18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Note 3		21	32	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

QUADRUPEL 2-INPUT MULTIPLEXERS WITH STORAGE TYPE 52AL5388, 52AL5389, 52AL5390, 52AL5391

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	1 V
Input voltage	1 V
Operating free-air temperature range: 52AL5388, 52AL5390	-55°C to 125°C
Operating free-air temperature range: 52AL5391	0°C to 70°C
Storage temperature range	-55°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	TEST CONDITIONS	52AL5388, 52AL5390		52AL5391		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		0	1	0	1	V
High-level output current, I_{OH}		-400		-400		mA
Low-level output current, I_{OL}		0		0		mA
Setup time, t_{SU}	With 10-pF clock pulse, input or low-level, 10%	20		20		ns
		20		20		ns
		45		45		ns
		0		0		ns
Hold time, t_{H}	With 10-pF clock pulse, input or low-level, 10%	20		20		ns
		20		20		ns
		45		45		ns
		0		0		ns
Operating free-air temperature, T_A		-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	52AL5388, 52AL5390		52AL5391		UNIT
		MIN	MAX	MIN	MAX	
High-level input voltage, V_{IH}		0		0		V
Low-level input voltage, V_{IL}		0.7		0.7		V
Input clamp voltage, V_{IK}		-1.5		-1.5		V
High-level output voltage, V_{OH}	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $I_{OH} = -400 \mu\text{A}$	0.8	0.9	0.8	0.9	V
	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $I_{OH} = -400 \mu\text{A}$	0.8	0.9	0.8	0.9	V
	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $I_{OH} = -400 \mu\text{A}$	0.8	0.9	0.8	0.9	V
	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $I_{OH} = -400 \mu\text{A}$	0.8	0.9	0.8	0.9	V
Low-level output voltage, V_{OL}	$V_{CC} = \text{MAX.}$ $V_{IL} = 0.7 \text{ V.}$ $I_{OL} = 400 \mu\text{A}$	0.1		0.1		V
	$V_{CC} = \text{MAX.}$ $V_{IL} = 0.7 \text{ V.}$ $I_{OL} = 400 \mu\text{A}$	0.1		0.1		V
	$V_{CC} = \text{MAX.}$ $V_{IL} = 0.7 \text{ V.}$ $I_{OL} = 400 \mu\text{A}$	0.1		0.1		V
	$V_{CC} = \text{MAX.}$ $V_{IL} = 0.7 \text{ V.}$ $I_{OL} = 400 \mu\text{A}$	0.1		0.1		V
Input current at maximum input voltage, I_{IH}		20		20		mA
Input current at low-level input voltage, I_{IL}		-0.4		-0.4		mA
Low-level input current, I_{IK}		-100		-100		mA
Short-circuit output current, I_{OS}		1.3		1.3		mA
Supply current, I_{CC}		1.3		1.3		mA

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

For typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

For typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

For typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

For typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

For typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

For typical values at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	52AL5388, 52AL5390		52AL5391		UNIT
		MIN	MAX	MIN	MAX	
Propagation delay time, low-to-high-level output, t_{PLH}	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$	18		18		ns
Propagation delay time, high-to-low-level output, t_{PLL}	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$	21		21		ns

NOTE 2: See General Information Section for load circuit and waveform waveforms.

TYPES SN54S412, SN74S412 (TIM8212) MULTI-MODE BUFFERED LATCHES

OCTOBER 1975—REVISED DECEMBER 1983

- PNP Inputs and 3-State Outputs Maximize I/O and Data Bus Capabilities
- Data Latch Transparency Permits Asynchronous or Latched Receiver Modes
- Mode and Select Inputs Permit Storing With Outputs Enabled or Disabled
- Strobe-Controlled Flag Flip-Flop Indicates Status or Interrupt
- Asynchronous Clear Sets All Eight Data Latches Low and Initializes Status Flag
- High-Level Output Voltage, Typically 4 V, Drives Most MOS Functions Directly
- Direct Replacement for Intel 3212 or 8212 in Most Applications

description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The three-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides package busy or request interrupt commands. The outputs, with a 4-volt typical high-level voltage, are compatible for driving low-threshold MOS directly.

DATA LATCHES

The eight data latches are fully transparent when the internal gate enable, G, input is high and the outputs are enabled (OE = H). Latch transparency is selected by the mode control (M), select ($\bar{S}1$ and S2), and the strobe (STB) inputs and during transparency each data output (DO_i) follows its respective data input (DI_i). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See data latches function table.

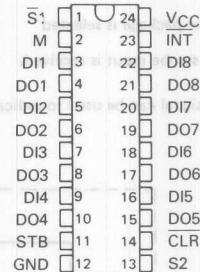
MODE SELECTION

An input mode or an output mode is selectable from this single input line. In the input mode, MD = L, the eight data latch inputs are enabled when the strobe is high regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\bar{S}1$ and S2) inputs. See data latches function table.

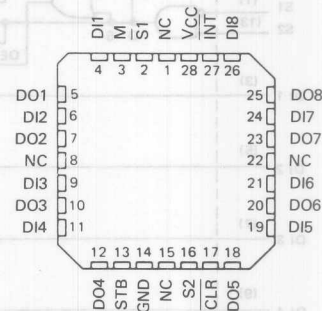
SN54S412 ... J PACKAGE
SN74S412 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54S412 ... FK PACKAGE
SN74S412

(TOP VIEW)



NC - No internal connection

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TEXAS
INSTRUMENTS

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TYPES SN54S412, SN74S412 (TIM8212) MULTI-MODE BUFFERED LATCHES

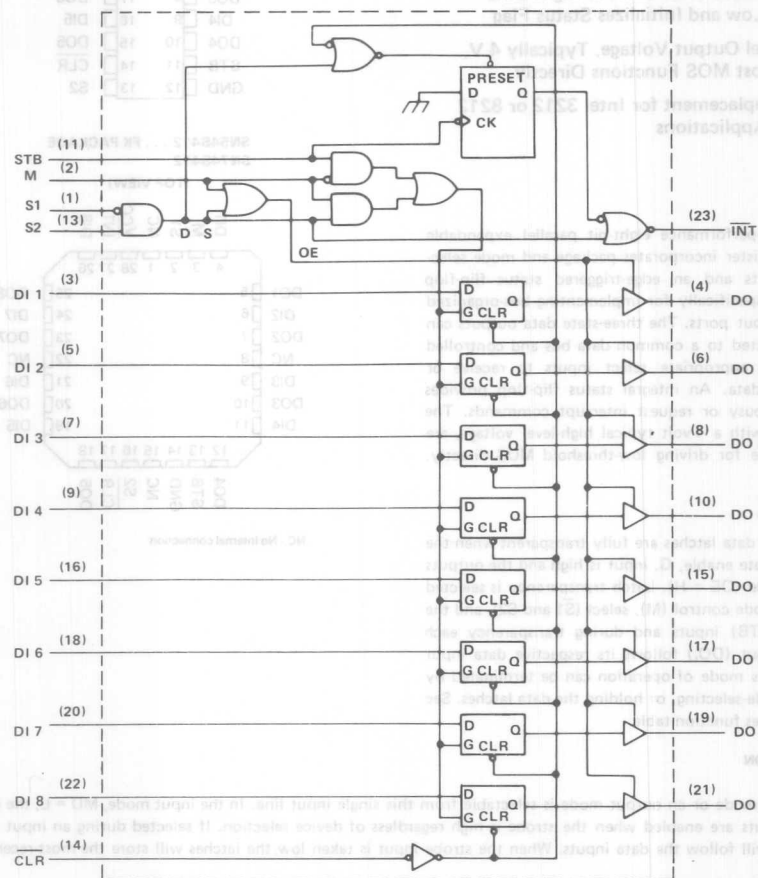
STATUS FLIP-FLOP

The status flip-flop provides a low-level output signal when:

- the package is selected
- a strobe input is received.

This status signal can be used to indicate that the register is busy or to initiate an interrupt type command.

logic diagram

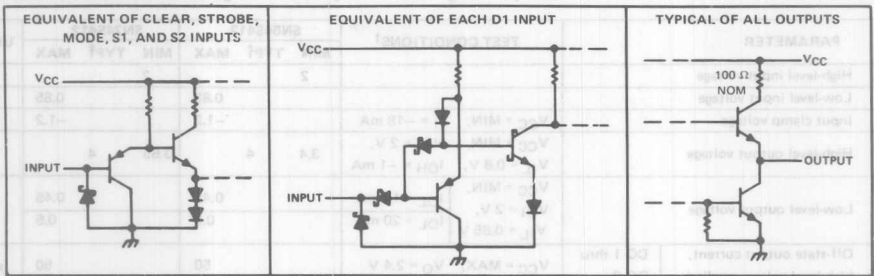


Pin numbers shown on logic notation are for DW, J or N packages.

3 TTL DEVICES

TYPES SN54S412, SN74S412 (TIM8212) MULTI-MODE BUFFERED LATCHES

schematics of inputs and outputs



DATA LATCHES FUNCTION TABLE

FUNCTION	CLEAR	M	S1	S2	STB	DATA IN	DATA OUT
Clear	L	H	H	X	X	X	L
	L	L	H	L	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q _O
	H	L	L	H	L	X	Q _O
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

STATUS FLIP-FLOP FUNCTION TABLE

CLEAR	S1	S2	STB	INT
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high impedance (off)
↓ = transition from low to high level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S412	-55°C to 125°C
SN74S412	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54S412			SN74S412			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}			4.5	5	5.5	4.75	5	5.25	V
Pulse width, t _w	STB or S1 · S2		25	Input high		25	Input high		ns
(see Figures 1, 2, and 4)			25	Input low		25	Input low		
Setup time, t _{su} (see Figure 3)			15↓	Setup time		15↓	Setup time		ns
Hold time, t _h (see Figures 1 and 3)			20↓	Hold time		20↓	Hold time		ns
Operating free-air temperature, T _A			−55	125		0	70		°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

TYPES SN54S412, SN74S412 (T1M8212) MULTI-MODE BUFFERED LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54S412			SN74S412			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage					2			2			V
V _{IL}	Low-level input voltage							0.85			0.85	V
V _{IK}	Input clamp voltage		V _{CC} = MIN; I _I = -18 mA					-1.2			-1.2	V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA			3.4	4		3.65	4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.85 V	I _{OL} = 15 mA				0.45			0.45	V
				I _{OL} = 20 mA				0.5			0.5	
I _{OZH}	Off-state output current, high-level voltage applied	DO 1 thru DO 8	V _{CC} = MAX, V _O = 2.4 V					50			50	µA
I _{OZL}	Off-state output current, low-level voltage applied	DO 1 thru DO 8	V _{CC} = MAX, V _O = 0.5 V					-50			-50	µA
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 5.5 V					1			1	mA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 5.25 V					20			10	µA
I _{IL}	Low-level input current	$\bar{S}1$	V _{CC} = MAX, V _I = 0.4 V					-1			-1	mA
		M						-0.75			-0.75	
		All others						-0.25			-0.25	
I _{OS}	Short-circuit output current§		V _{CC} = MAX			-20		-65	-20		-65	mA
I _{CC}	Supply current		V _{CC} = MAX, see Note 2				82			82	130	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, clear input at 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	STB, $\bar{S}1$, or S2	Any	1	C _L = 30 pF, See Note 3		18	27	ns
t _{PHL}		DO				15	25	
t _{PLH}	CLR	Any DO	2			18	27	ns
t _{PHL}						12	20	
t _{PLH}	DI _i	DO _i	3			10	20	ns
t _{PHL}						12	20	
t _{PLH}	$\bar{S}1$ or S2	INT	4	C _L = 30 pF, See Note 3		16	25	ns
t _{PHL}	STB	INT	4			21	35	
t _{PZH}	$\bar{S}1$, S2, or M	Any DO	5	C _L = 30 pF, See Note 3		25	40	ns
t _{PZL}						9	20	
t _{PHZ}	$\bar{S}1$, S2, or M	Any DO	5			12	20	ns
t _{PLZ}								

t_{PLH} propagation delay time, low-to-high-level output

t_{PHL} propagation delay time, high-to-low-level output

t_{PZH} output enable time to high level

t_{PZL} output enable time to low level

t_{PHZ} output disable time from high level

t_{PLZ} output disable time from low level

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TTL DEVICES 3

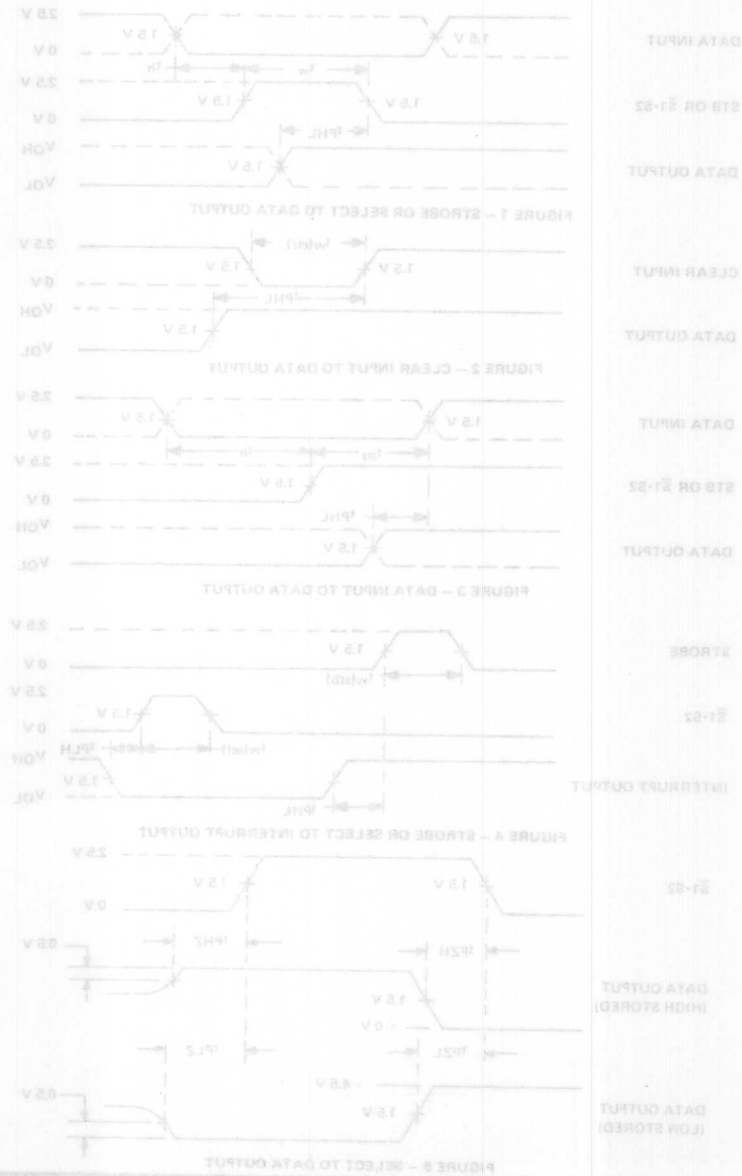
Timing diagram for the 74VHC123 showing the relationship between the Strobe, S1-S2, and Interrupt Output signals. The diagram includes the following parameters:

- Strobe:** A pulse with a width of 1.5 V. The pulse width is labeled $t_w(stb)$.
- S1-S2:** A pulse with a width of 1.5 V. The pulse width is labeled $t_w(sel)$.
- Interrupt Output:** A pulse with a width of 1.5 V. The pulse width is labeled t_{PLH} (low-to-high) and t_{PHL} (high-to-low).

The timing diagram illustrates the input and output waveforms for the 74VHC04. The input signal $\overline{S1-S2}$ is shown at the top, with a high level at 1.5 V and a low level at 0 V. The output signal is shown at the bottom, with a high level at 1.5 V and a low level at 0 V. The propagation delay t_{PZH} is the time from the input rising to the output rising. The propagation delay t_{PHZ} is the time from the input falling to the output falling. The output is shown with a 0.5 V overshoot. The input is shown with a 1.5 V overshoot. The output is shown with a 0.5 V overshoot. The input is shown with a 1.5 V overshoot. The output is shown with a 0.5 V overshoot.

TEXAS
INSTRUMENTS 

PARAMETER MEASUREMENT INFORMATION



3 TTL DEVICES

TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

D2536, JANUARY 1980

- Will Not Trigger from Clear
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- 'LS422 Has Internal Timing Resistor

description

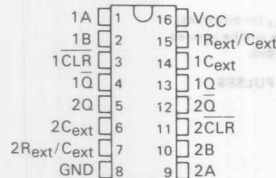
The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

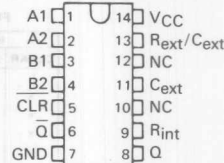
The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond. The 'LS422 R_{int} is nominally 10 k ohms.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS422 and SN74LS423 are characterized for operation from 0°C to 70°C .

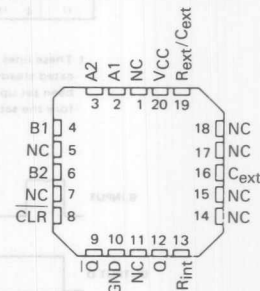
SN54LS423 ... J OR W PACKAGE
SN74LS423 ... D, J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



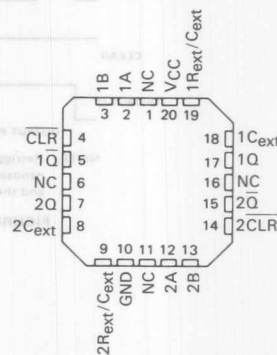
SN54LS422 ... J OR W PACKAGE
SN74LS422 ... D, J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS422 ... FK PACKAGE
SN74LS422
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS423 ... FK PACKAGE
SN74LS423
(TOP VIEW) (SEE NOTES 1 THRU 4)



- NOTES:
1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
 2. To use the internal timing resistor of 'LS422, connect R_{int} to V_{CC} .
 3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
 4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC} .

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TEXAS
INSTRUMENTS

3-935

TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

description (continued)

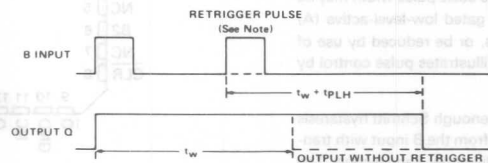
**'LS422
FUNCTION TABLE**

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	\bar{Q}
L	X	X	X	X	H	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	L	H	L	L
H	L	X	X	L	L	L
H	X	L	L	H	L	L
H	X	L	X	L	L	L
H	X	X	L	L	L	L
H	X	X	X	L	L	L
H	L	L	L	L	L	L

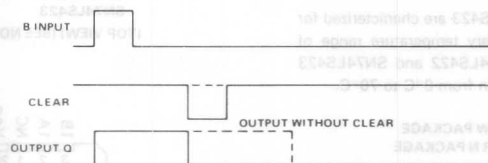
**'LS423
FUNCTION TABLE**

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	L	L	L
H	X	L	L	L
H	L	X	L	L
H	X	X	L	L

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.



OUTPUT PULSE CONTROL USING RETRIGGER PULSE



OUTPUT PULSE CONTROL USING CLEAR INPUT

NOTE: Retrigger pulses starting before 0.22 C_{ext} (in picofarads) nanoseconds after the initial trigger pulse will be ignored, and the output pulse will remain unchanged.

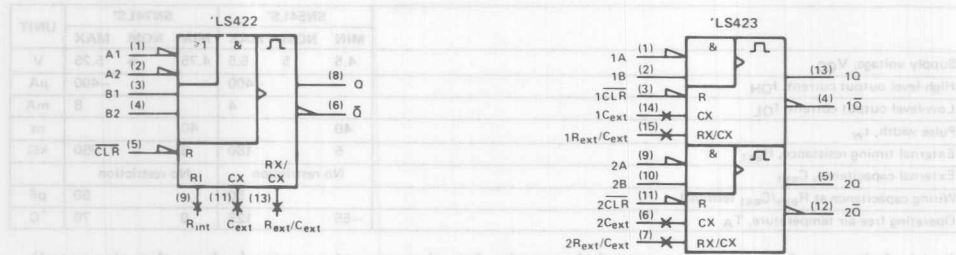
FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

3

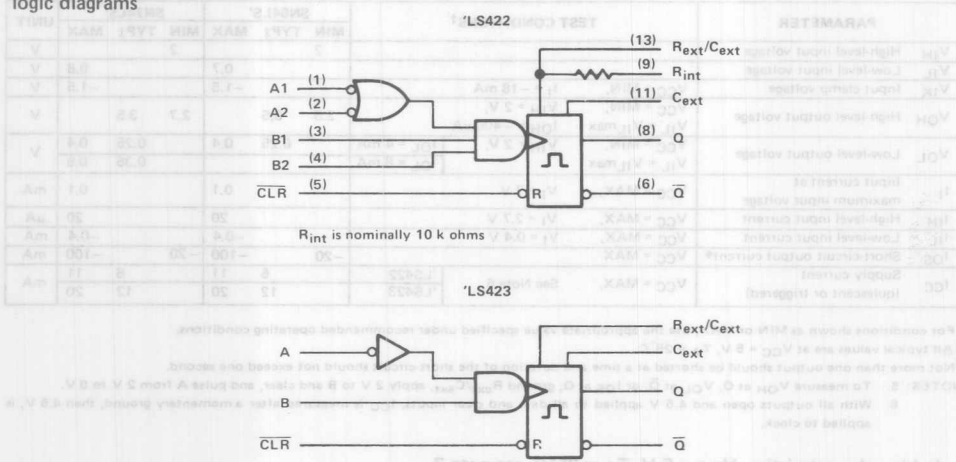
TTL DEVICES

TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

logic symbols



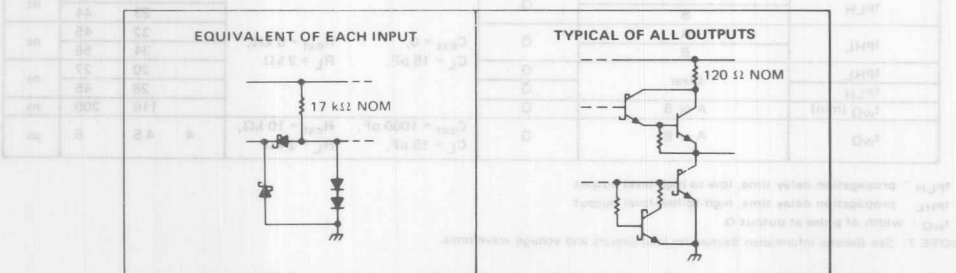
logic diagrams



R_{int} is nominally 10 k ohms

Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54LS ¹			SN74LS ¹			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	k Ω
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS ¹			SN74LS ¹			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL \text{ max}}$ $I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL \text{ max}}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current [¶]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current (quiescent or triggered)	$V_{CC} = \text{MAX}$, See Note 6							mA
		LS422			LS423			
			6	11		6	11	
			12	20		12	20	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[¶]Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 5. To measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q, ground R_{ext}/C_{ext} , apply 2 V to B and clear, and pulse A from 2 V to 0 V.

6. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, see note 7

PARAMETER [§]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_{ext} = 0$, $C_L = 15 \text{ pF}$, $R_{ext} = 5 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$		23	33	ns
	B	Q			23	44	
t_{PHL}	A	\bar{Q}			32	45	ns
	B	\bar{Q}			34	56	
t_{PHL}	Clear	Q			20	27	ns
t_{PLH}	Clear	\bar{Q}			28	45	
$t_{wQ} \text{ (min)}$	A or B	Q	$C_{ext} = 1000 \text{ pF}$, $C_L = 15 \text{ pF}$, $R_{ext} = 10 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$		116	200	ns
t_{wQ}	A or B	Q		4	4.5	5	

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{wQ} = width of pulse at output Q

NOTE 7: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR 'LS422, 'LS423†

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF, use Figure 3, or may be defined as:

$$t_w \approx K \cdot R_T \cdot C_{ext}$$

When $C_{ext} \geq 1 \mu F$, the output pulse width is defined as:

$$t_w \approx 0.33 \cdot R_T \cdot C_{ext}$$

Where

K is multiplier factor, see Figure 4

R_T is in K ohms (internal or external timing resistance)

C_{ext} is in pF

t_w is in nanoseconds

For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS422 and 'LS423, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.

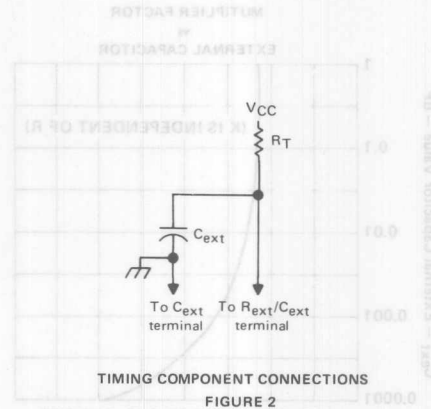


FIGURE 2

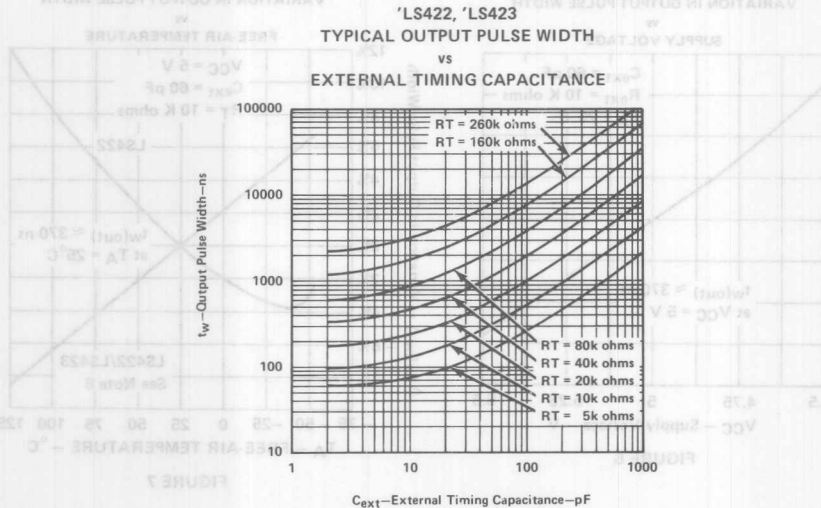


FIGURE 3

† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

TYPICAL APPLICATION DATA FOR 'LS422, 'LS423 †

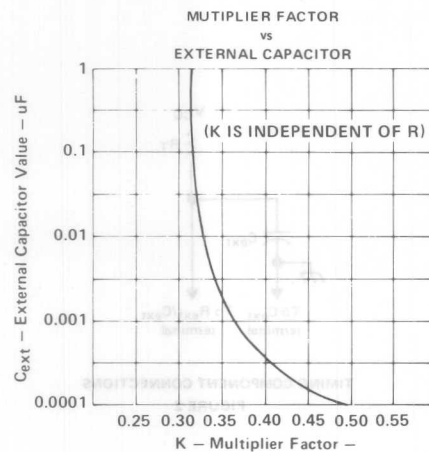


FIGURE 4

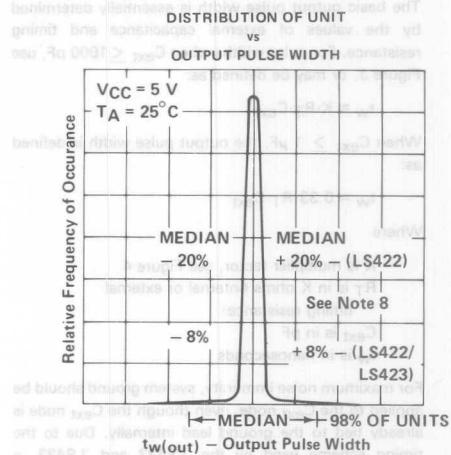


FIGURE 5

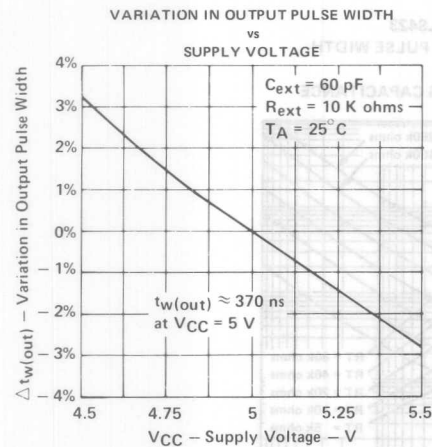


FIGURE 6

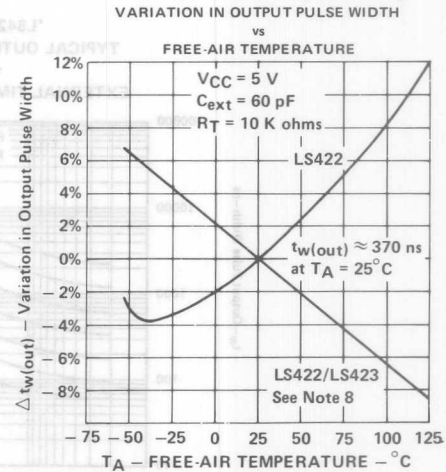


FIGURE 7

NOTE 8: For the LS422, the internal timing resistor, R_{int} was used. For the LS422/423, an external timing resistor was used for R_T .
† Data for temperatures below $0^\circ C$ and above $70^\circ C$ and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS422 and SN54LS423 only.

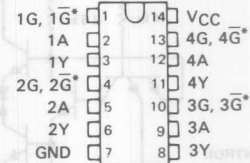
TYPES SN54425, SN74425

QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

REVISED DECEMBER 1983

- Quad Bus Buffers
- 3-State Outputs
- Separate Control for Each Channel

SN54425 ... J OR W PACKAGE
SN74425 ... J OR N PACKAGE
(TOP VIEW)

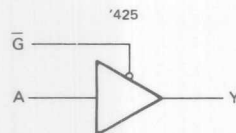


*G on '425

description

These bus buffers feature three-state outputs that, when enabled, have the low impedance characteristics of a TTL output with additional drive capability at high logic levels to permit driving heavily loaded bus lines without external pull-up resistors, when disabled, both output transistors are turned off presenting a high-impedance state to the bus so the output will act neither as a significant load nor as a driver. The outputs are disabled when \bar{G} is high.

logic diagram (each gate)



positive logic: $Y = A$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54*	-55°C to 125°C
SN74*	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-941

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TTL DEVICES

schematic (each gate)



3-942

TYPES SN54425, SN74425 QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54425			SN74425			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-2			-5.2	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54425			SN74425			UNIT
				MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA					-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V	I _{OH} = -2 V		2.4	3.3		2.4	3.1		V
		I _{OH} = -5.2 V								
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA	V _{IL} = 0.8 V,				0.4			0.4	V
I _{OZ}	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = 0.8 V	V _O = 2.4 V				40			40	μA
		V _O = 0.4 V				-40			-40	
I _I	V _{CC} = MAX, V _I = 5.5 V					1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V					40			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V					-1.6			-1.6	mA
I _{OS} §	V _{CC} = MAX			-30		-70	-28		-70	mA
I _{CC}	V _{CC} = MAX, (see Note 2)	'425			32	54		32	54	mA
		'426			36	62		36	62	

† For condition shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time.

NOTE 2: Data inputs = 0 V; output control = 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25° C (see note 3)

PARAMETER	TEST CONDITIONS		SN54/74425			UNIT
			MIN	TYP	MAX	
t _{PLH}	R _L = 400 Ω, C _L = 50 pF			8	13	ns
t _{PHL}				12	18	ns
t _{PZH}				11	17	ns
t _{PZL}				16	25	ns
t _{PHZ}	R _L = 400 Ω, C _L = 5 pF			5	8	ns
t _{PLZ}				7	12	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES

QUADRIPLER BUS BUFFERS WITH 3-STATE OUTPUTS TYPED SN54422, SN74422

recommended operating conditions

PARAMETER	SN54422	SN74422	UNIT
V _{CC} Supply voltage	MIN NOM MAX	MIN NOM MAX	V
V _{IH} High-level input voltage	4.5 5 5.5	4.5 5 5.5	V
V _{IL} Low-level input voltage	0.5	0.5	V
I _{OH} High-level output current	0	0	mA
I _{OL} Low-level output current	15	15	mA
T _A Operating free-air temperature	0 75 125	0 75 125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		UNIT
	MIN	MAX	
V _{IC}	V _{CC} = MIN V _{IH} = 1.5 V	1.5	V
V _{OH}	V _{CC} = MIN V _{IH} = 1.5 V I _{OH} = -2.5 V	2.5	V
V _{OL}	V _{CC} = MIN V _{IH} = 1.5 V I _{OL} = 15 mA	0.5	V
I _{OS}	V _{CC} = MAX V _{IH} = 1.5 V V _{OL} = 0.4 V	40	mA
I _I	V _{CC} = MAX V _I = 0.5 V	1	mA
I _{IH}	V _{CC} = MAX V _I = 1.4 V	40	mA
I _{IL}	V _{CC} = MAX V _I = 0.4 V	15	mA
I _{OS2}	V _{CC} = MAX	40	mA
I _{CC}	V _{CC} = MAX (see note 3)	450	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

2. All typical values are at V_{CC} = 5 V, T_A = 25°C.

3. Input must be at logic 0 or logic 1; output should be shown as a note.

NOTE 3: Data input = 0 V, output current = 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	TEST CONDITIONS		UNIT
	MIN	MAX	
t _{PLH}	R _L = 100 Ω	8	ns
t _{PHL}	R _L = 100 Ω	12	ns
t _{PLZ}	C _L = 50 pF	12	ns
t _{PHZ}	C _L = 50 pF	12	ns
t _{PLZ}	R _L = 100 Ω	8	ns
t _{PHZ}	R _L = 100 Ω	12	ns

NOTE 3: See General Information Section for load circuit and voltage waveform.

3

TTL DEVICES

TYPES SN54LS440 THRU SN54LS444, SN54LS448 SN74LS440 THRU SN74LS444, SN74LS448 QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

D2425, AUGUST 1979

- 3-Way Asynchronous Communication
- On-Chip Bus Selection Decoding
- Input Hysteresis Improves Noise Margin
- Choice of Open-Collector or 3-State Outputs

description

These bus transceivers are designed for asynchronous three-way communication between four-line data buses. They give the designer a choice of selecting inverting, noninverting, or a combination of inverting and noninverting data paths with either 3-state or open-collector outputs.

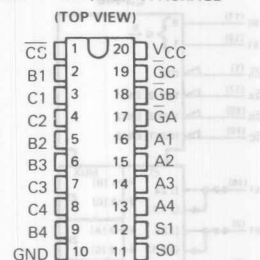
The S0 and S1 inputs select the bus from which data are to be transferred. The \bar{G} inputs enable the bus or buses to which data are to be transferred. The port for any bus selected for input and any other bus not enabled for output will be at high impedance including those of the open-collector devices.

The SN54LS440 through SN54LS444 and SN54LS448 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS440 through SN74LS444 and SN74LS448 are characterized for operation from 0°C to 70°C .

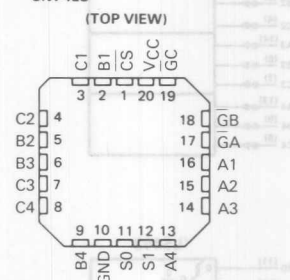
FUNCTION TABLE

INPUTS						TRANSFERS BETWEEN BUSES		
\bar{CS}	S1	S0	\bar{GA}	\bar{GB}	\bar{GC}	'LS440	'LS441	'LS444
						'LS442	'LS443	'LS448
H	X	X	X	X	X	None	None	None
X	H	H	X	X	X	None	None	None
X	X	X	H	H	H	None	None	None
X	L	L	X	H	H	None	None	None
X	L	H	X	X	H	None	None	None
X	H	L	H	H	X	None	None	None
L	L	L	X	L	L	$A \cdot B, A \cdot C$	$A \cdot B, A \cdot C$	$A \cdot B, A \cdot C$
L	L	H	L	X	L	$B \cdot C, B \cdot A$	$B \cdot C, B \cdot A$	$B \cdot C, B \cdot A$
L	H	L	L	L	X	$C \cdot A, C \cdot B$	$C \cdot A, C \cdot B$	$C \cdot A, C \cdot B$
L	L	L	X	L	H	$A \cdot B$	$A \cdot B$	$A \cdot B$
L	L	H	H	X	L	$B \cdot C$	$B \cdot C$	$B \cdot C$
L	H	L	L	H	X	$C \cdot A$	$C \cdot A$	$C \cdot A$
L	L	L	X	H	L	$A \cdot C$	$A \cdot C$	$A \cdot C$
L	L	H	L	X	H	$B \cdot A$	$B \cdot A$	$B \cdot A$
L	H	L	H	L	X	$C \cdot B$	$C \cdot B$	$C \cdot B$

SN54LS' ... J PACKAGE
SN74LS' ... DW, J OR N PACKAGE



SN54LS' ... FK PACKAGE
SN74LS' ...



DEVICE

'LS440
'LS441
'LS442
'LS443
'LS444
'LS448

OUTPUT

Open-Collector
Open-Collector
3-State
3-State
3-State
Open-Collector

LOGIC

True
Inverting
True
Inverting
True/Inverting
True/Inverting

3

TTL DEVICES

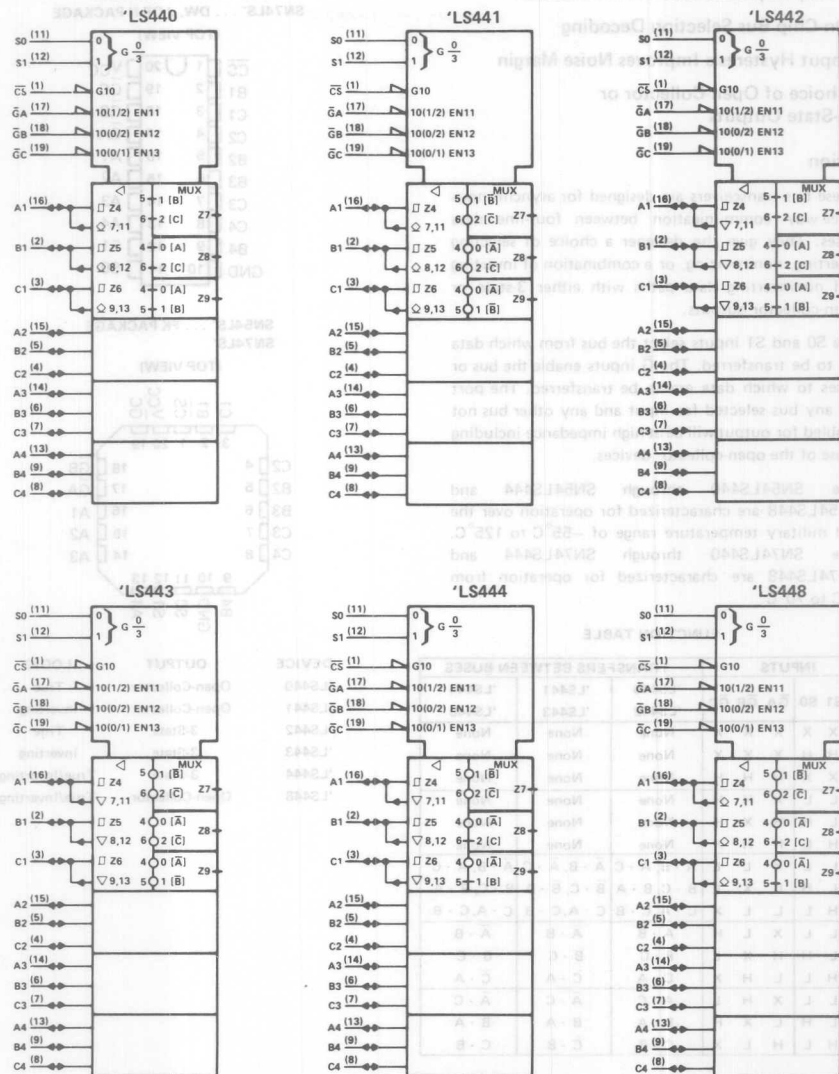
PRODUCTION DATA

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TEXAS
INSTRUMENTS

TYPES SN54LS440 THRU SN54LS444, SN54LS448,
SN74LS440 THRU SN74LS444, SN74LS448
QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

logic symbols



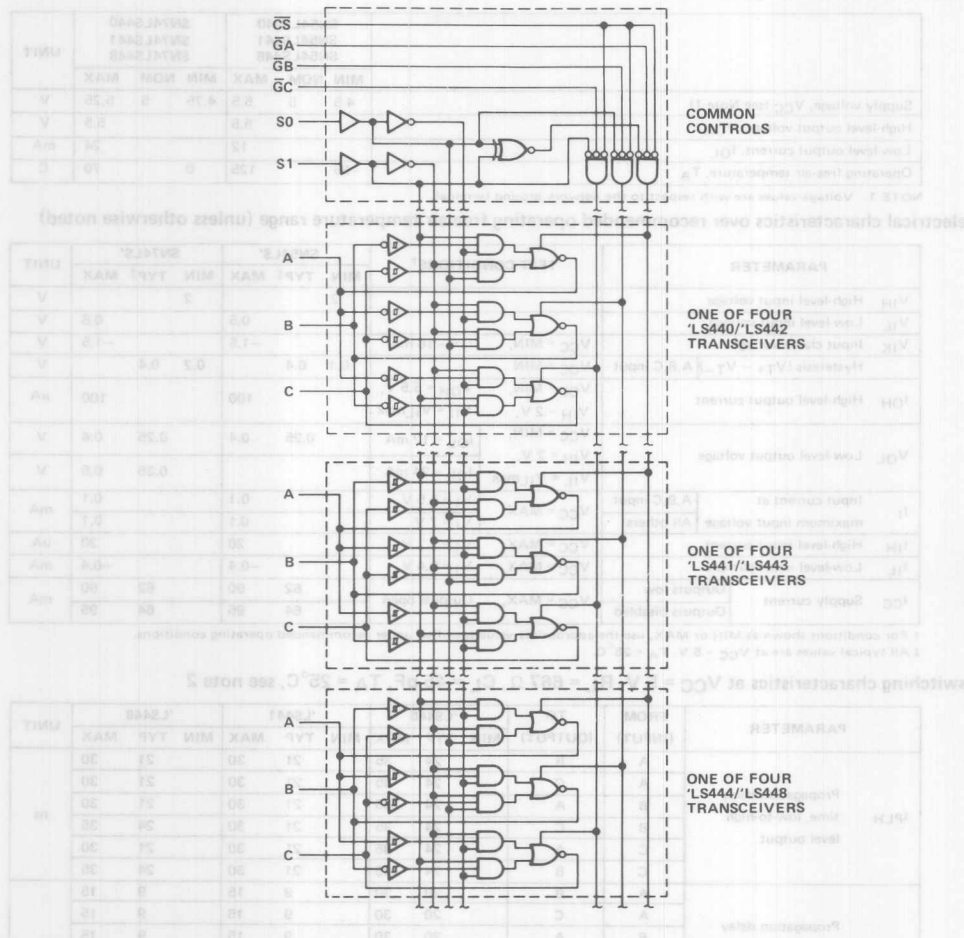
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS440 THRU SN54LS444, SN54LS448, SN74LS440 THRU SN74LS444, SN74LS448 QUADUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

logic diagram (composite showing one of four transceivers from each type, positive logic)



3

TTL DEVICES

TYPES SN54LS440, SN54LS441, SN54LS448,
SN74LS440, SN74LS441, SN74LS448
QUAD TRIDIRECTIONAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS440 SN54LS441 SN54LS448			SN74LS440 SN74LS441 SN74LS448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.5			0.6	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A, B, C input	0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$			100			100	µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$							
		$I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5		V
I_I	Input current at maximum input voltage	A, B, C input			0.1			0.1	mA
		All others			0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC}	Supply current	Outputs low	62	90		62	90		mA
		Outputs disabled	64	95		64	95		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5 \text{ V}, R_L = 667 \Omega, C_L = 45 \text{ pF}, T_A = 25^\circ\text{C}$, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'LS440			'LS441			'LS448			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A → B	24	35		21	30		21	30		ns
		A → C	24	35		21	30		21	30		
		B → A	24	35		21	30		21	30		
		B → C	24	35		21	30		24	35		
		C → A	24	35		21	30		21	30		
t_{PHL}	Propagation delay time, high-to-low level output	C → B	24	35		21	30		24	35		ns
		A → B	20	30		9	15		9	15		
		A → C	20	30		9	15		9	15		
		B → A	20	30		9	15		9	15		
		B → C	20	30		9	15		20	30		
t_{PLH}	Propagation delay time, low-to-high level output	C → A	20	30		9	15		9	15		ns
		C → B	20	30		9	15		20	30		
		any \bar{G} → A, B, C	29	45		23	35		25	40		
		S0, S1 → A, B, C	33	50		27	40		26	40		
		CS → A, B, C	31	45		26	40		25	40		
t_{PHL}	Propagation delay time, high-to-low level output	any \bar{G} → A, B, C	27	40		20	30		22	35		ns
		S0, S1 → A, B, C	32	50		26	40		27	40		
		CS → A, B, C	28	45		21	30		22	35		

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS442, SN54LS443, SN54LS444,
SN74LS442, SN74LS443, SN74LS444
QUAD TRIDIRECTIONAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54LS442	SN54LS443	SN54LS444	SN74LS442	SN74LS443	SN74LS444	UNIT
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.5			0.6	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	A, B, C input	0.1	0.4		0.2	0.4		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	0.25	0.4		0.25	0.4		V
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}$			20			20	µA
I_{OZL} Off-state output current, low-level voltage applied	\overline{CS} at 2 V, $V_O = 0.4 \text{ V}$			-400			-400	µA
I_I Input current at maximum input voltage	A, B, C: $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ Others: $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short circuit output current	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC} Supply current	Outputs low	62	90		62	90		mA
	Outputs at Hi-Z	64	95		64	95		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

¶ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

3
TTL DEVICES

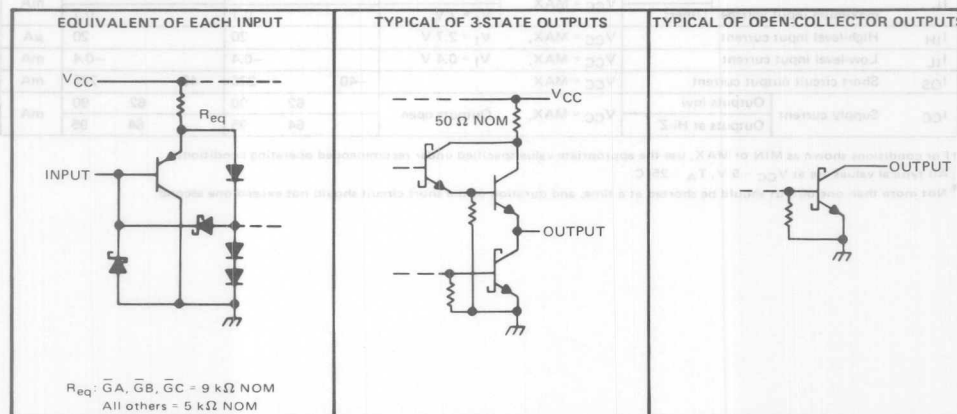
TYPES SN54LS442, SN54LS443, SN54LS444,
SN74LS442 THRU SN74LS443, SN74LS444
QUAD TRIDIRECTIONAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS442			'LS443			'LS444			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A, B	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$	10	14		9	14		9	14		ns
		A, C		10	14		9	14		9	14		
		B, A		10	14		9	14		9	14		
		B, C		10	14		9	14		9	14		
		C, A		10	14		9	14		9	14		
		C, B		10	14		9	14		10	14		
t_{PHL}	Propagation delay time, high-to-low level output	A, B		13	20		7	13		7	13		ns
		A, C		13	20		7	13		7	13		
		B, A		13	20		7	13		7	13		
		B, C		13	20		7	13		13	20		
		C, A		13	20		7	13		7	13		
		C, B		13	20		7	13		13	20		
t_{PZL}	Output enable time to low level	Any \overline{G}	$C_L = 5\text{ pF}$, $R_L = 667\ \Omega$	22	33		22	33		22	33		ns
		S_0 or S_1		28	42		28	42		28	42		
		\overline{CS}		23	36		24	36		23	36		
t_{PZH}	Output enable time to high level	\overline{G} , S \overline{CS}	A, B, C	21	32		20	32		24	32		ns
t_{PLZ}	Output disable time from low level	\overline{G} , S , \overline{CS}	A, B, C	14	25		15	25		14	25		ns
t_{PHZ}	Output disable time from high level	\overline{G} , S , \overline{CS}	A, B, C	14	25		15	25		14	25		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54LS445, SN74LS445 BCD-TO-DECIMAL DECODERS/DRIVERS

D2427, NOVEMBER 1977—REVISED DECEMBER 1983

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Low-Voltage Version of SN54LS145/
SN74LS145
- Full Decoding of Input Logic
- SN74LS445 Has 80-mA Sink-Current
Capability
- All Outputs Are Off for Invalid BCD
Input Conditions
- Low Power Dissipation . . . 35 mW
Typical

logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

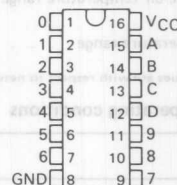
description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the output transistors will sink up to 80 milliamperes of current. Each input is one Series 54LS/74LS standard load. Inputs and outputs are entirely compatible for use with TTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

PRODUCTION DATA

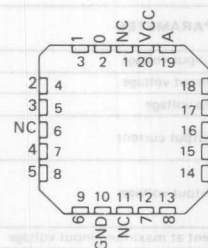
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54LS445 . . . J PACKAGE
SN74LS445 . . . D, J OR N PACKAGE
(TOP VIEW)



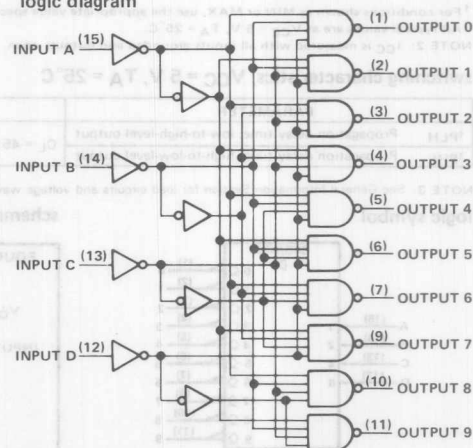
SN54LS445 . . . FK PACKAGE
SN74LS445

(TOP VIEW)



NC - No internal connection

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

TEXAS
INSTRUMENTS

3

TTL DEVICES

3-951

TYPES SN54LS445, SN74LS445 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS445	-55°C to 125°C
SN74LS445	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS445			SN74LS445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			7			7	V
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS445			SN74LS445			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$I_{O(off)}$ Off-state output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 7 \text{ V}$			250			250	μA
$V_{O(on)}$ On-state output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{IH} = 2 \text{ V}$, $I_{OL} = 24 \text{ mA}$					0.35	0.5	
	$V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 80 \text{ mA}$					2.3	3	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		20			20		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		7	13		7	13	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

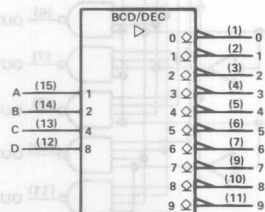
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}$, $R_L = 665 \Omega$, See Note 3		50	ns
t_{PHL} Propagation delay time, high-to-low-level output			50	ns

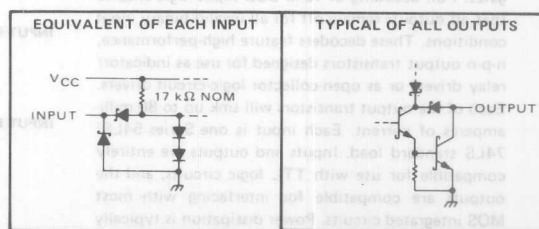
NOTE 3: See General Information Section for load circuits and voltage waveforms.

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

schematic of inputs and outputs

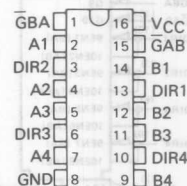


TYPES SN54LS446, SN54LS449, SN74LS446, SN74LS449 QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

D2613, OCTOBER 1980 — REVISED DECEMBER 1983

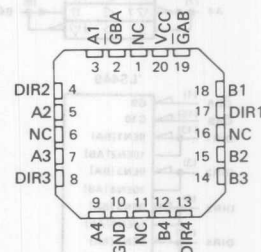
SN54LS446, SN54LS449 ... J PACKAGE
SN74LS446, SN74LS449 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS446, SN54LS449 ... FK PACKAGE
SN74LS446, SN74LS449

(TOP VIEW)



NC - No internal connection

- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce DC Loading on Bus Line
- Hysteresis at Bus Inputs Improves Noise Margins
- Flow-Thru Data Pinout (B Bus Opposite A Bus)
- Choice of True ('LS449) and Inverting ('LS446)

description

These quadruple bus transceivers are designed for data transmission from individual lines of the A bus to individual lines of the B bus or the reverse, depending on the logic levels at the direction-control pins DIR1 through DIR4. These direction controls (one for each channel) allow maximum flexibility in timing. The enable inputs $\overline{G}BA$ and $\overline{G}AB$ can be used to disable the A or B outputs respectively, or to disable both buses for effective isolation.

The SN54LS446 and SN54LS449 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS446 and SN74LS449 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

ENABLE		DIRECTION DIR	OPERATION	
$\overline{G}BA$	$\overline{G}AB$		'LS446	'LS449
H	H	X	Isolation	Isolation
X	L	H	A data to B Bus	A data to B Bus
L	X	L	B data to A Bus	B data to A Bus
X	H	H	Isolation	Isolation
H	X	L	Isolation	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

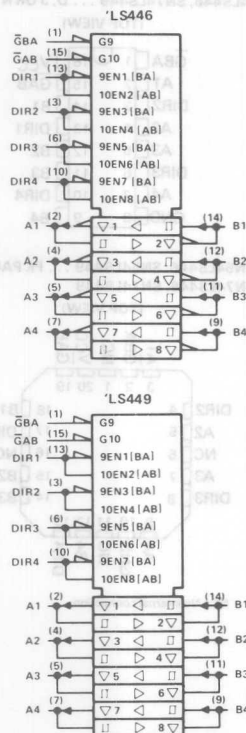
3-953

3

TTL DEVICES

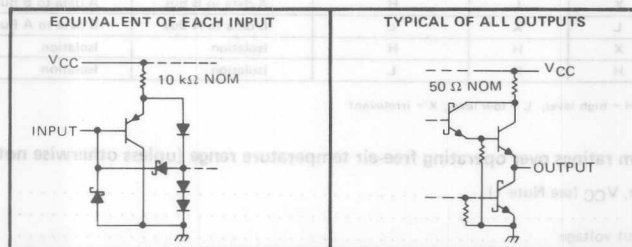
TYPES SN54LS446, SN54LS449, SN74LS446, SN74LS449 QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

logic symbols

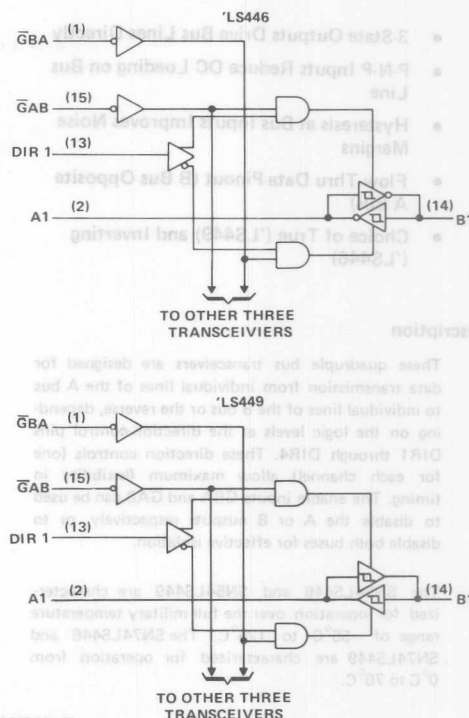


Pin numbers shown on logic notation are for D, J or N packages.

schematics of inputs and outputs



logic diagrams (positive logic)



3 TTL DEVICES

TYPES SN54LS446, SN54LS449, SN74LS446, SN74LS449 QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

recommended operating conditions

PARAMETER	SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage		0.6			0.7			V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA	−1.5			−1.5			V	
Hysteresis (V _{T+} − V _{T−}), A or B input		V _{CC} = MIN	0.1	0.4		0.2	0.4		V	
V _{OH}	High-level output voltage	V _{CC} = MIN, I _{OH} = −3 mA	2.4	3.4		2.4	3.4		V	
		V _{IL} = V _{IL max} , I _{OH} = MAX	2		2					
V _{OL}	Low-level output voltage	V _{CC} = MIN, I _{OL} = 12 mA	0.25 0.4		0.25 0.4			V		
		V _{IL} = V _{IL max} , I _{OL} = 24 mA			0.35 0.5					
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, \bar{G} at 2 V, V _O = 2.7 V	20			20			μA	
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, \bar{G} at 2 V, V _O = 0.4 V	−0.4			−0.4			mA	
I _I	Input current at maximum input voltage	A or B	V _I = 5.5 V			0.1			mA	
		$\bar{G}AB$ or $\bar{G}BA$	V _I = 2 V			0.1				
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V	20			20			μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	−0.4			−0.4			mA	
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	−40		−225	−40		−225	mA	
I _{CC}	Total supply current	'LS446	Outputs high		35	56	35		56	mA
			Outputs low		39	63	39		63	
			Outputs at Hi-Z		42	68	42		68	
		'LS449	Outputs high		42	68	42		68	
			Outputs low		47	75	47		75	
			Outputs at Hi-Z		50	80	50		80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

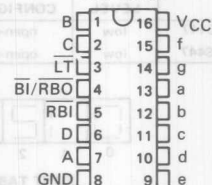
3 TTL DEVICES

NOTE 2: See General Information Section for load circuits and voltage waveforms.

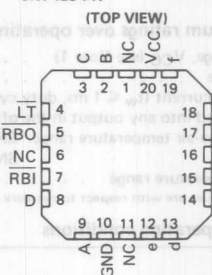
TYPES SN54LS447, SN74LS447 **BCD-TO-SEVEN-DECODERS/DRIVERS** D2428, NOVEMBER 1977—REVISED DECEMBER 1983

- Low-Voltage Version of SN54LS247/SN74LS247
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

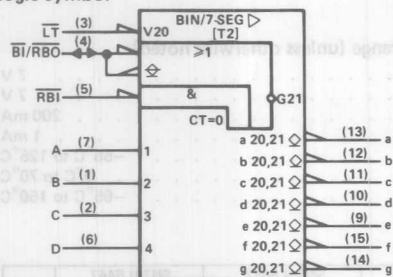
SN54LS447 ... J PACKAGE
SN74LS447 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS447 ... FK PACKAGE
SN74LS447
(TOP VIEW)



logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

NC — No internal connection

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS							BI/RBO [†]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A			a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input ($\overline{\text{BI}}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{\text{RBI}}$) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input ($\overline{\text{BI}}$), all segment outputs are off regardless of the level of any other input.

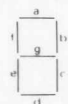
3. When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a low level (response condition).

4. When the blanking input/ripple blanking output ($\overline{\text{BI/RBO}}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

[†] $\overline{\text{BI/RBO}}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$).

TYPES SN54LS447, SN74LS447 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS447	low	open-collector	12 mA	7 V	35 mW	J
SN74LS447	low	open-collector	24 mA	7 V	35 mW	J, N



0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
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FONT TABLE T2 — NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

SEGMENT
IDENTIFICATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS447	-55°C to 125°C
SN74LS447	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS447			SN74LS447			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	B1/RBO			-50			-50	μA
Low-level output current, I_{OL}	B1/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		-55		125	0		70	$^\circ\text{C}$

3

TTL DEVICES

TYPES SN54LS447, SN74LS447
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS447			SN74LS447			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	$\overline{\text{BI}}/\overline{\text{RBO}}$ V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -50 µA	2.4	4.2		2.4	4.2		V
V _{OL}	Low-level output voltage	$\overline{\text{BI}}/\overline{\text{RBO}}$ V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
		I _{OL} = 3.2 mA					0.35	0.5	
I _{O(off)}	Off-state output current	a thru g V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _{O(off)} = 7 V		250			250		µA
V _{O(on)}	On-state output voltage	a thru g V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{O(on)} = 12 mA		0.25	0.4		0.25	0.4	V
		I _{O(on)} = 24 mA					0.35	0.5	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V		20			20		µA
I _{IL}	Low-level input current	Any input except $\overline{\text{BI}}/\overline{\text{RBO}}$ V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
		$\overline{\text{BI}}/\overline{\text{RBO}}$		-1.2			-1.2		
I _{OS}	Short-circuit output current	$\overline{\text{BI}}/\overline{\text{RBO}}$ V _{CC} = MAX	-0.3	-2		-0.3	-2		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	7	13		7	13		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{off}	Turn-off time from A input	C _L = 15 pF, R _L = 665 Ω, See Note 4			100	ns
t _{on}	Turn-on time from A input				100	
t _{off}	Turn-off time from $\overline{\text{RBI}}$ input				100	ns
t _{on}	Turn-on time from $\overline{\text{RBI}}$ input				100	

NOTE 4: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74LS47		SN74LS47	
		MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage		0.7			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -10 \text{ mA}$	-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -50 \mu\text{A}$	2.4	4.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 10 \text{ mA}$	0.25	0.4		V
$I_{O(EN)}$ On-state output current	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 10 \text{ mA}$	250			mA
$I_{O(EN)}$ On-state output voltage	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 10 \text{ mA}$	0.25	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 2 \text{ V}$	0.1			mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2 \text{ V}$	50			nA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.4			mA
I_{OS} Short-circuit output current	$V_{CC} = \text{MAX}$	-0.3			mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{See Note 2}$	3	10		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ At typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
§ I_{CC} is measured with all outputs open and all inputs at 0 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Turn-on time from A input	$C_L = 10 \text{ pF}, R_L = 600 \Omega$		100		ns
t_{PHL} Turn-off time from A input			100		ns
t_{PLT} Turn-on time from B input			100		ns
t_{PLT} Turn-on time from B input			100		ns

NOTE 4: See General Information section for load circuit and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468 OCTAL BUFFERS WITH 3-STATE OUTPUTS

D2631, JANUARY 1981—REVISED DECEMBER 1983

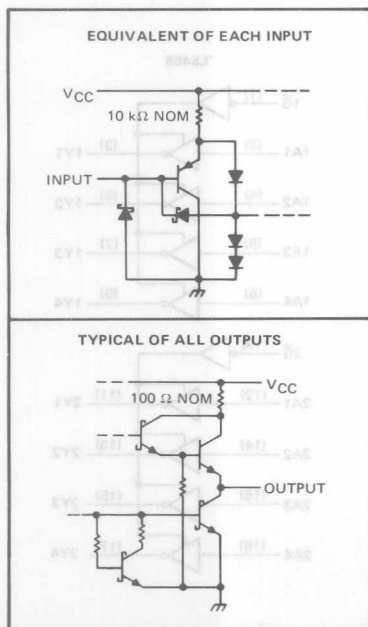
- Mechanically and Functionally Interchangeable With DM71/81LS95 thru DM71/81LS98
- P-N-P Inputs Reduce Bus Loading
- 3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for 54LS and 74LS, Respectively

DEVICE	DATA PATH
'LS465	True
'LS466	Inverting
'LS467	True
'LS468	Inverting

description

These octal buffers utilize the latest low-power Schottky technology. The 'LS465 and 'LS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'LS467 and 'LS468 have two separate active-low enable inputs each controlling four data buffers. In either case, a high level on any \bar{G} places the affected outputs at high impedance.

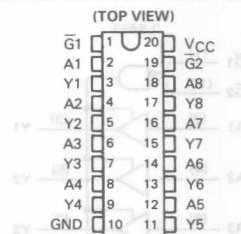
schematics of inputs and outputs



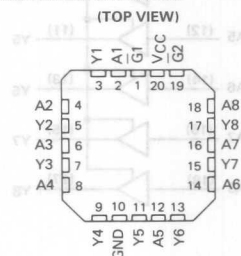
PRODUCTION DATA

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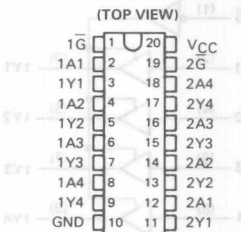
SN54LS465 AND SN54LS466 ... J PACKAGE
SN74LS465 AND SN74LS466 ... DW, J OR N PACKAGE



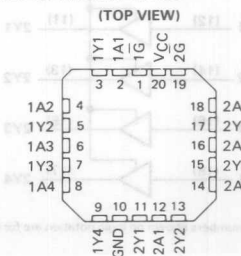
SN54LS465 AND SN54LS466 ... FK PACKAGE
SN74LS465 AND SN74LS466



SN54LS467 AND SN54LS468 ... J PACKAGE
SN74LS467 AND SN74LS468 ... DW, J OR N PACKAGE



SN54LS467 AND SN54LS468 ... FK PACKAGE
SN74LS467 AND SN74LS468



TEXAS
INSTRUMENTS

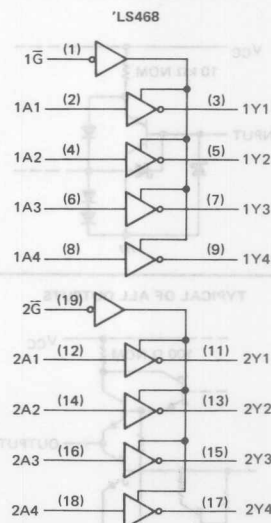
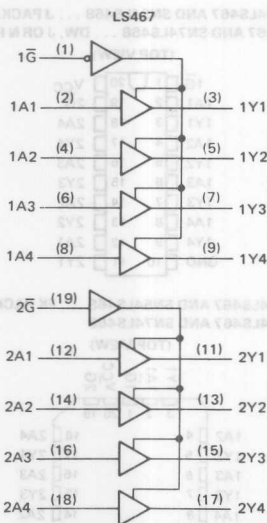
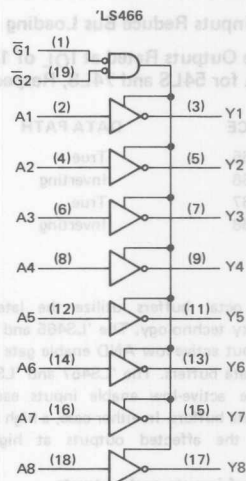
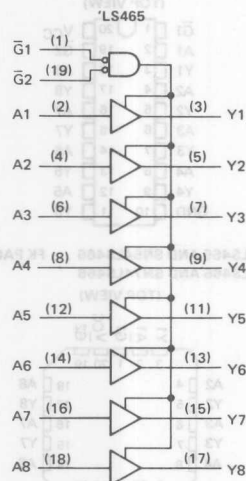
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3

TTL DEVICES

TYPES SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468 OCTAL BUFFERS WITH 3-STATE OUTPUTS

logic diagrams (positive logic)



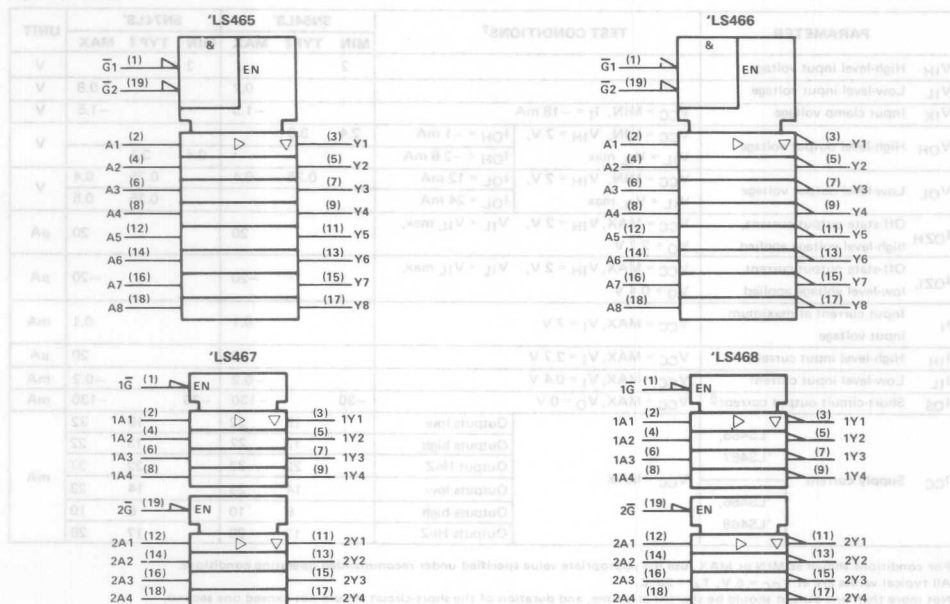
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468 OCTAL BUFFERS WITH 3-STATE OUTPUTS

logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS465 thru SN54LS468	-55°C to 125°C
SN74LS465 thru SN74LS468	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

TYPES SN54LS465 THRU SN54LS468, SN74LS465, THRU SN74LS468 OCTAL BUFFERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage					0.7			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5			V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OH} = -1 mA I _{OH} = -2.6 mA	2.4	3.3				V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 12 mA I _{OL} = 24 mA	0.25	0.4	0.25	0.4		V
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V	V _{IL} = V _{IL} max,	20			20		μA
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V	V _{IL} = V _{IL} max,	-20			-20		μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V	0.1			0.1			mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V	20			20			μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	-0.2			-0.2			mA
I _{OS}	Short-circuit output current §	V _{CC} = MAX, V _O = 0 V	-30			-130	-30	-130	mA
I _{CC}	Supply current	V _{CC} = MAX	Outputs low	19	32	19	32	mA	
			Outputs high	13	22	13	22		
			Output Hi-Z	22	37	22	37		
			Outputs low	14	23	14	23		
			Outputs high	6	10	6	10		
			Outputs Hi-Z	17	28	17	28		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

3

TTL DEVICES

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS465, 'LS467			'LS466, 'LS468			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	A _i	Y _i	R _L = 667 Ω, C _L = 45 pF	9	15		7	12		ns
t _{PHL}	A _i	Y _i		12	18		9	15		ns
t _{PZH}	G _i	Y		25	40		25	40		ns
t _{PZL}	G _i	Y	R _L = 667 Ω, C _L = 5 pF	29	45		29	45		ns
t _{PHZ}	G _i	Y		25	40		25	40		ns
t _{PLZ}	G _i	Y		30	45		30	45		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TEMP	'LS465, 'LS467			'LS466, 'LS468		
	MIN	TYP	MAX	MIN	TYP	MAX
V	0.5	0.5	0.5	0.5	0.5	0.5
A _{in}	0.5	0.5	0.5	0.5	0.5	0.5
A _{out}	0.5	0.5	0.5	0.5	0.5	0.5
Q	0.5	0.5	0.5	0.5	0.5	0.5

TYPES SN54490, SN54LS490, SN74490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

OCTOBER 1976—REVISED DECEMBER 1983

- Dual Versions of Popular SN5490A, SN54LS90, SN7490A, and SN74LS90 Counters
- Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter
- Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%
- Maximum Count Frequency ... 35 MHz Typical
- Buffered Outputs Reduce Possibility of Collector Commutation

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single '490 or 'LS490. Buffering on each output is provided to ensure that susceptibility to collector commutation is reduced significantly. All inputs are diode-clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54490 and SN54LS490 are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74490 and SN74LS490 are characterized for use in industrial systems operating from 0°C to 70°C .

BCD COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

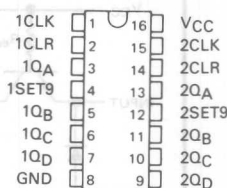
CLEAR/SET-TO-9
FUNCTION TABLE
(EACH COUNTER)

INPUTS		OUTPUTS			
CLEAR	SET-TO-9	Q _A	Q _B	Q _C	Q _D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

H = high level, L = low level

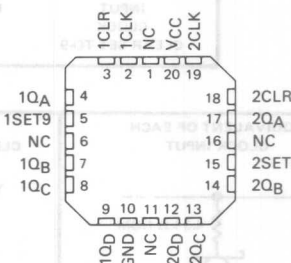
SN54490, SN54LS490 ... J OR W PACKAGE
SN74490 ... J OR N PACKAGE
SN74LS490 ... D, J OR N PACKAGE

(TOP VIEW)



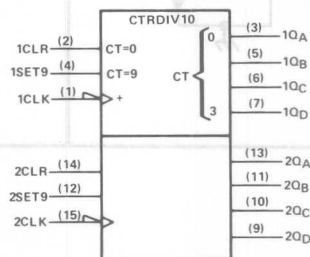
SN54LS490 ... FK PACKAGE
SN74LS490

(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.
NC - No internal connection

PRODUCTION DATA

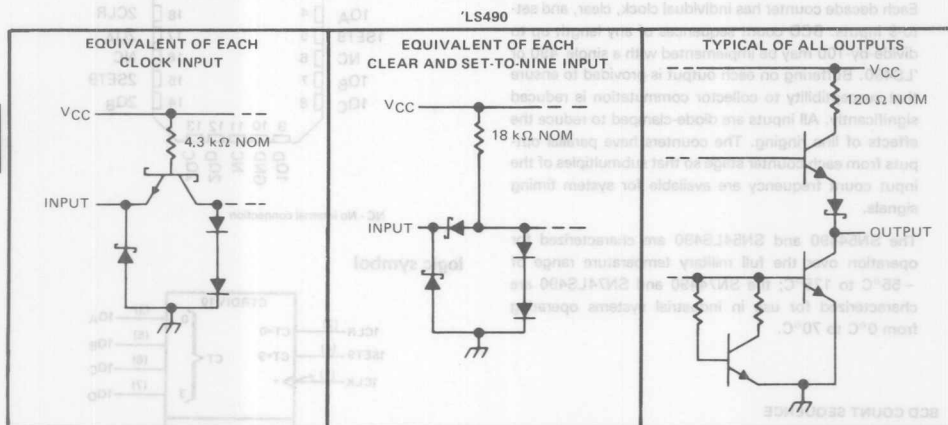
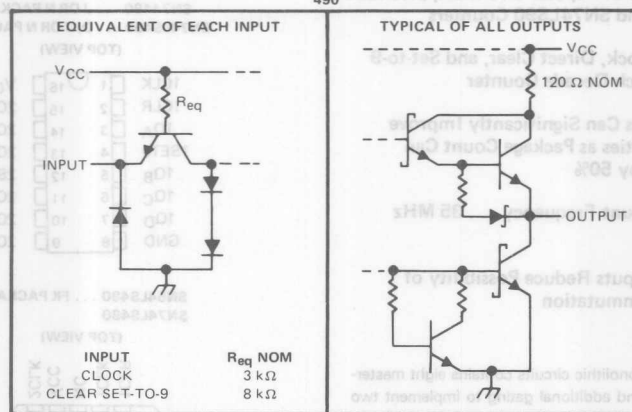
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TEXAS
INSTRUMENTS

TYPES SN54490, SN54LS490, SN74490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

1985-REVISED DECEMBER 1985

schematics of inputs and outputs



3 TTL DEVICES

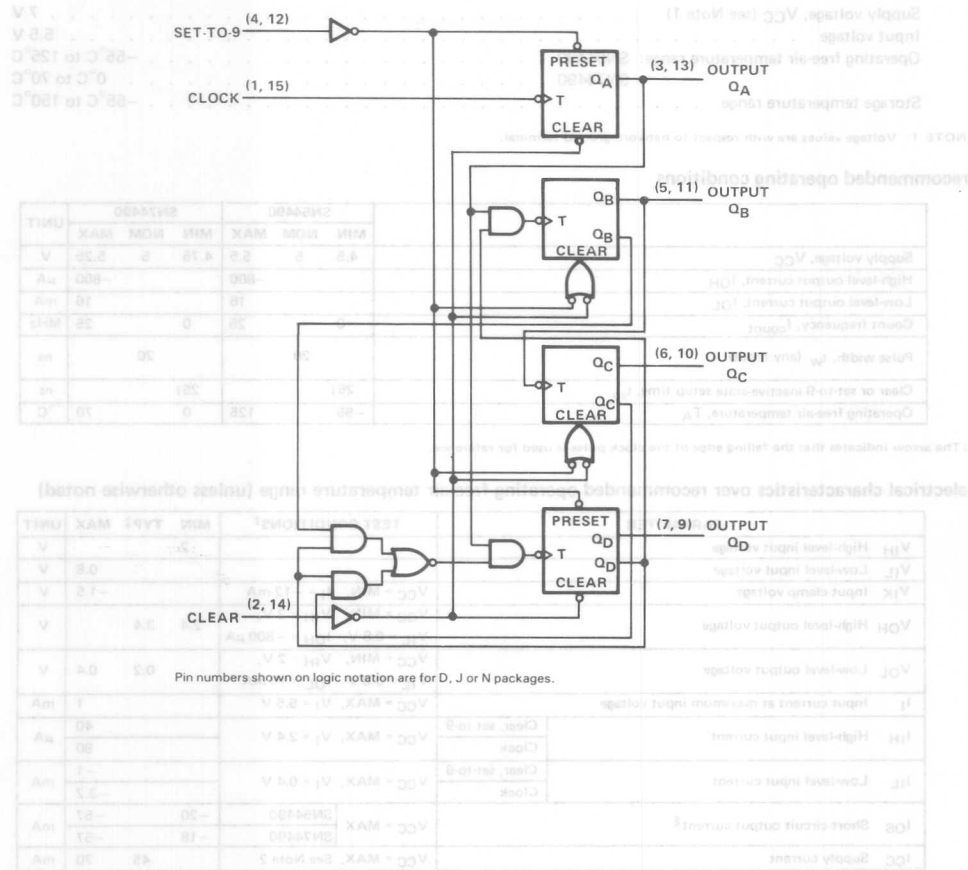
FUNCTION TABLE (EACH COUNTER)

INPUTS	OUTPUTS
CLEAR SET-TO-9	0 0 0 0 0 0
H L L L L L	0 0 0 0 0 0
L H L L L L	0 0 0 0 0 0
L L H L L L	0 0 0 0 0 0
L L L H L L	0 0 0 0 0 0
L L L L H L	0 0 0 0 0 0
L L L L L H	0 0 0 0 0 0
COUNT	0 1 2 3 4 5 6 7 8 9

H = high level, L = low level

TYPES SN54490, SN54LS490, SN74490, SN74LS490
DUAL 4-BIT DECADE COUNTERS

logic diagram (each counter)



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

TYPES SN54490, SN74490 DUAL 4-BIT DECADE COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54490	−55°C to 125°C
SN74490	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54490			SN74490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Count frequency, f_{count}	0		25	0		25	MHz
Pulse width, t_W (any input)		20			20		ns
Clear or set-to-9 inactive-state setup time, t_{SU}		25			25		ns
Operating free-air temperature, T_A	−55		125	0		70	°C

†The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \text{ μA}$		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	Clear, set-to-9	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
		Clock				80	
I_{IL}	Low-level input current	Clear, set-to-9	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			−1	mA
		Clock				−3.2	
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54490	−20		−57	mA
			SN74490	−18		−57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 2			45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

3

TTL DEVICES

TYPES SN54490, SN74490 DUAL 4-BIT DECADE COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max}	Clock	Q_A	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Figure 1 and Note 3	25	35		MHz
t_{PLH}	Clock	Q_A		12	20		ns
t_{PHL}		Q_A		13	20		ns
t_{PLH}	Clock	Q_B, Q_D		24	39		ns
t_{PHL}		Q_B, Q_D		26	39		ns
t_{PLH}	Clock	Q_C		32	54		ns
t_{PHL}		Q_C		36	54		ns
t_{PHL}	Clear	Any		24	39		ns
t_{PLH}	Set-to-9	Q_A, Q_D		24	39		ns
t_{PHL}		Q_B, Q_C		20	36		ns

[†] f_{\max} = maximum count frequency

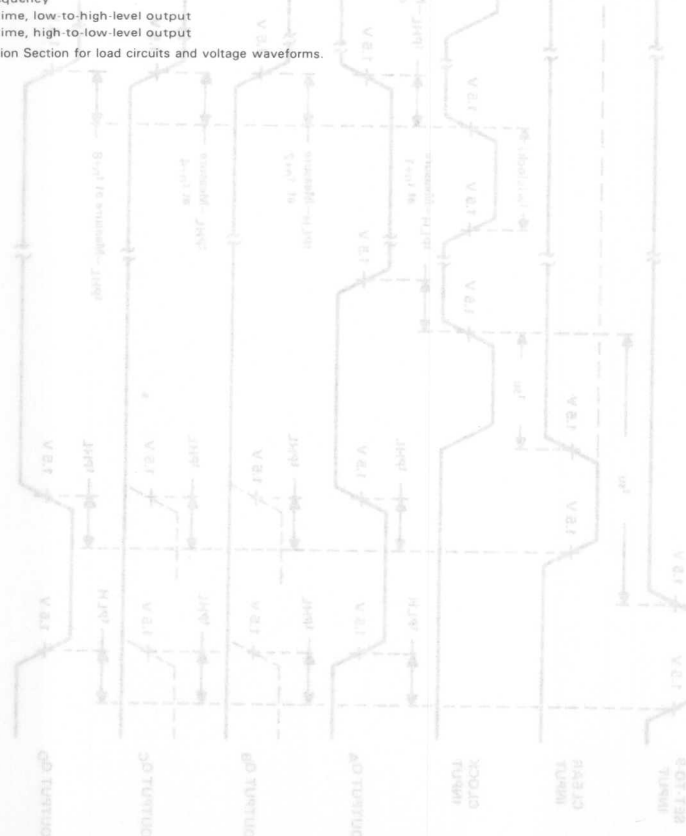
t_{PLH} = propagation delay time, low-to-high level output

t_{PHL} = propagation delay time, high-to-low level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

FIGURE 1

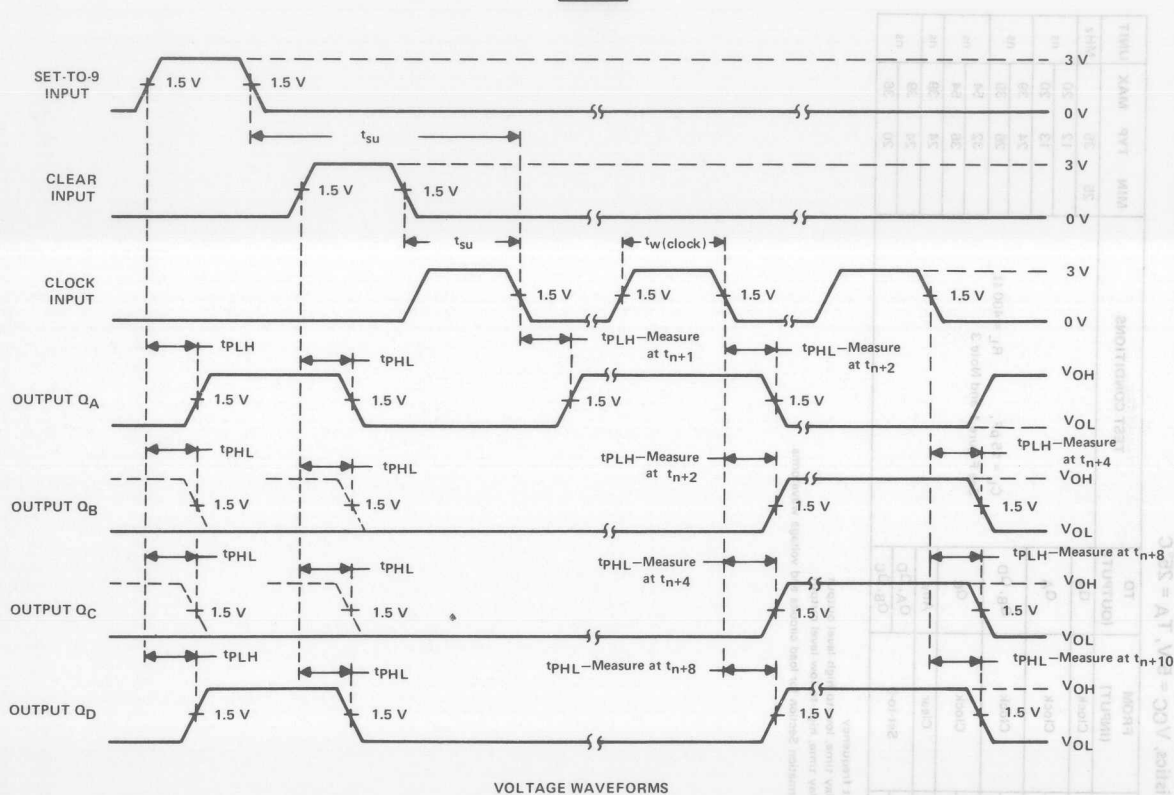
VOLTAGE WAVEFORMS



3

TTL DEVICES

TYPES SN54490, SN74490
DUAL 4-BIT DECADE COUNTERS



NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

FIGURE 1

TTL DEVICES

3

TYPES SN54LS490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Clear and set-to-9 input voltage	7 V
Clock input voltage	5.5 V
Operating free-air temperature range: SN54LS490	-55°C to 125°C
SN74LS490	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS490			SN74LS490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Count frequency, f_{count}	0		25	0		25	MHz
Pulse width, t_w (any input)	20			20			ns
Clear or set-to-9 inactive-state setup time, t_{su}	25			25			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS490			SN74LS490			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$							V
		$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
		$V_I = 5.5 \text{ V}$			0.2			0.2	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
					100			100	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
					-1.6			-1.6	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2		15	26		15	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

TYPES SN54LS490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Clock	Q _A	C _L = 15 pF, R _L = 2 kΩ See Figure 2 and Note 3	25	35		MHz
t _{PLH}	Clock	Q _A		12	20		ns
t _{PHL}				13	20		
t _{PLH}	Clock	Q _B , Q _D		24	39		ns
t _{PHL}				26	39		
t _{PLH}	Clock	Q _C		32	54		ns
t _{PHL}				36	54		
t _{PHL}	Clear	Any		24	39		ns
t _{PLH}	Set-to-9	Q _A , Q _D		24	39		ns
t _{PHL}				20	36		

[†] f_{\max} = maximum count frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

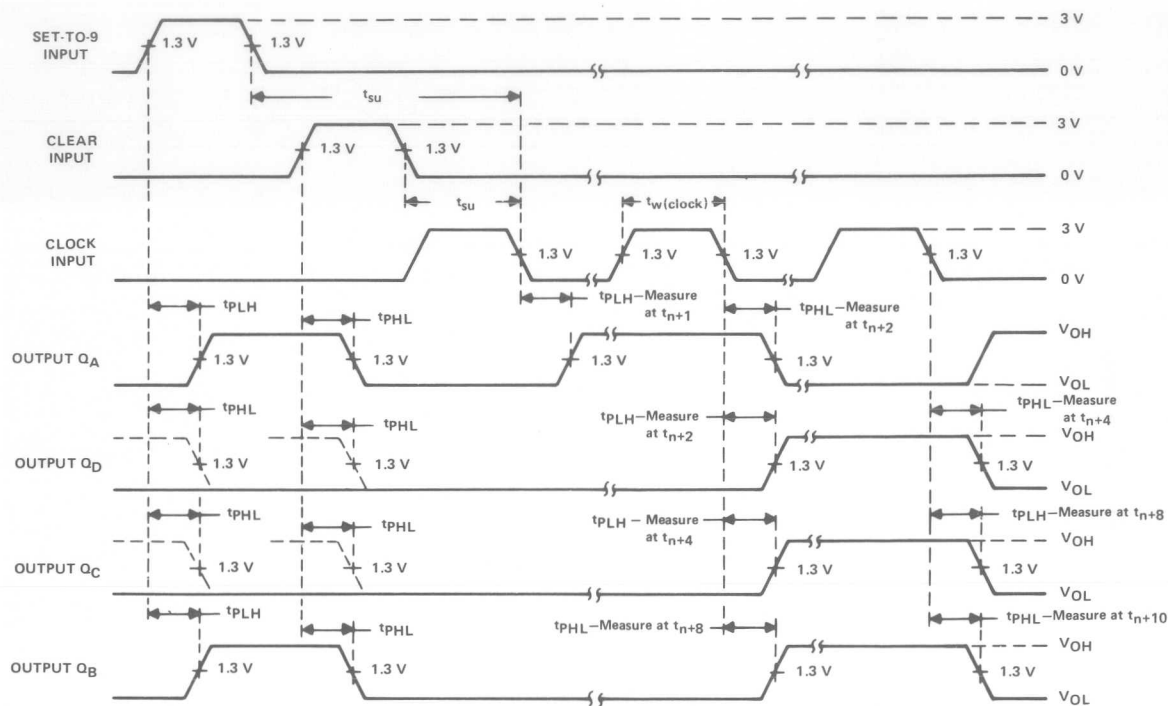
NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

PARAMETER	TEST CONDITIONS [†]	SN54LS490			SN74LS490		
		MIN	TYP	MAX	MIN	TYP	MAX
V_{IH} High-level input voltage		2			2		
V_{IL} Low-level input voltage		0.7			0.7		
V_{IC} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -15\text{ mA}$	-1.5			-1.5		
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $V_{IL} = V_{IL}(\text{max})$	3.5	3.4		3.3	3.4	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OL} = 8\text{ mA}$	0.55	0.4		0.55	0.4	
	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OL} = 8\text{ mA}$	0.55	0.4		0.55	0.4	
I_I Input current at maximum input voltage	Clear, $V_{CC} = \text{MAX}$, $V_I = 2.5\text{ V}$	0.1			0.1		
	Clock, $V_{CC} = \text{MAX}$, $V_I = 2.5\text{ V}$	0.3			0.3		
I_{IH} High-level input current	Clear, $V_{CC} = \text{MAX}$, $V_I = 2.5\text{ V}$	50			50		
	Clock, $V_{CC} = \text{MAX}$, $V_I = 2.5\text{ V}$	100			100		
I_{IL} Low-level input current	Clear, $V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$	-0.5			-0.5		
	Clock, $V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$	-1.5			-1.5		
I_{OZ} Short-circuit output current [‡]	$V_{CC} = \text{MAX}$	-50			-50		
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	15	25		15	25	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
 Not more than one output should be loaded at a time, and duration of the short-circuit should not exceed the second.
 NOTE 2: I_{CC} is measured with all outputs open, both clock inputs grounded through a $10\text{ k}\Omega$ resistor to 0.5 V , and all other inputs grounded.



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

FIGURE 2

TTL DEVICES



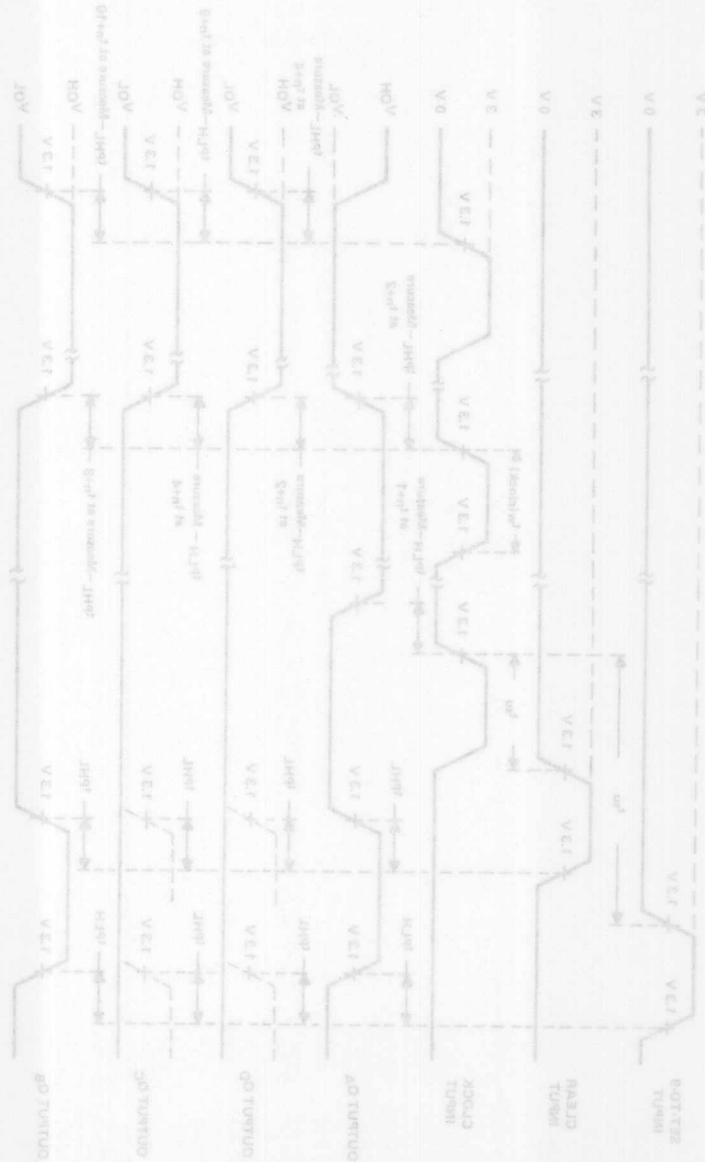


FIGURE 3

3 TTL DEVICES

TYPES SN54LS540, SN54LS541, SN74LS540, SN74LS541, OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2546, AUGUST 1979—REVISED APRIL 1985

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

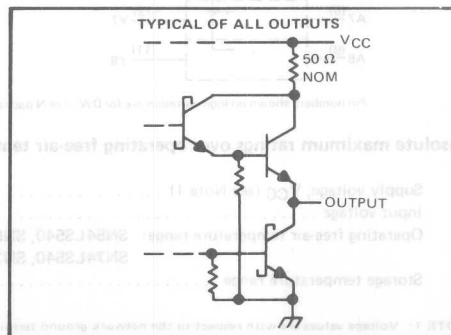
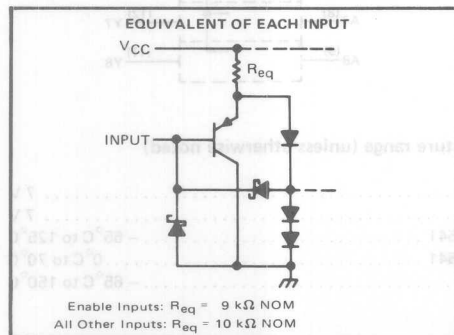
The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C .

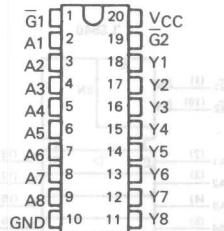
TYPE	RATED I_{OL} (SINK CURRENT)	RATED I_{OH} (SOURCE CURRENT)	TYPICAL POWER DISSIPATION (ENABLED)
			'LS540 'LS541
SN54LS'	12 mA	— 12 mA	92.5 mW 120 mW
SN74LS'	24 mA	— 15 mA	92.5 mW 120 mW

schematics of inputs and outputs



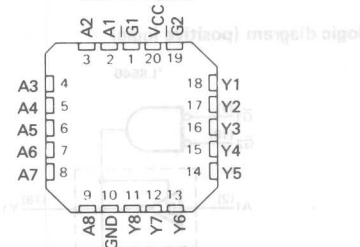
SN54LS540, SN54LS541 ... J PACKAGE
SN74LS540, SN74LS541 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS540, SN54LS541 ... FK PACKAGE
SN74LS540, SN74LS541

(TOP VIEW)



3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

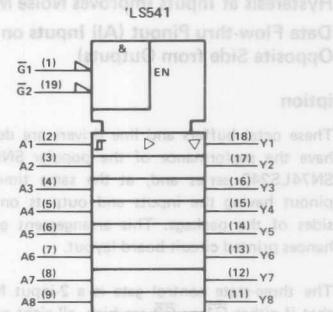
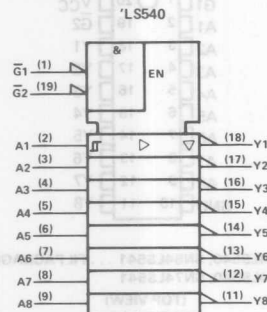
TEXAS
INSTRUMENTS

3-975

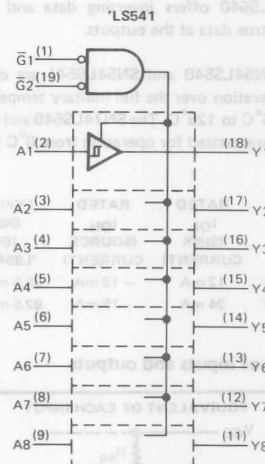
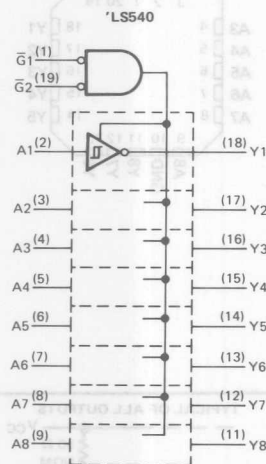
TYPES SN54LS540, SN54LS541, SN74LS540, SN74LS541

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbols



logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS540, SN54LS541	-55°C to 125°C
SN74LS540, SN74LS541	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

TYPES SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'		SN74LS'		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IH}	High-level input voltage			2			2	V
V _{IL}	Low-level input voltage					0.5		0.6
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA				−1.5		−1.5
	Hysteresis (V _{T+} − V _{T−})	V _{CC} = MIN		0.2	0.4		0.2	0.4
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = −3 mA		2.4	3.4		2.4	3.4
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.5 V, I _{OH} = MAX		2			2	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 12 mA		0.25	0.4		0.25	0.4
		I _{OL} = 24 mA					0.35	0.5
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _O = 2.7 V				20		20
I _{OZL}	Off-state output current, low-level voltage applied					−20		−20
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1		0.1
I _{IH}	High-level input current, any input	V _{CC} = MAX, V _I = 2.7 V				20		20
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V				−0.2		−0.2
I _{OS}	Short-circuit output current*	V _{CC} = MAX		−40		−225	−40	−225
I _{CC}	Supply current	Outputs high	V _{CC} = MAX, Outputs open	'LS540	13	25	13	25
				'LS541	18	32	18	32
		Outputs low		'LS540	24	45	24	45
				'LS541	30	52	30	52
		All outputs disabled		'LS540	30	52	30	52
				'LS541	32	55	32	55

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

* Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	'LS540			'LS541			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Note 2	9	15		9	15		ns
t_{PHL} Propagation delay time, high-to-low-level output		9	15		10	18		ns
t_{PZL} Output enable time to low level		25	38		25	38		ns
t_{PZH} Output enable time to high level		15	25		20	32		ns
t_{PLZ} Output disable time from low level	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$ See Note 2	10	18		10	18		ns
t_{PHZ} Output disable time from high level		15	25		18	29		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

recommended operating conditions

PARAMETER	SN54LS ²		SN74LS ²		UNIT	
	MIN	NOM	MAX	MIN		MAX
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5.25	V
High-level output current, I_{OH}	—	—	—	—	—18	mA
Low-level output current, I_{OL}	—	—	—	—	34	mA
Operating free-air temperature, T_A	—55	—	125	0	70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹		SN54LS ²		SN74LS ²		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH} High-level input voltage			2		2		V
V_{IL} Low-level input voltage			0.8		0.8		V
V_{IK} Input clamp voltage			—1.5		—1.5		V
Threshold voltage, $V_T = (V_{IH} + V_{IL})/2$			0.3	0.4	0.3	0.4	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OH} = -3\text{ mA}$		2.4	3.4	2.4	3.4	V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OH} = \text{MAX}$		2		2		V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OH} = \text{MAX}$		0.25	0.4	0.25	0.4	V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{OH} = \text{MAX}$		0.25	0.4	0.25	0.4	V
I_{OZH} On-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2\text{ V}$, $V_{OL} = 0.4\text{ V}$		—30		—30		mA
	$V_{CC} = \text{MAX}$, $V_{IH} = 2\text{ V}$, $V_{OL} = 0.4\text{ V}$		—30		—30		mA
I_{OL} On-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2\text{ V}$, $V_{OL} = 0.4\text{ V}$		30		30		mA
	$V_{CC} = \text{MAX}$, $V_{IH} = 2\text{ V}$, $V_{OL} = 0.4\text{ V}$		30		30		mA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 2\text{ V}$		0.1		0.1		mA
I_{IH} High-level input current, any input	$V_{CC} = \text{MAX}$, $V_I = 2\text{ V}$		—0.5		—0.5		mA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$		—35		—35		mA
I_{CC} Supply current	Outputs high		12	25	13	28	mA
	Outputs low		18	35	18	35	mA
	Outputs open		34	65	34	65	mA
	All outputs disabled		30	65	30	65	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
² All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
³ For more than one output should be turned at a time, and duration of the switching should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		SN54LS ²		SN74LS ²		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} Propagation delay time, low-to-high output			9	18	9	18	ns
t_{PHL} Propagation delay time, high-to-low output			9	18	10	18	ns
t_{ZL} Output enable time to low level			25	35	25	35	ns
t_{ZH} Output enable time to high level			15	25	15	25	ns
t_{FL} Output disable time from low level			10	15	10	15	ns
t_{FL} Output disable time from high level			15	25	15	25	ns

NOTE 2: See General Information Section for load circuit and voltage waveforms.

TYPES SN54LS589, SN74LS589

8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

REVISED DECEMBER 1983

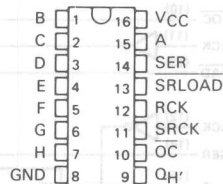
- 8-Bit Parallel Storage Register Inputs
- Shift Register has Direct Overriding Load and Power-Up Clear
- Guaranteed Shift Frequency . . . DC to 20 MHz

description

The 'LS589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register with 3-state outputs. Both the storage register and shift register have positive-edge triggered clocks. The shift register has a direct load (from storage) input.

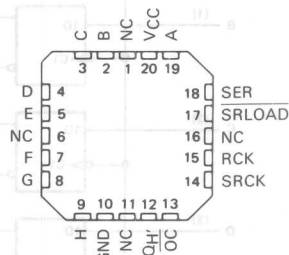
SN54LS589 . . . J PACKAGE
SN74LS589 . . . J OR N PACKAGE

(TOP VIEW)



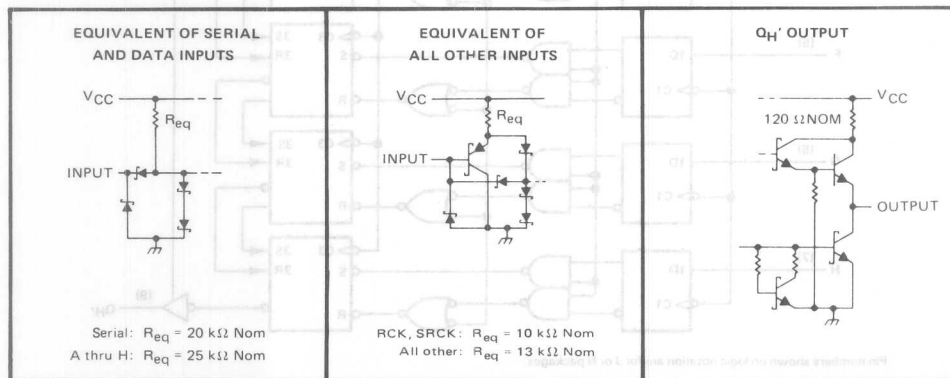
SN54LS589 . . . FK PACKAGE
SN74LS589

(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



PRODUCTION DATA

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TEXAS
INSTRUMENTS

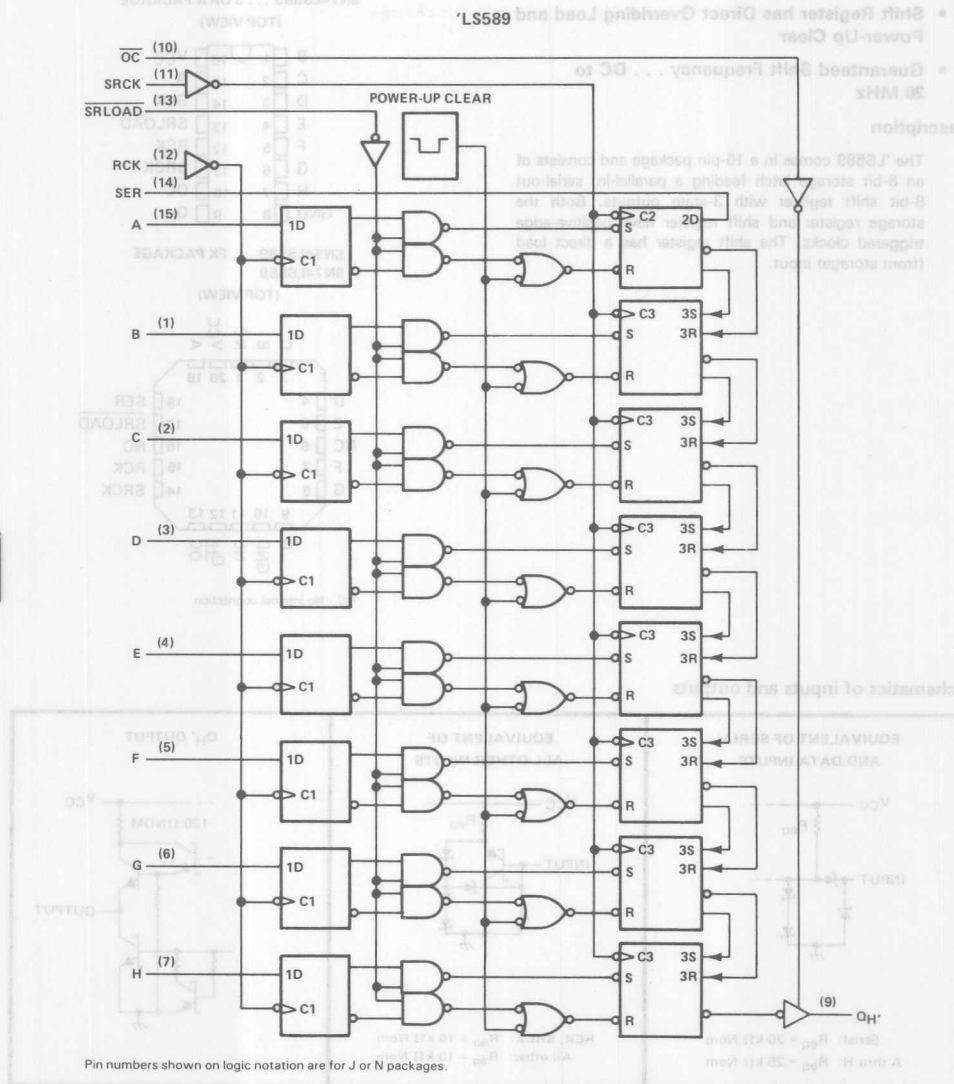
3-979

3

TTL DEVICES

TYPES SN54LS589, SN74LS589 8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

logic diagram

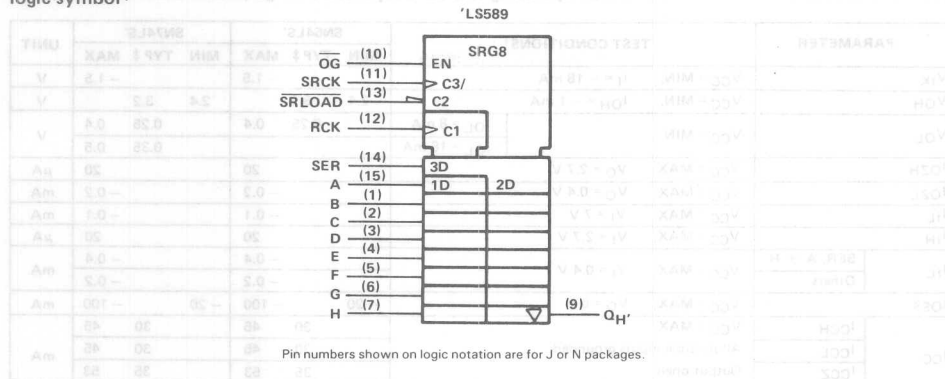


3

TTL DEVICES

TYPES SN54LS589, SN74LS589 8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

logic symbol†



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS589	–55°C to 125°C
SN74LS589	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
I _{OH}	High-level output current					− 1			− 1	mA
I _{OL}	Low-level output current					8			16	mA
f _{SRCK}	Shift clock frequency			0		20	0		20	MHz
t _w	Pulse duration	SRCK	High	15			15			ns
			Low	35			35			
		RCK		20			20			
		SRLOAD		40			40			
t _{su}	Setup time	Data before RCK †		20			20			ns
		SER before SRCK †		20			20			
		SRLOAD inactive before SRCK †		30			30			
		RCK † before SRLOAD † (see Note 2)		40			40			
t _h	Hold time	Data after RCK †		0			0			ns
		SER after SRCK †		0			0			
T _A	Operating free-air temperature			− 55		125	0		70	°C

NOTE 2: The RCK ↑ to SRLOAD setup time ensures the data saved by RCK ↑ will also be loaded into the counter.

TYPES SN54LS589, SN74LS589 8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, I _{OH} = -1 mA	2.4	3.2		2.4	3.2		V
V _{OL}	V _{CC} = MIN, I _{OL} = 8 mA		0.25	0.4		0.25	0.4	V
						0.35	0.5	
I _{OZH}	V _{CC} = MAX, V _O = 2.7 V			20			20	µA
I _{OZL}	V _{CC} = MAX, V _O = 0.4 V			-0.2			-0.2	mA
I _{IL}	V _{CC} = MAX, V _I = 7 V			-0.1			-0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	µA
I _{IL}	SER, A → H			-0.4			-0.4	mA
	Others			-0.2			-0.2	
I _{OS} §	V _{CC} = MAX, V _O = 0 V	-20		-100	-20		-100	mA
I _{CC}	I _{CCH}		30	45		30	45	mA
	I _{CCL}		30	45		30	45	
	I _{CCZ}		35	53		35	53	

† For conditions shown as MIN or MAX use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

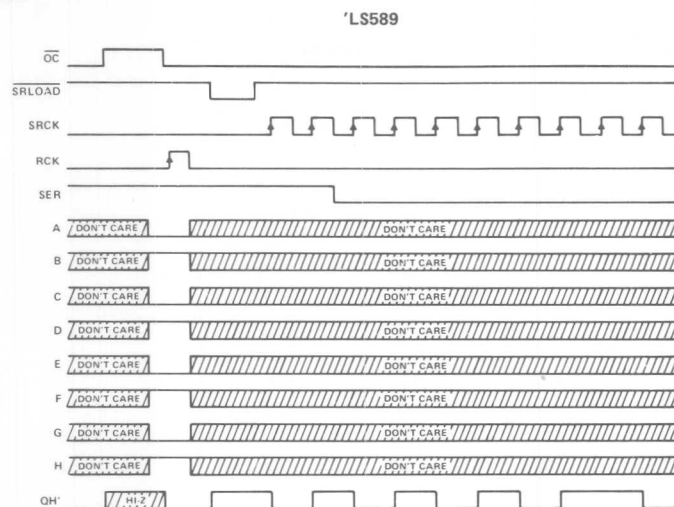
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS589			UNIT
				MIN	TYP	MAX	
f _{max}	SRCK			20	35		MHz
t _{PLH}	SRCK ↑	Q _H '	R _L = 1 kΩ, C _L = 30 pF		15	23	ns
t _{PHL}					20	30	
t _{PLH}	SRLOAD ↓	Q _H '			38	57	ns
t _{PHL}					29	44	
t _{PLH}	RCK ↑	Q _H '	R _L = 1 kΩ, C _L = 30 pF, SRLOAD = L		41	60	ns
t _{PHL}					32	48	
t _{PZH}					10	15	ns
t _{PZL}					18	27	
t _{PHZ}	OC	Q _H '	R _L = 667 Ω, C _L = 5 pF		20	30	ns
t _{PLZ}					20	30	

NOTE 2: See General Information Section for load circuits and voltage waveforms.

PARAMETER	TEST CONDITIONS	UNIT
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns
t _{SR}	SRCK ↑, SRLOAD ↓, R _L = 1 kΩ, C _L = 30 pF	ns

TYPES SN54LS589, SN74LS589
8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

timing diagram



3

TTL DEVICES



TYPES SN54LS590, SN54LS591, SN74LS590, SN74LS591 8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

D2632, JANUARY 1981 — REVISED JUNE 1983

- 8-Bit Counter with Register
- Parallel Register Outputs
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency: DC to 20 MHz

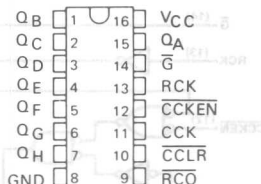
description

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{\text{CLR}}$ and a count enable input $\overline{\text{CKEN}}$. For cascading, a ripple carry output RCO is provided. Expansion is easily accomplished for two stages by connecting RCO of the first stage to $\overline{\text{CKEN}}$ of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to CCK of the following stage.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

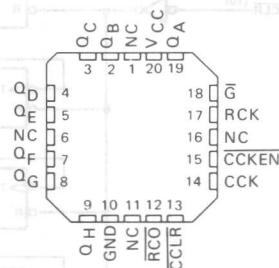
SN54LS590, SN54LS591 ... J OR W PACKAGE
SN74LS590, SN74LS591 ... J OR N PACKAGE

(TOP VIEW)



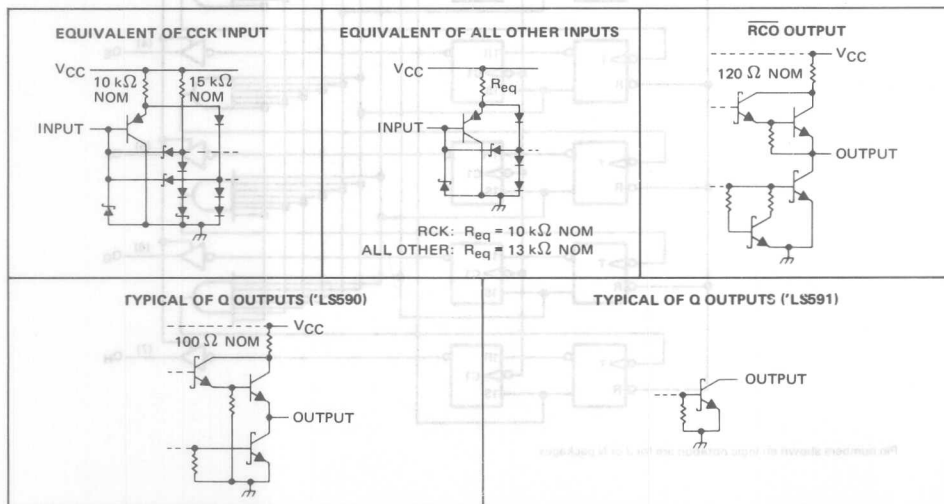
SN54LS590, SN54LS591 ... FK PACKAGE
SN74LS590, SN74LS591

(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



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TEXAS
INSTRUMENTS

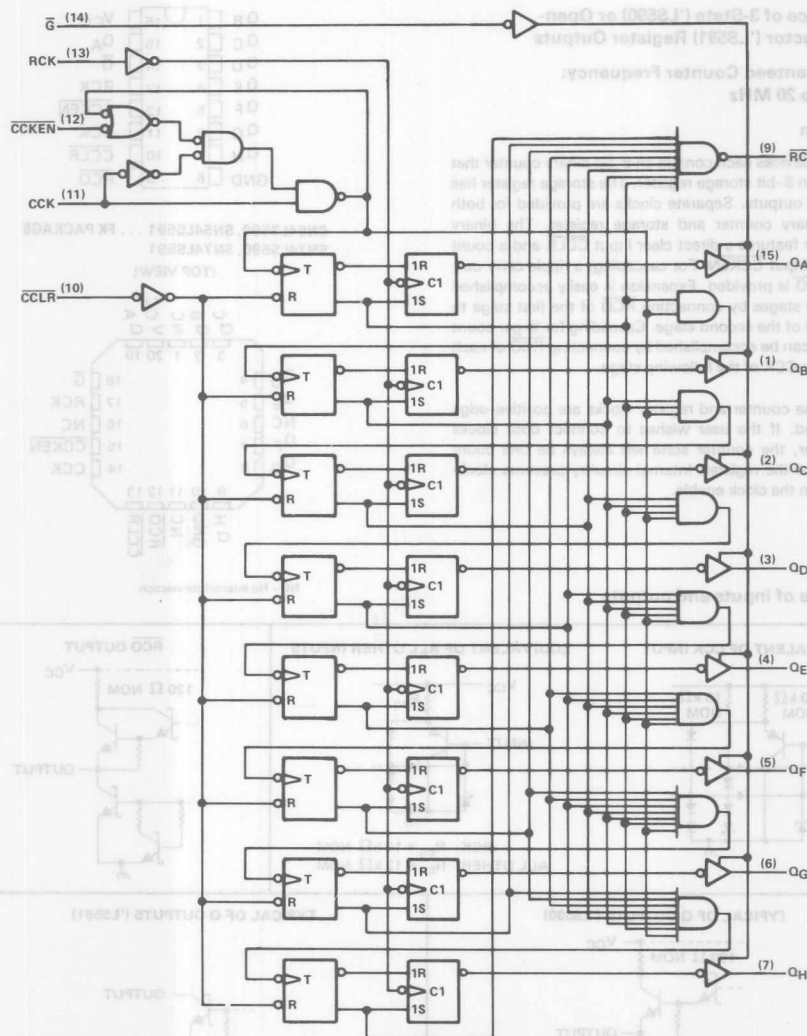
3-985

3

TTL DEVICES

TYPES SN54LS590, SN54LS591, SN74LS590, SN74LS591 8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

logic diagram (positive logic)



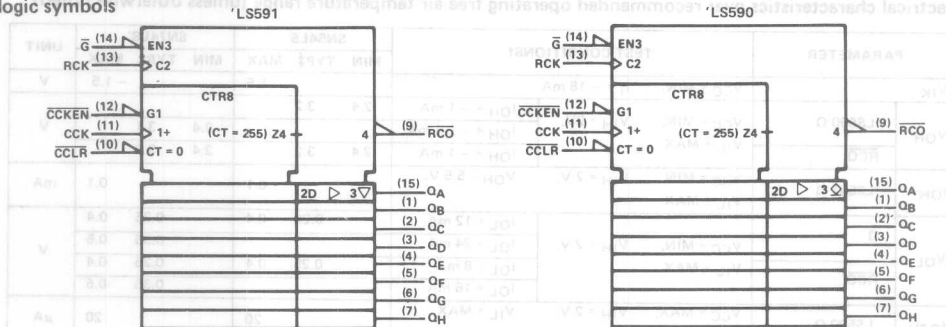
Pin numbers shown on logic notation are for J or N packages.

3

TTL DEVICES

TYPES SN54LS590, SN54LS591, SN74LS590, SN74LS591 8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

logic symbols



Pin numbers shown on logic notation are for J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591	-55°C to 125°C
SN74LS590, SN74LS591	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS*			SN74LS*			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{OH}	High-level output voltage	Q, 'LS591 only			5.5			5.5	V
I _{OH}	High-level output current	RCO			− 1			− 1	mA
		Q, 'LS590 only			− 1			− 2.6	
I _{OL}	Low-level output current	RCO			8			16	mA
		Q			12			24	
f _{CCK}	Counter clock frequency		0		20	0		20	MHz
f _{RCK}	Register clock frequency		0		25	0		25	MHz
t _w (CCK)	Duration of counter clock pulse		25			25			ns
t _w (CCLR)	Duration of counter clear pulse		20			20			ns
t _w (RCK)	Duration of register clock pulse		20			20			ns
t _{su}	Setup time	CCKEN low before CCK ↑	20			20			ns
		CCLR inactive before CCK ↑	20			20			
		CCK before RCK ↑ (see Note 2)	40			40			
t _h	Hold time	CCKEN low after CCK ↑	0			0			ns
T _A	Operating free-air temperature		− 55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

TYPES SN54LS590, SN54LS591, SN74LS590, SN74LS591 8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	'LS590 Q	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -1 mA	2.4	3.2		2.4	3.1		V
	RCO	V _{IL} = MAX, I _{OH} = -2.6 mA							
I _{OH}	'LS591 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V, V _{IL} = MAX			0.1			0.1	mA
V _{OL}	Q	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 12 mA	0.25	0.4		0.25	0.4		V
		I _{OL} = 24 mA				0.35	0.5		
	RCO	V _{IL} = MAX, I _{OL} = 8 mA	0.25	0.4		0.25	0.4		
		I _{OL} = 16 mA				0.35	0.5		
I _{OZH}	'LS590 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V, V _{IL} = MAX			20			20	μA
I _{OZL}	'LS590 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V, V _{IL} = MAX			-20			-20	μA
I _I		V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	CCK	V _{CC} = MAX, V _I = 0.4 V			-0.8			-0.8	mA
	All others				-0.2			-0.2	
I _{OS} §	'LS590 Q	V _{CC} = MAX, V _O = 0 V	-30	-130		-30	-130		mA
	RCO		-20	-100		-20	-100		
I _{CC}	'LS590	I _{CCH}	33	55		33	55		mA
		I _{CCL}	44	65		44	65		
		I _{CCZ}	46	65		46	65		
	'LS591	I _{CCH}	35	55		35	55		
		I _{CCL}	42	65		42	65		
		I _{CCZ}							

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS590			'LS591			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{max}	CCK	RCO	R _L = 1 kΩ, C _L = 30 pF	20	35		20	35		MHz
t _{PLH}	CCK	RCO		14	22		16	24		ns
t _{PHL}	CCK	RCO		20	30		25	38		ns
t _{PLH}	CCK	RCO		30	45		32	48		ns
t _{PLH}	RCK	Q	R _L = 667 Ω, C _L = 45 pF	12	18		25	38		ns
t _{PHL}	RCK	Q		22	33		28	42		ns
t _{PZH}	Q	Q		25	38					ns
t _{PZL}	Q	Q		30	45					ns
t _{PHZ}	Q	Q	R _L = 667 Ω, C _L = 5 pF	20	30					ns
t _{PLZ}	Q	Q		25	38					ns
t _{PLH}	Q	Q	R _L = 667 Ω, C _L = 45 pF				34	50		ns
t _{PHL}	Q	Q					32	48		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

02633, JANUARY 1981 — REVISED DECEMBER 1983

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Guaranteed Counter Frequency: DC to 20 MHz

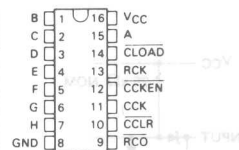
description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going \overline{RCO} pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to \overline{CCK} of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (\overline{CCKEN} , \overline{CCKEN}) inputs. A register clock enable (\overline{RCKEN}) is also provided.

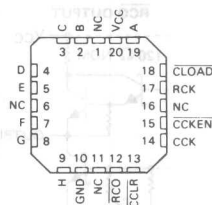
SN54LS592 ... J OR W PACKAGE
SN74LS592 ... J OR N PACKAGE

(TOP VIEW)



SN54LS592 ... FK PACKAGE
SN74LS592

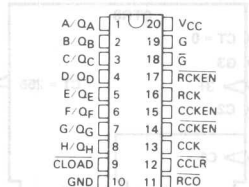
(TOP VIEW)



NC — No internal connection

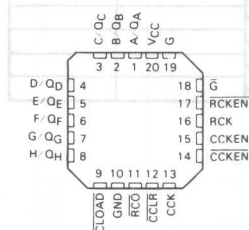
SN54LS593 ... J PACKAGE
SN74LS593 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS593 ... FK PACKAGE
SN74LS593

(TOP VIEW)



OUTPUT ENABLE CONTROL ('593 ONLY)

G	\overline{G}	A/Q _A thru H/Q _H
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

COUNTER CLOCK ENABLE CONTROL

CCKEN	\overline{CCKEN}	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

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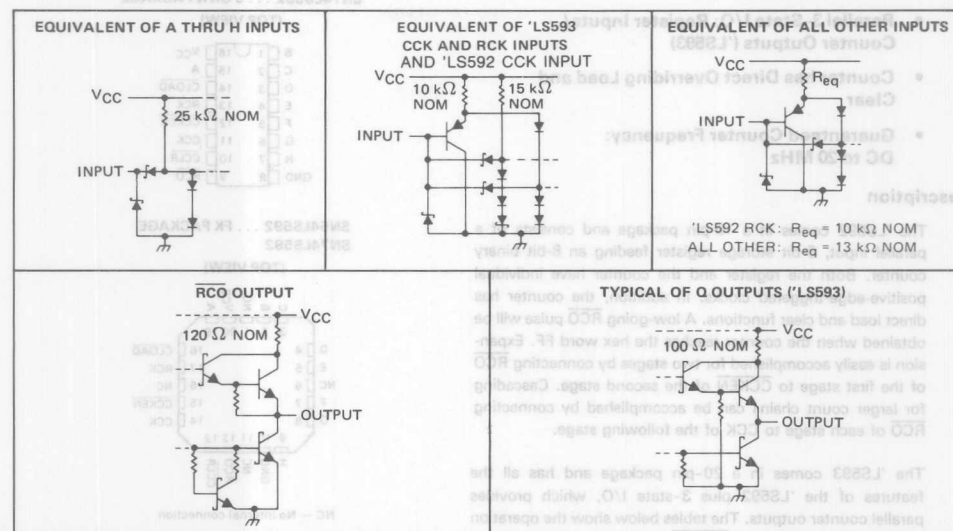
TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

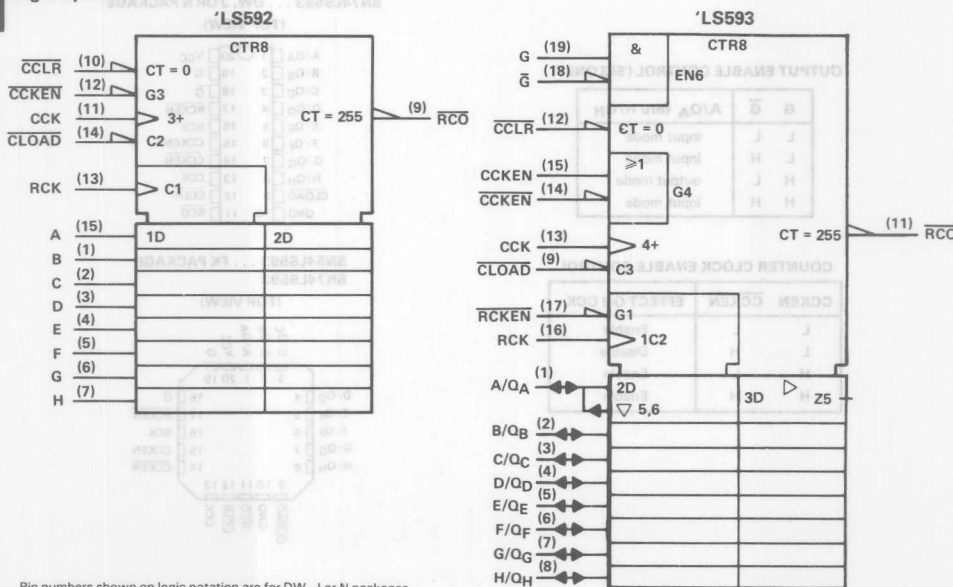
schematics of inputs and outputs



3

logic symbols

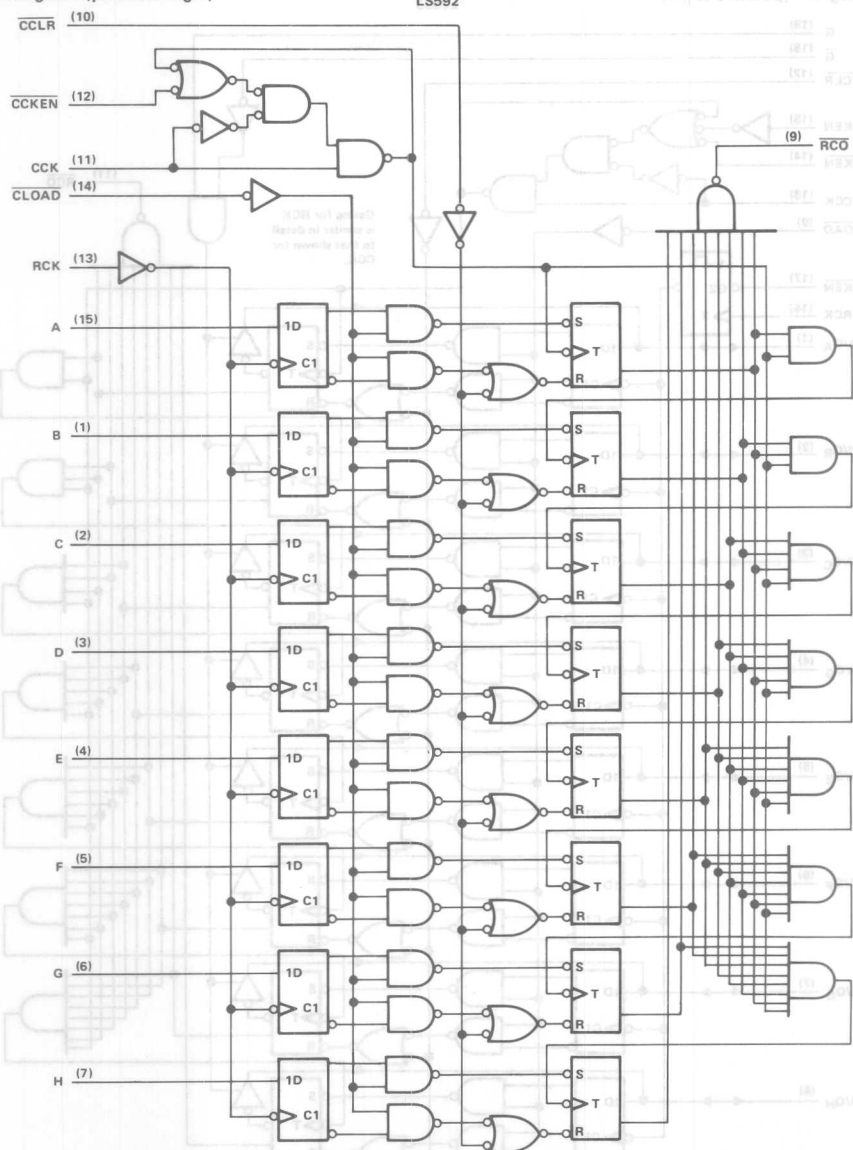
TTL DEVICES



Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN54LS592, SN74LS592
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)



Pin numbers shown on logic notation are for J or N packages.

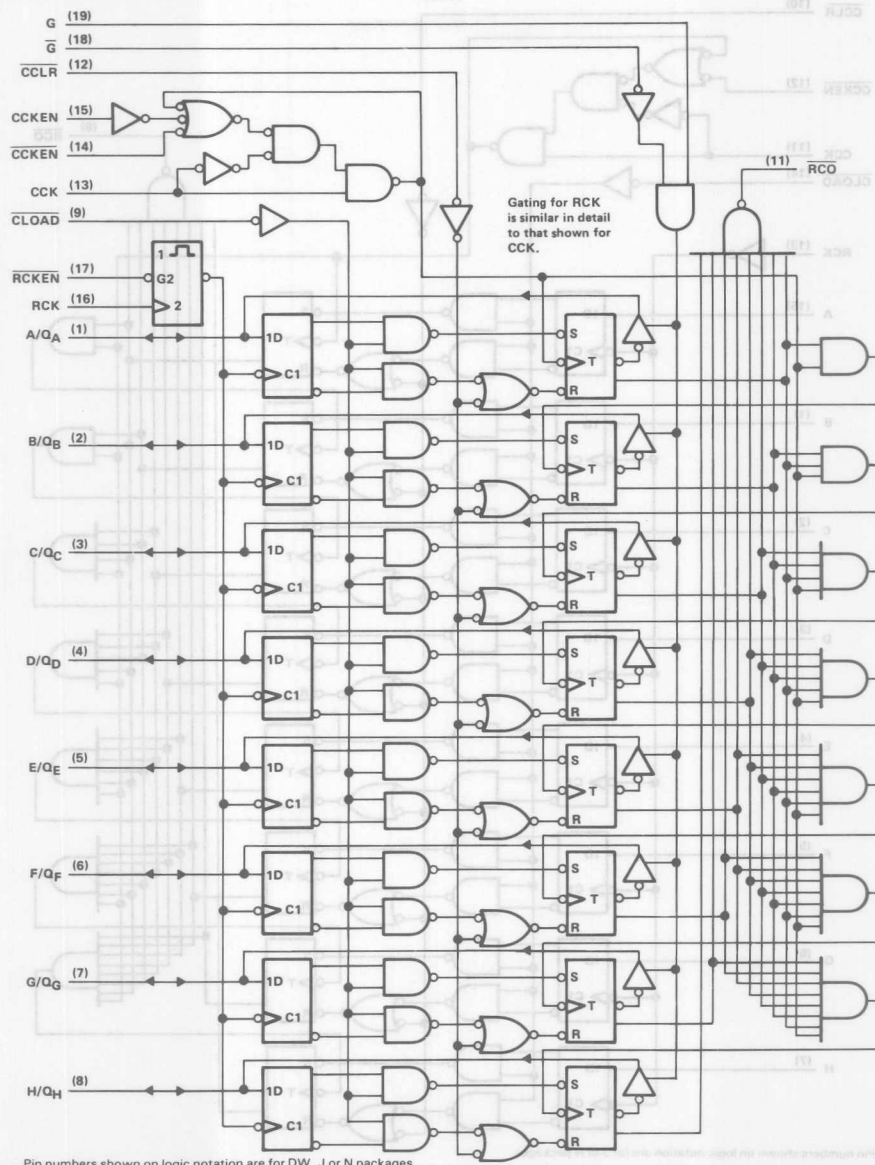
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TTL DEVICES

TYPES SN54LS593, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

'LS593

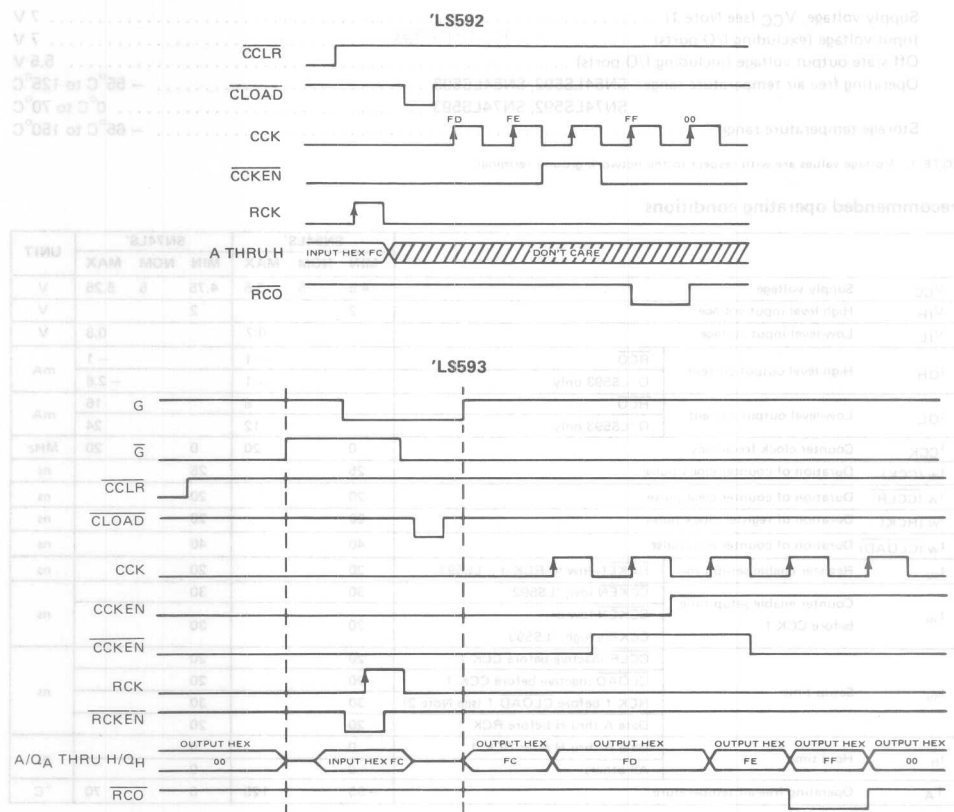


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TTL DEVICES

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

typical operating sequences



3

TTL DEVICES

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593	-55°C to 125°C
SN74LS592, SN74LS593	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	RCO			-1			-1	mA
		Q 'LS593 only			-1			-2.6	
I_{OL}	Low-level output current	RCO			8			16	mA
		Q 'LS593 only			12			24	
f_{CCK}	Counter clock frequency		0		20	0		20	MHz
t_w (CCK)	Duration of counter clock pulse		25			25			ns
t_w (CCLR)	Duration of counter clear pulse		20			20			ns
t_w (RCK)	Duration of register clock pulse		20			20			ns
t_w (CLOAD)	Duration of counter load pulse		40			40			ns
t_{su}	Register enable setup time	RCKEN low to RCK ↑, 'LS593	20			20			ns
t_{su}	Counter enable setup time before CCK ↑	CCKEN low, 'LS592	30			30			ns
		CCKEN low or CCKEN high, 'LS593	30			30			
t_{su}	Setup time	CCLR inactive before CCK ↑	20			20			ns
		CLOAD inactive before CCK ↑	20			20			
		RCK ↑ before CLOAD ↑ (see Note 2)	30			30			
		Data A thru H before RCK ↑	20			20			
t_h	Hold time	Data A thru H after RCK ↑	0			0			ns
		All others	0			0			
T_A	Operating free-air temperature		-55		125	0		70	°C

NOTE 2: This time insures the data saved by RCK ↑ will also be loaded into the counter.

3
TTL DEVICES

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	'LS593 Q	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	2.4	3.2		2.4	3.1		V
	\overline{RCO}	$V_{IL} = \text{MAX}, I_{OH} = -2.6 \text{ mA}$							
V_{OL}	'LS593 Q	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
	\overline{RCO}	$V_{IL} = \text{MAX}, I_{OL} = 24 \text{ mA}$				0.35	0.5		
		$I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4		
		$I_{OL} = 16 \text{ mA}$				0.35	0.5		
I_{OZH}	'LS593 Q	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	'LS593 Q	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_O = 0.4 \text{ V}$			-0.4			-0.4	mA
I_I	'LS593 Q	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1			0.1	mA
	Others	$V_I = 7 \text{ V}$			0.1			0.1	
I_{IH}		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	'LS593/593 CCK, RCK	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8			-0.8	mA
	A Thru H				-0.4			-0.4	
	Others				-0.2			-0.2	
$I_{OS}§$	'LS593 Q	$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$	-30	-130	-30	-130			mA
	\overline{RCO}		-20	-100	-20	-100			
I_{CC}	'LS592	$V_{CC} = \text{MAX},$ All possible inputs grounded, All outputs open			40	60		40	60
	$\overline{I_{CCL}}$				40	60		40	60
	'LS593	$\overline{I_{CCH}}$			47	70		47	70
	$\overline{I_{CCL}}$				53	80		53	80
	$\overline{I_{CCZ}}$				57	85		57	85

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

3

TTL DEVICES

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS592			'LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	CCK ↑	RCO	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	20	35		20	35		MHz
t_{PLH}	CCK ↑	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$					14	21	ns
t_{PHL}	CCK ↑	Q						26	39	ns
t_{PLH}	CLOAD ↓	Q						34	51	ns
t_{PHL}	CLOAD ↓	Q						28	42	ns
t_{PHL}	CCLR ↓	Q						25	38	ns
t_{PZH}	G ↑	Q						31	47	ns
t_{PZL}	G ↑	Q						27	40	ns
t_{PZH}	\overline{G} ↓	Q						29	45	ns
t_{PZL}	\overline{G} ↓	Q						31	47	ns
t_{PHZ}	G ↓	Q						33	50	ns
t_{PLZ}	G ↓	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$					35	52	ns
t_{PHZ}	\overline{G} ↑	Q						26	39	ns
t_{PLZ}	\overline{G} ↑	Q						28	42	ns
t_{PLH}	CCK ↑	RCO	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	15	23		14	21		ns
t_{PHL}	CCK ↑	RCO		20	30		20	30		ns
t_{PLH}	CLOAD ↓	RCO		31	47		31	47		ns
t_{PHL}	CLOAD ↓	RCO		27	41		27	41		ns
t_{PLH}	CCLR ↓	RCO	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	30	45		30	45		ns
t_{PLH}	RCK ↑	RCO		35	53		42	63		ns
t_{PHL}	RCK ↑	RCO		30	45		33	50		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

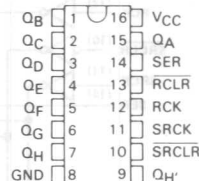
TYPES SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

D2747, JUNE 1983 — REVISED DECEMBER 1983

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of Output Configurations:
'LS594 ... Buffered
'LS599 ... Open-Collector
- Guaranteed Shift Frequency:
DC to 20 MHz
- Independent Direct-Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers

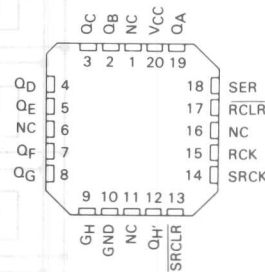
SN54LS594, SN54LS599 ... J OR W PACKAGE
SN74LS594, SN74LS599 ... J OR N PACKAGE

(TOP VIEW)



SN54LS594, SN54LS599 ... FK PACKAGE
SN74LS594, SN74LS599

(TOP VIEW)



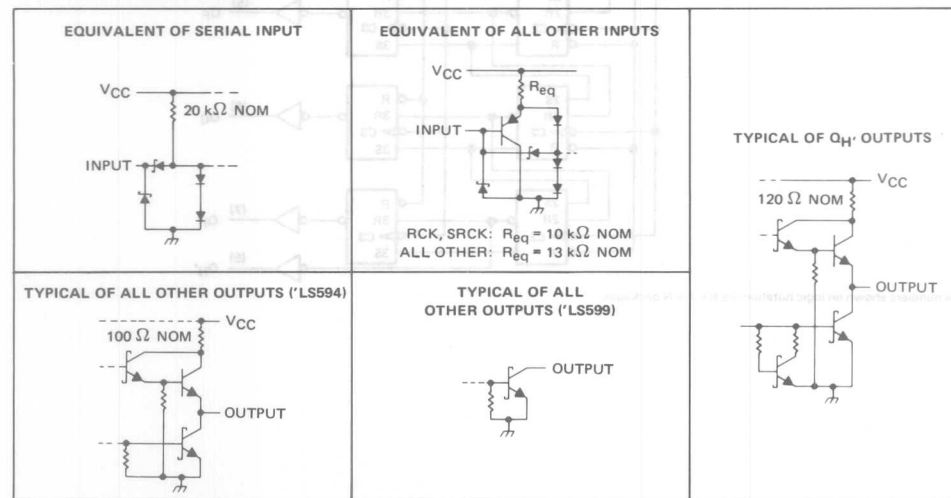
NC — No internal connection

description

These devices each contain an 8-bit D-type storage register. The storage register has buffered ('LS594) or open-collector ('LS599) outputs. Separate clocks and direct-overriding clears are provided on both the shift and storage registers. A shift output (Q_H') is provided for cascading purposes.

Both the shift register and the storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one clock pulse ahead of the storage register.

schematics of inputs and outputs



PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

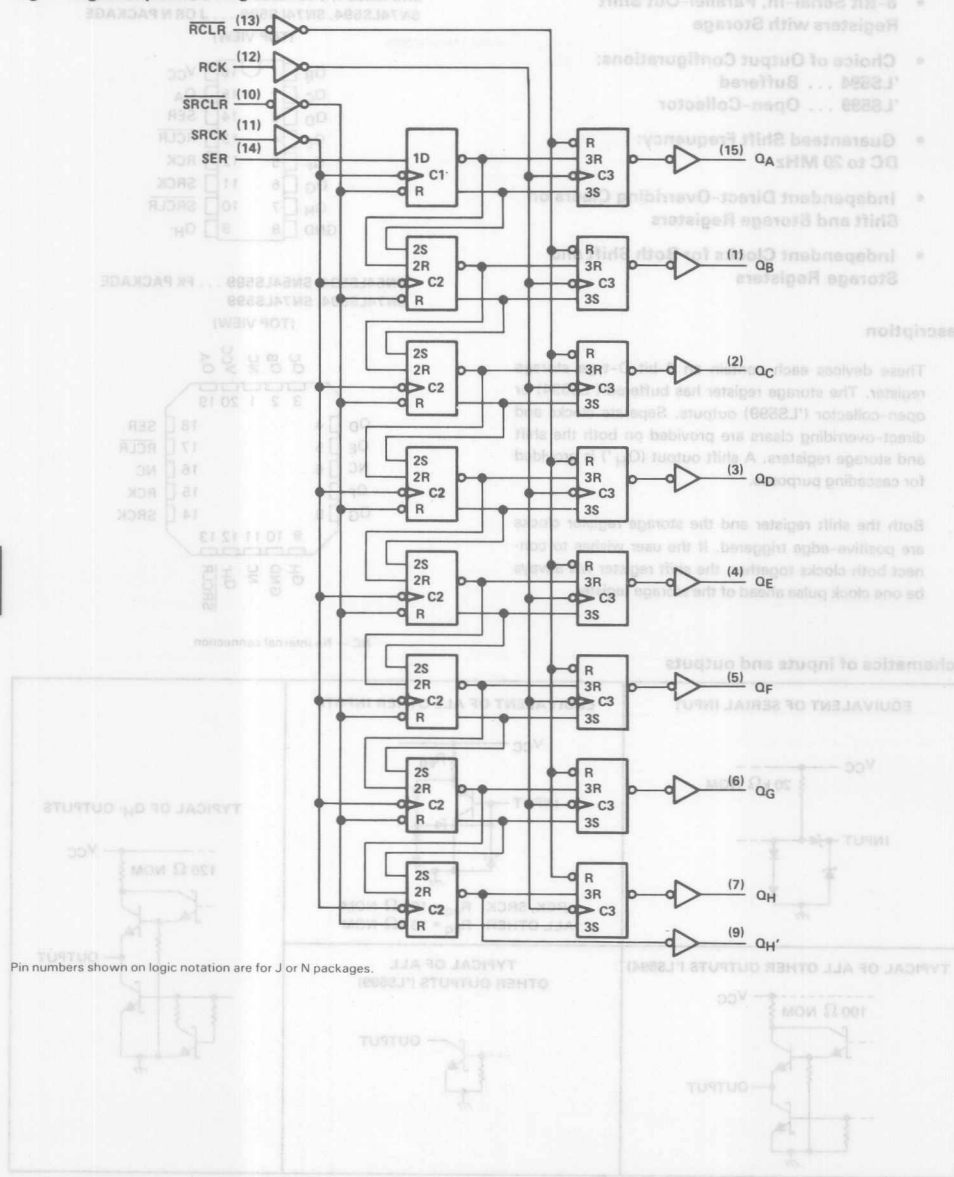
3-997

3

TTL DEVICES

TYPES SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

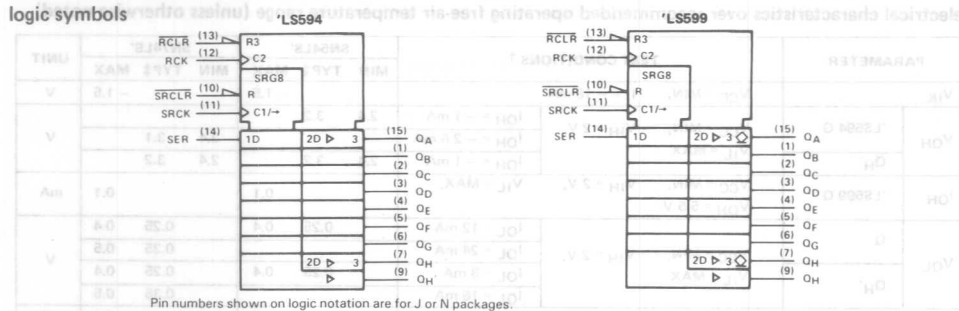
logic diagram (positive logic)



3 TTL DEVICES

TYPES SN54LS594, SN54LS599, SN74LS594, SN74LS599 8-BIT, SHIFT REGISTERS WITH OUTPUT LATCHES

logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS594, SN54LS599	– 55°C to 125°C
SN74LS594, SN74LS599	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS ¹			SN74LS ¹			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current	Q_A thru Q_H , 'LS599 only		– 1	Q_A thru Q_H , 'LS594 only		– 2.6	mA
		Q_H			Q_H			
I_{OL}	Low-level output current	Q_A thru Q_H , 'LS594 only		8	Q_A thru Q_H , 'LS599 only		16	mA
		Q_H		12	Q_H		24	
f_{SRCK}	Shift clock frequency	0		20	0		20	MHz
f_{RCK}	Register clock frequency	0		25	0		25	MHz
$t_w(SRCK)$	Duration of shift clock pulse	25			25			ns
$t_w(RCK)$	Duration of register clock pulse	20			20			ns
$t_w(SRCLR)$	Duration of shift clear pulse, low level	20			20			ns
$t_w(RCLR)$	Duration of register clear pulse, low level	35			35			ns
t_{su}	Setup time	SRCLR inactive before SRCK↑		20	SRCLR inactive before SRCK↑		20	ns
		SER before SRCK↑		20	SER before SRCK↑		20	
		SRCK↑ before RCK↑ (see Note 2)		40	SRCK↑ before RCK↑ (see Note 2)		40	
		SRCLR low before RCK↑		40	SRCLR low before RCK↑		40	
		RCLR high before RCK↑		20	RCLR high before RCK↑		20	
t_h	Hold time	SER after SRCK↑		0	SER after SRCK↑		0	ns
T_A	Operating free-air temperature	– 55		125	0		70	C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.

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PARAMETER		TEST CONDITIONS †	SN54LS'		SN74LS'		UNIT			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IK}		$V_{CC} = \text{MIN.}$ $I_I = -18 \text{ mA}$			-1.5			-1.5	V	
V_{OH}	'LS594 Q	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX}$	$I_{OH} = -1 \text{ mA}$		2.4	3.2			V	
			$I_{OH} = -2.6 \text{ mA}$				2.4	3.1		
	Q_H'		$I_{OH} = -1 \text{ mA}$		2.4	3.2	2.4	3.2	V	
I_{OH}	'LS599 Q	$V_{CC} = \text{MIN.}$ $V_{OH} = 5.5 \text{ V}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX.}$					0.1		0.1	mA
V_{OL}	Q	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4	V	
			$I_{OL} = 24 \text{ mA}$				0.35	0.5		
			$I_{OL} = 8 \text{ mA}$		0.25	0.4	0.25	0.4		
	Q_H'		$I_{OL} = 16 \text{ mA}$				0.35	0.5		
I_I		$V_{CC} = \text{MAX.}$ $V_I = 7 \text{ V}$			0.1			0.1	mA	
I_{IH}		$V_{CC} = \text{MAX.}$ $V_I = 2.7 \text{ V}$			20			20	μA	
I_{IL}	SER	$V_{CC} = \text{MAX.}$ $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA	
	All others				-0.2			-0.2		
$I_{OS} \S$	'LS594 Q	$V_{CC} = \text{MAX.}$ $V_O = 0$	-30	-130	-30	-130			mA	
	Q_H'		-20	-100	-20	-100				
I_{CCH}	'LS594	$V_{CC} = \text{MAX.}$ All possible inputs grounded, All outputs open	34	50	34	50			mA	
	'LS599		30	45	30	45				
I_{CCL}	'LS594		42	65	42	65			mA	
	'LS599		38	55	38	55				

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics. $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$. (see note 3)

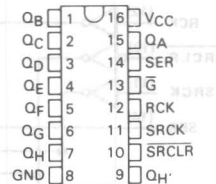
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS594			'LS599			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SRCK†	Q_H	$R_L = 1\text{ k}\Omega$,	$C_L = 30\text{ pF}$	12	18		12	18	ns	
t_{PHL}					15	23		17	25	ns	
t_{PLH}	RCK†	Q_A thru Q_H	$R_L = 667\text{ }\Omega$,	$C_L = 45\text{ pF}$	12	18		28	42	ns	
t_{PHL}					20	30		24	35	ns	
t_{PHL}	SRCLR‡	Q_H	$R_L = 1\text{ k}\Omega$,	$C_L = 30\text{ pF}$	22	33		24	35	ns	
t_{PHL}	RCLR‡	Q_A thru Q_H	$R_L = 667\text{ }\Omega$,	$C_L = 45\text{ pF}$	38	57		40	60	ns	

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

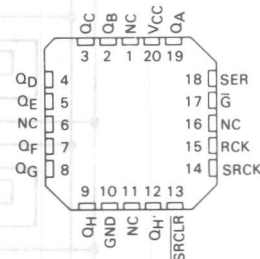
02634, JANUARY 1981 — REVISED DECEMBER 1983

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Guaranteed Shift Frequency: DC to 20 MHz

SN54LS595, SN54LS596 ... J OR W PACKAGE
SN74LS595, SN74LS596 ... J OR N PACKAGE
(TOP VIEW)



SN54LS595, SN54LS596 ... FK PACKAGE
SN74LS595, SN74LS596
(TOP VIEW)



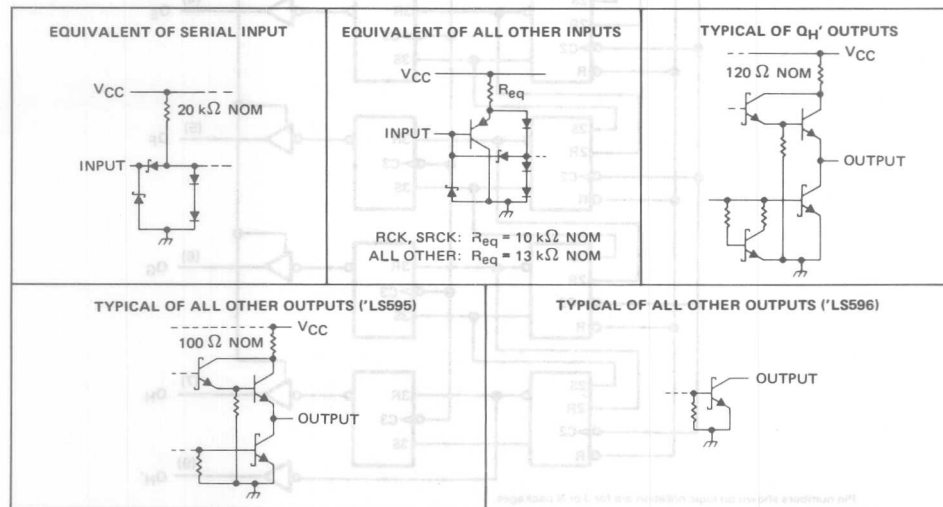
NC - No internal connection

description

These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

schematics of inputs and outputs



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TEXAS
INSTRUMENTS

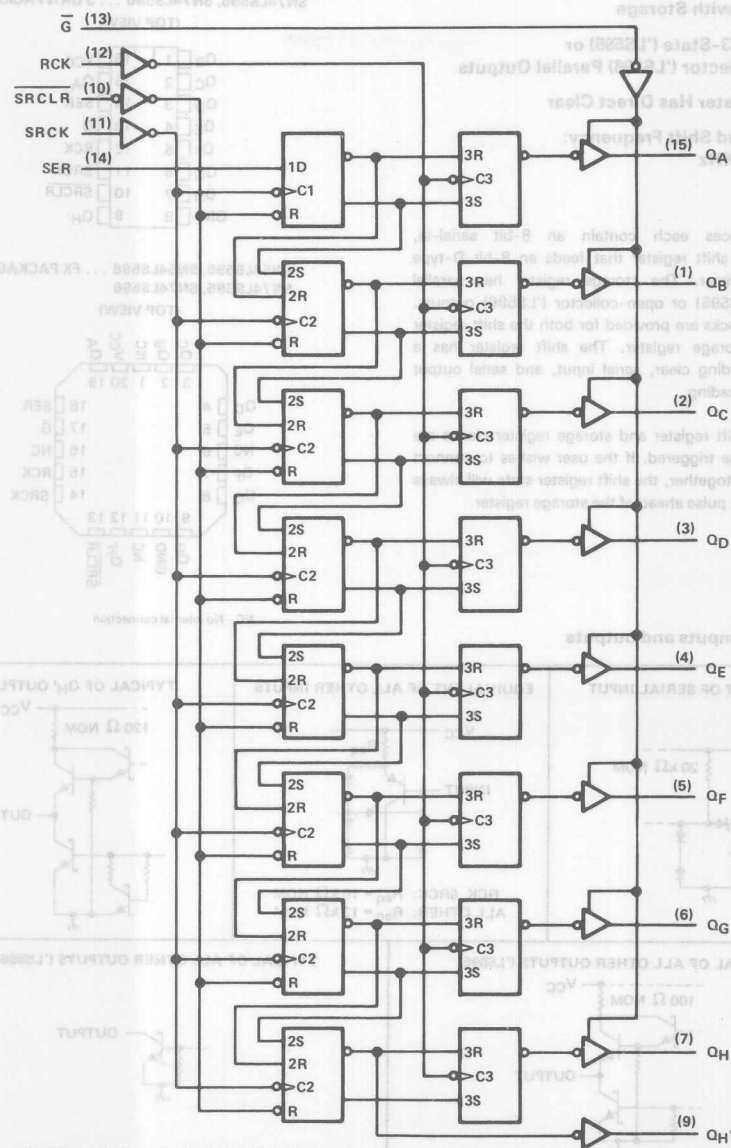
3-1001

3

TTL DEVICES

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

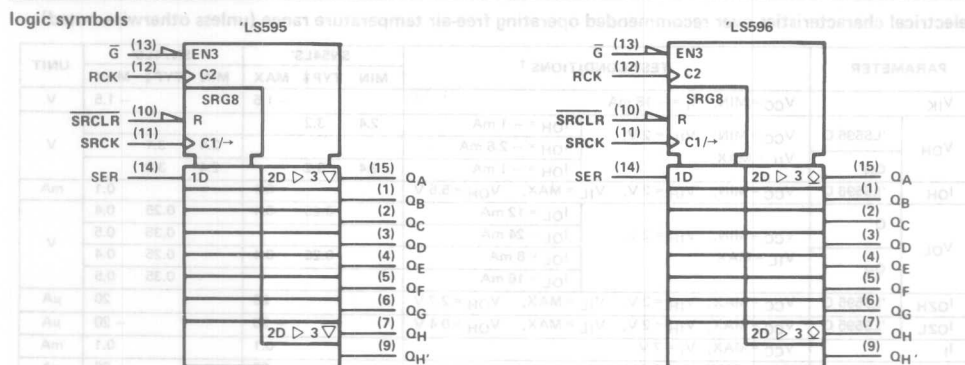
logic diagram (positive logic)



3

TTL DEVICES

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES



Pin numbers shown on logic notation are for J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596	-55°C to 125°C
SN74LS595, SN74LS596	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage	Q _A thru Q _H , 'LS596 only		5.5			5.5	V
I _{OH}	High-level output current	Q _H '		− 1			− 1	mA
		Q _A thru Q _H , 'LS595 only		− 1			− 2.6	
I _{OL}	Low-level output current	Q _H '		8			16	mA
		Q		12			24	
f _{SRCK}	Shift clock frequency	0		20	0		20	MHz
t _w (SRCK)	Duration of shift clock pulse	25			25			ns
t _w (RCK)	Duration of register clock pulse	20			20			ns
t _w (SRCLR)	Duration of shift clear pulse, low level	20			20			ns
t _{su}	Setup time	SRCLR inactive before SRCK ↑		20		20		ns
		SER before SRCK ↑		20		20		
		SRCK ↑ before RCK ↑ (see Note 2)		40		40		
		SRCLR low before RCK ↑		40		40		
t _h	Hold time	SER after SRCK ↑		0		0		ns
T _A	Operating free-air temperature	− 55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54LS*			SN74LS*			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	'LS595 Q	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OH} = -1 \text{ mA}$	2.4	3.2				V
	Q_H'		$I_{OH} = -2.6 \text{ mA}$			2.4	3.1		
I_{OH}	'LS596 Q	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OL}	Q	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4	V
			$I_{OL} = 24 \text{ mA}$				0.35	0.5	
	Q_H'		$I_{OL} = 8 \text{ mA}$	0.25	0.4		0.25	0.4	
			$I_{OL} = 16 \text{ mA}$				0.35	0.5	
I_{OZH}	'LS595 Q	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 2.7 \text{ V}$		20			20		μA
I_{OZL}	'LS595 Q	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 0.4 \text{ V}$		-20			-20		μA
I_I		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH}		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μA
I_{IL}	SER	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
	All others			-0.2			-0.2		
$I_{OS} §$	'LS595 Q	$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$		-30	-130		-30	-130	mA
	Q_H'			-20	-100		-20	-100	
I_{CCH}	'LS595	$V_{CC} = \text{MAX}$		33	50		33	50	mA
	'LS596			30	45		30	45	
I_{CCL}	'LS595	All possible inputs grounded,		42	65		42	65	mA
	'LS596			36	55		36	55	
I_{CCZ}	'LS595	All outputs open		44	65		44	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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TTL DEVICES

UNIT	SN54LS*		SN74LS*	
	MIN	MAX	MIN	MAX
V_{CC} Supply voltage	4.5	5.5	4.75	5.25
V_{IH} High-level input voltage	2		2	
V_{IL} Low-level input voltage	0.8		0.8	
V_{OH} High-level output voltage	2.4	3.2	2.4	3.1
I_{OH} High-level output current	-1		-1	
I_{OL} Low-level output current	15	24	15	24
Shift clock frequency	0	20	0	20
Duration of shift clock pulse	25	30	25	30
Duration of register clock pulse	25	30	25	30
Duration of shift clock pulse, low level	25	30	25	30
Setup time	25	30	25	30
Hold time	0	0	0	0
Operating free-air temperature	-55	125	-55	125

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS595			'LS596			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SRCK \uparrow	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	12	18		14	21		ns
t_{PHL}				17	25		20	30		ns
t_{PLH}	RCK \uparrow	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	12	18		28	42		ns
t_{PHL}				24	35		24	35		ns
t_{PZH}	$\overline{G} \downarrow$	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	20	30					ns
t_{PZL}				25	38					ns
t_{PHZ}	$\overline{G} \uparrow$	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$	20	30					ns
t_{PLZ}				25	38					ns
t_{PLH}	$\overline{G} \uparrow$	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$				40	60		ns
t_{PHL}	$\overline{G} \downarrow$	Q_A thru Q_H					25	38		ns
t_{PHL}	SRCLR \uparrow	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	24	35		24	35		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

switching characteristics $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T ₁ (ns)		UNIT
				MIN	MAX	
t _{PLH}	SCLK ↑	Q _H	R _L = 1 kΩ, C _L = 30 pF	12	18	ns
				17	22	ns
t _{PHL}	SCLK ↑	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	12	18	ns
				17	22	ns
t _{PLZ}	Q _L	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	20	30	ns
				25	35	ns
t _{PHZ}	Q _H	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	20	30	ns
				25	35	ns
t _{PLZ}	Q _L	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	20	30	ns
				25	35	ns
t _{PHZ}	Q _H	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	20	30	ns
				25	35	ns
t _{PLZ}	Q _L	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	20	30	ns
				25	35	ns
t _{PHZ}	Q _H	Q _L thru Q _H	R _L = 887 Ω, C _L = 45 pF	20	30	ns
				25	35	ns

NOTE 3: See General Information Section for test circuit and voltage waveform.

TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

02635, JANUARY 1981—REVISED DECEMBER 1983

- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Guaranteed Shift Frequency ... DC to 20 MHz

description

The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

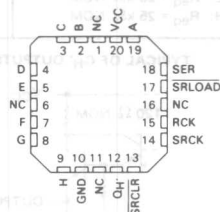
SN54LS597 ... J PACKAGE SN74LS597 ... J OR N PACKAGE

(TOP VIEW)



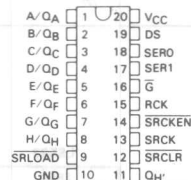
SN54LS597 ... FK PACKAGE SN74LS597

(TOP VIEW)



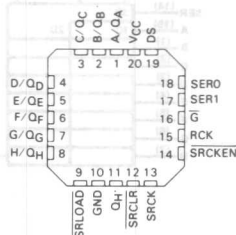
SN54LS598 ... J PACKAGE SN74LS598 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS598 ... FK PACKAGE SN74LS598

(TOP VIEW)



NC - No internal connection

PRODUCTION DATA

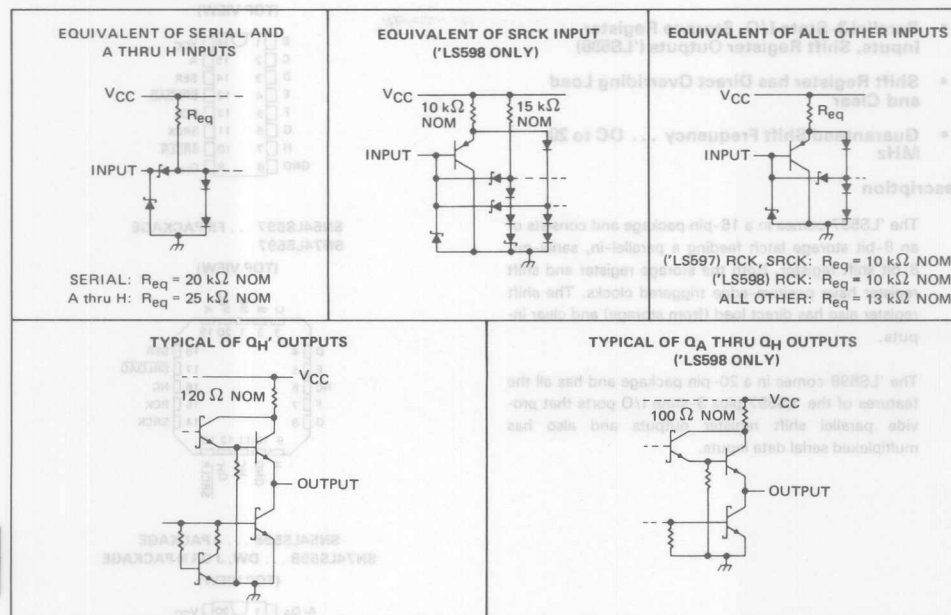
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TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

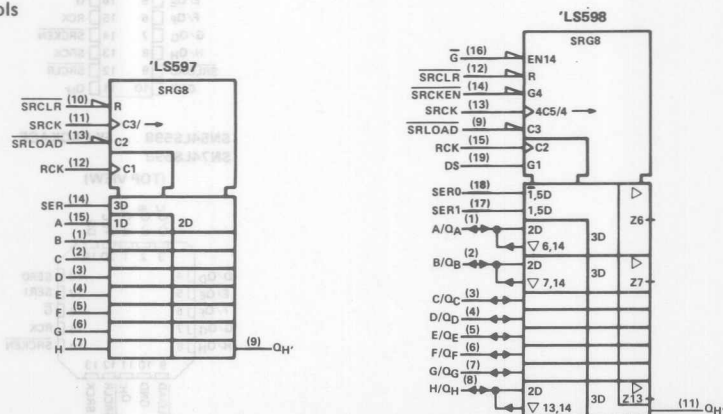
schematics of inputs and outputs



3

TTL DEVICES

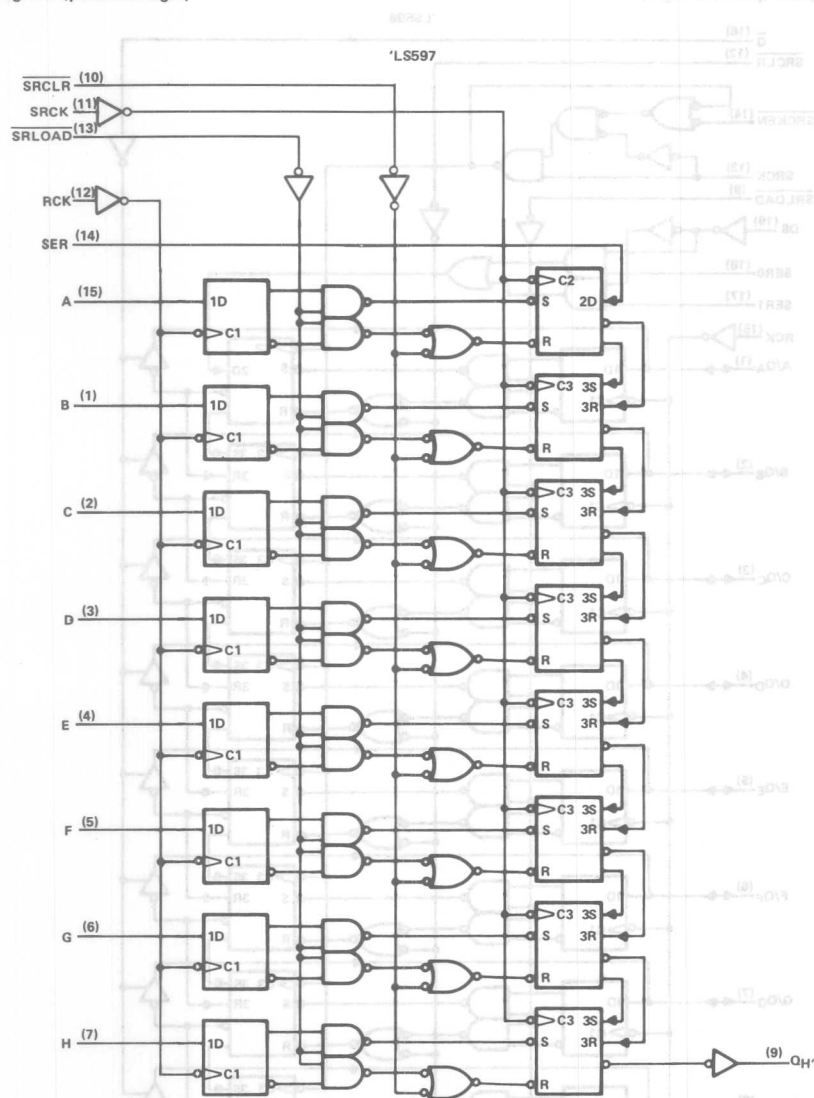
logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN54LS597, SN74LS597 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

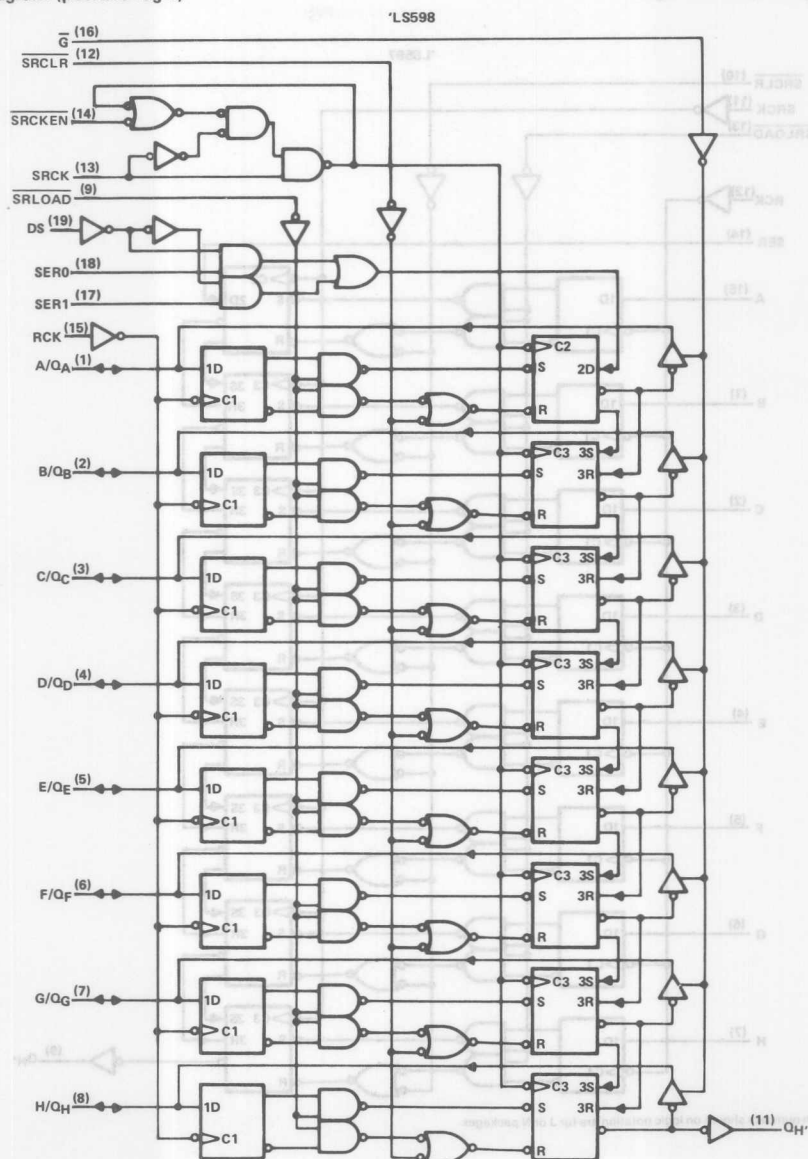
logic diagram (positive logic)



Pin numbers shown on logic notation are for J or N packages.

TYPES SN54LS598, SN74LS598
8-BIT SHIFT REGISTERS WITH INPUT LATCHES

logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598	– 55°C to 125°C
SN74LS597, SN74LS598	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS*			SN74LS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	Q_H^*		– 1	Q_H^*		– 1	mA
		Q_A thru Q_H , 'LS598 only		– 1	Q_A thru Q_H , 'LS598 only		– 2.6	
I_{OL}	Low-level output current	Q_H^*		8	Q_H^*		16	mA
		Q_A thru Q_H , 'LS598 only		12	Q_A thru Q_H , 'LS598 only		24	
f_{SCK}	Shift clock frequency	0	20		0	20		MHz
t_w	Pulse duration	SRCK	high	15	SRCK	high	15	ns
			low	35		low	35	
		RCK		20	RCK		20	
		SRCLR		20	SRCLR		20	
t_{su}	Setup time	SRLOAD		40	SRLOAD		40	ns
		Data before RCK ↑		20	Data before RCK ↑		20	
		DS before SRCK ↑ ('LS598 only)		30	DS before SRCK ↑ ('LS598 only)		30	
		SRCKEN low before SRCK ↑ ('LS598 only)		20	SRCKEN low before SRCK ↑ ('LS598 only)		20	
		SRCLR inactive before SRCK ↑		25	SRCLR inactive before SRCK ↑		25	
		SRLOAD inactive before SRCK ↑		30	SRLOAD inactive before SRCK ↑		30	
		RCK ↑ before SRLOAD ↑ (see Note 2)		40	RCK ↑ before SRLOAD ↑ (see Note 2)		40	
t_h	Hold time	SER before SRCK ↑		20	SER before SRCK ↑		20	ns
				0			0	
T_A	Operating free-air temperature	– 55	125		0	70		°C

NOTE 2: The RCK ↑ before SRLOAD ↑ setup time ensures the data saved by RCK ↑ will also be loaded into the shift register.

3

TTL DEVICES

TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS*			SN74LS*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = - 18 mA				- 1.5			- 1.5	V
V _{OH}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = - 1 mA	2.4	3.2					V
	Q _H '		I _{OH} = - 2.6 mA				2.4	3.1		
V _{OL}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = - 1 mA	2.4	3.2			2.4	3.2	V
	Q _H '		I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I _{OL} = 24 mA					0.35	0.5	
			I _{OL} = 8 mA		0.25	0.4		0.25	0.4	
			I _{OL} = 16 mA					0.35	0.5	
I _{OZH}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V	V _{IL} = MAX,				20		20	μA
I _{OZL}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V	V _{IL} = MAX,			- 0.4			- 0.4	mA
I _I	'LS598 Q	V _{CC} = MAX	V _I = 5.5 V			0.1			0.1	mA
	Others		V _I = 7 V		0.1		0.1			
I _{IH}		V _{CC} = MAX, V _I = 2.7 V				20		20	μA	
I _{IL}	'LS598 SRCK	V _{CC} = MAX, V _I = 0.4 V				- 0.8			- 0.8	mA
	SER, A Thru H				- 0.4		- 0.4			
	Others				- 0.2		- 0.2			
I _{OS} §	'LS598 Q	V _{CC} = MAX, V _O = 0 V				- 30	- 130	- 30	- 130	mA
	Q _H '				- 20	- 100	- 20	- 100		
I _{CC}	'LS597	V _{CC} = MAX, All possible inputs grounded, All outputs open	I _{CCH}			35	53	35	53	mA
			I _{CCL}			35	53	35	53	
	'LS598		I _{CCH}			45	68	45	68	
			I _{CCL}			54	80	54	80	
			I _{CCZ}			56	85	56	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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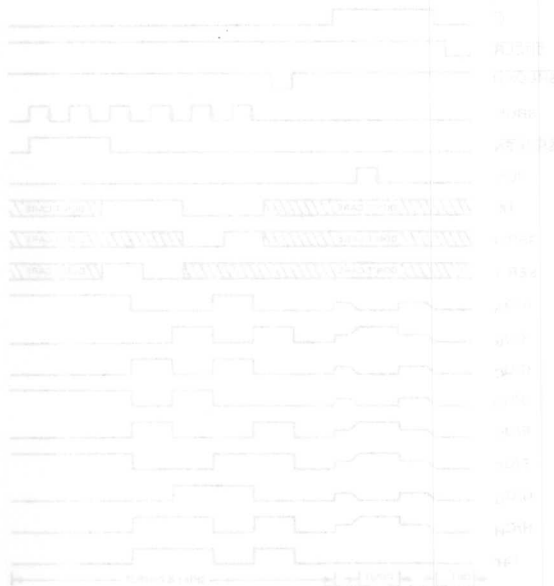
TTL DEVICES

TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS597			'LS598			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	SRCK			20	35		20	35		MHz
t_{PLH}	SRCK \uparrow	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$		15	23		11	17	ns
t_{PHL}	SRCK \uparrow	Q_H'			20	30		15	23	ns
t_{PLH}	SRLOAD \downarrow	Q_H'			38	57		28	42	ns
t_{PHL}	SRLOAD \downarrow	Q_H'			29	44		20	30	ns
t_{PHL}	SRCLR \downarrow	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$ SRLOAD = L		24	36		18	27	ns
t_{PLH}	RCK \uparrow	Q_H'			41	60		32	48	ns
t_{PHL}	RCK \uparrow	Q_H'			32	48		24	36	ns
t_{PLH}	SRCK \uparrow	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$					12	18	ns
t_{PHL}	SRCK \uparrow	Q						19	28	ns
t_{PLH}	SRLOAD \downarrow	Q						32	48	ns
t_{PHL}	SRLOAD \downarrow	Q						27	40	ns
t_{PHL}	SRCLR \downarrow	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$					25	38	ns
t_{PZH}	G \downarrow	Q						26	31	ns
t_{PZL}	G \downarrow	Q						29	43	ns
t_{PHZ}	G \uparrow	Q						25	38	ns
t_{PLZ}	G \uparrow	Q						20	30	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

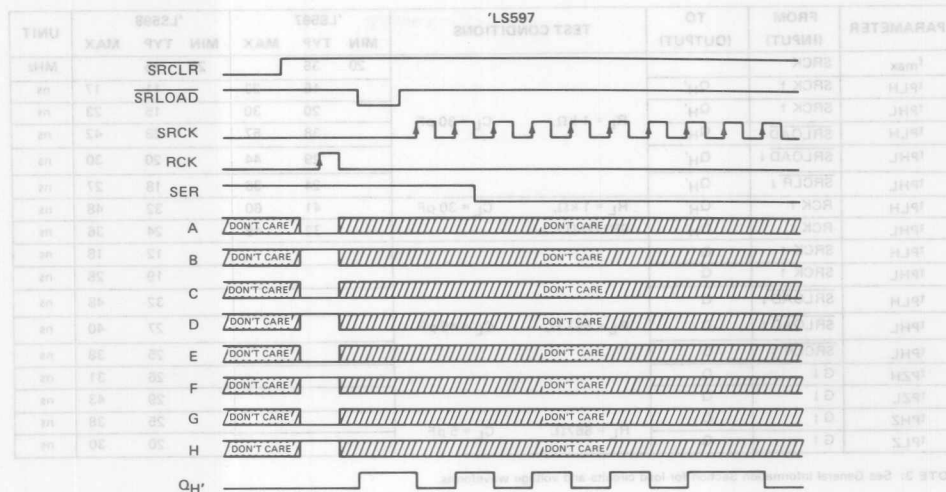


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TTL DEVICES

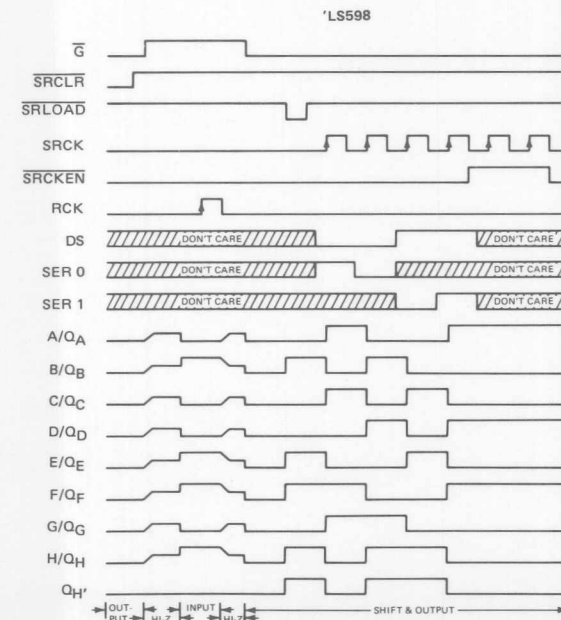
TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

typical operating sequences



3

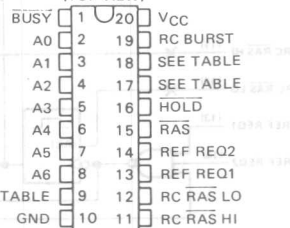
TTL DEVICES



TYPES SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

D2547, JANUARY 1981 REVISED JUNE 1983

SN54LS' ... J PACKAGE
SN74LS' ... DW, J OR N PACKAGE
(TOP VIEW)



FOR CHIP CARRIER INFORMATION
CONTACT THE FACTORY

SELECTION TABLE

DEVICE	REFRESH MODES	MEMORY SIZE	PIN ASSIGNMENTS		
			PIN 9	PIN 17	PIN 18
'LS600A	Transparent, Burst	4K or 16K	4K/16K	LATCHED RCO	RESET LATCHED RCO
'LS601A	Transparent, Burst	64K	A7	LATCHED RCO	RESET LATCHED RCO
'LS602A	Cycle Steal, Burst	4K or 16K	4K/16K	READY	RC CYCLE STEAL
'LS603A	Cycle Steal, Burst	64K	A7	READY	RC CYCLE STEAL

description

The 'LS600A thru 'LS603A memory refresh controllers contain one 8-bit synchronous counter, nine 3-state buffer drivers, four RC-controlled multivibrators, and other control circuitry on a single monolithic chip. These devices are designed to provide RAS-only refresh on 4K, 16K, and 64K dynamic RAMs. The 'LS600A and 'LS601A provide transparent refresh while the 'LS602A and 'LS603A provide cycle-steal refresh. In addition, a burst-mode timer is provided to warn the CPU that the maximum allowable refresh time is about to be violated.

operating modes

In the transparent refresh mode ('LS600A or 'LS601A), row-refresh cycles occur only during inactive CPU-memory times. In most cases the entire memory refresh sequence can be completed "transparently" without interrupting CPU operations. During idle CPU-memory periods, the REF REQ pins should be taken high so as many rows as possible can be refreshed. A low from BUSY will signal the CPU to wait until the end of that current row refresh before reinstating operations. If all row addresses have been refreshed before the burst-mode timer expires, the burst-mode timer will reset.

If the maximum allowable refresh time of the dynamic RAM is about to be exceeded, the burst mode timer will expire causing the HOLD pin to go low. This signals the CPU that a burst-mode refresh is mandatory and the burst-mode refresh will be accomplished when the CPU takes the REF REQ pins high. To ensure that all rows are refreshed, the address counter is reset to zero whenever the burst-mode timer expires. After the last row has been refreshed, the HOLD pin will return high, and the burst-mode timer will reset. The CPU can then return to normal transparent operation.

A LATCHED RCO output pin is also provided on the 'LS600A and 'LS601A to detect when the last row has been refreshed. Upon seeing a RCO from the address counter, the LATCHED RCO output will be set high. This latch is reset by providing a high-going pulse on the RESET LATCHED RCO input.

In the cycle-steal refresh mode ('LS602A or 'LS603A), refreshing is accomplished by dividing the safe refresh time into equal segments and refreshing one row in each segment. The segment time is programmed via the RC CYCLE STEAL input and will produce a low level on the READY output at the end of each segment period. This indicates to the CPU to suspend operations for one memory cycle for a row refresh. In effect it "steals" one memory cycle from the CPU. After the CPU recognizes the cycle-steal signal from the READY output, it must take both REF REQ pins high. These devices will then refresh one row and return control back to the CPU by taking READY high. The burst-mode timer is also provided to prevent exceeding the maximum allowable refresh time, and operates in the same manner as in the 'LS600A and 'LS601A. In applications where the burst-mode timer is not required, it can be disabled by connecting the RC Burst input to ground.

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TEXAS
INSTRUMENTS

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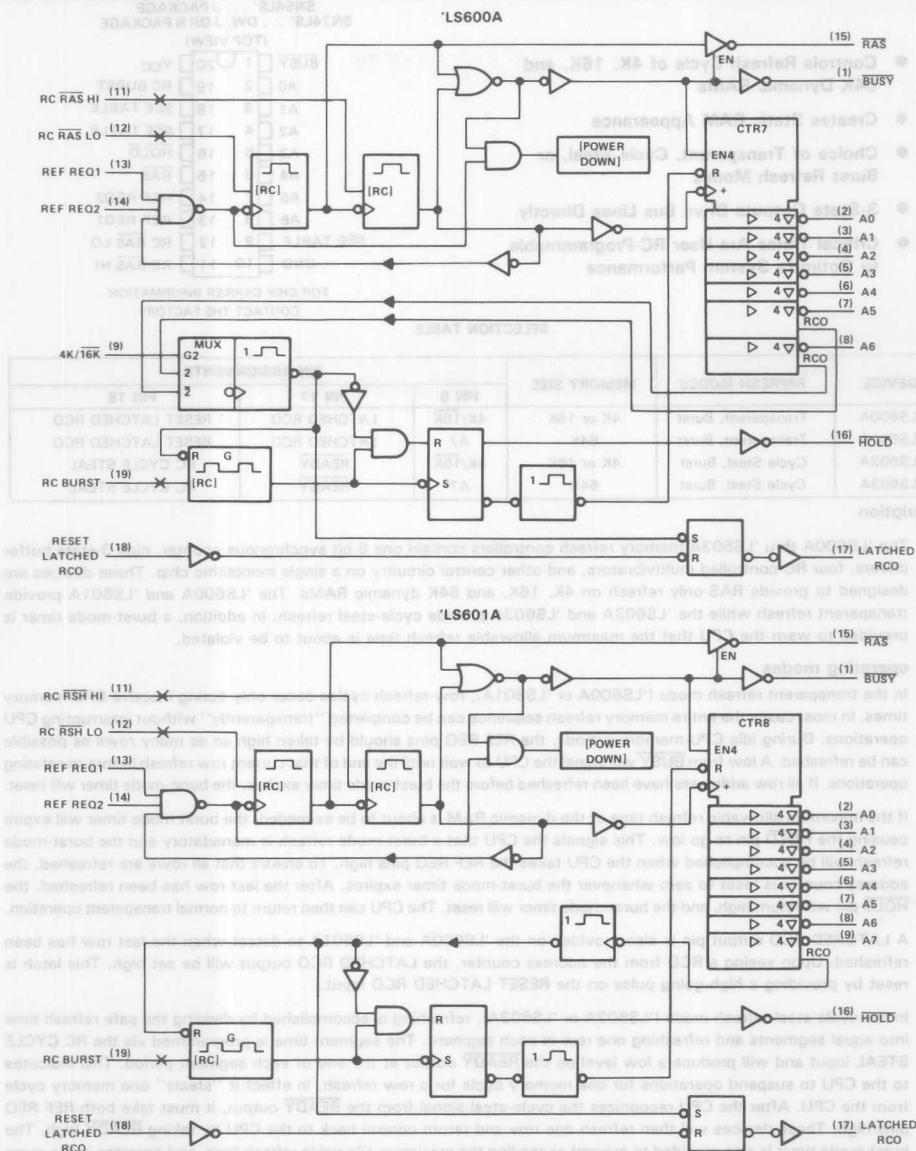
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TTL DEVICES

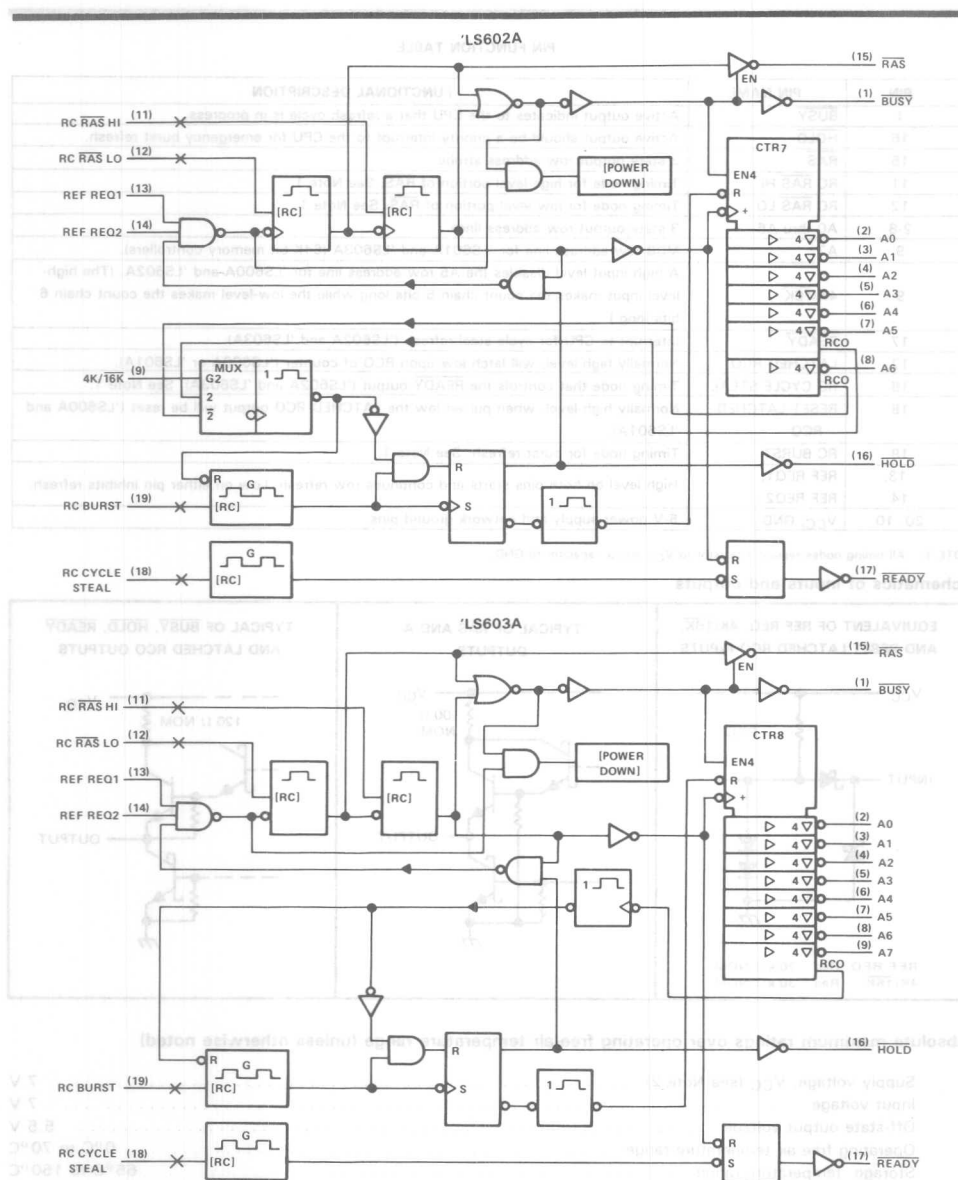
TYPES SN74LS600A, SN74LS601A MEMORY REFRESH CONTROLLERS

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Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN74LS602A, SN74LS603A MEMORY REFRESH CONTROLLERS



Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

PIN FUNCTION TABLE

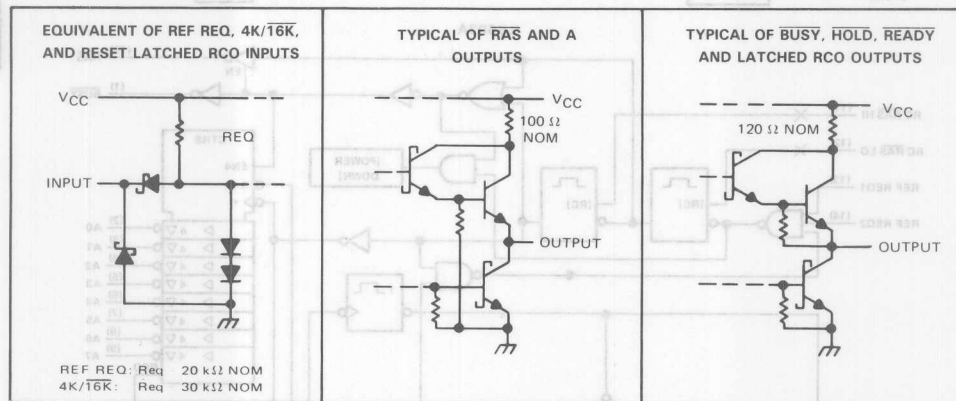
PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	BUSY	Active output indicates to the CPU that a refresh cycle is in progress.
16	HOLD	Active output should be a priority interrupt to the CPU for emergency burst refresh.
15	RAS	3-state output row address strobe.
11	RC RAS HI	Timing node for high-level portion of RAS. See Note 1.
12	RC RAS LO	Timing node for low-level portion of RAS. See Note 1.
2-8	A0 thru A6	3-state output row address lines.
9	A7	MSB row address line for 'LS601A and 'LS603A (64K-bit memory controllers).
9	4K/16K	A high input level disables the A5 row address line for 'LS600A and 'LS602A. (The high-level input makes the count chain 5 bits long while the low-level makes the count chain 6 bits long.)
17	READY	Interrupt to CPU for cycle steal refresh ('LS602A and 'LS603A).
17	LATCHED RCO	Normally high-level, will latch low upon RCO of counter ('LS600A or 'LS601A).
18	RC CYCLE STEAL	Timing node that controls the READY output ('LS602A and 'LS603A). See Note 1.
18	RESET LATCHED RCO	Normally high-level, when pulsed low the LATCHED RCO output will be reset ('LS600A and 'LS601A).
19	RC BURST	Timing node for burst refresh. See Note 1.
13, 14	REF REQ1, REF REQ2	High level on both pins starts and continues row refresh. Low on either pin inhibits refresh.
20, 10	V _{CC} , GND	5-V power supply and network ground pins.

NOTE 1: All timing nodes require a resistor to V_{CC} and a capacitor to GND.

schematics of inputs and outputs

3

TTL DEVICES



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 2)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

NOTE 2: Voltage values are with respect to network ground terminal.

TYPES SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	A, \overline{RAS}			-2.6	mA
	All others			-400	μ A
Low-level output current, I_{OL}	A, \overline{RAS}			24	mA
	All others			8	mA
Duration of \overline{RAS} output pulse [†]	High, t_{SHSL}	75			ns
	Low, t_{SLSH}	75			ns
Duration of RESET LATCHED RCO pulse, t_{RHRL}		35			ns
Duration of REF REQ pulse during CYCLE STEAL operation, t_{QHQL}		20			ns
External timing resistor, R_{ext}	RC \overline{RAS} LO, RC \overline{RAS} HI	1		6	k Ω
	RC BURST, RC CYCLE STEAL	1		1000	k Ω
Operating free-air temperature, T_A		0		70	°C

[†]Maximum operating frequency for the address counter corresponds to its minimum period, which is the sum of $t_{w(RAS-H)}$ min and $t_{w(RAS-L)}$ min.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = 4.75$ V, $I_I = -1.8$ mA				-1.5	V
V_{OH}	High-level output voltage	A, \overline{RAS}	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OH} = -2.6$ mA	2.4	2.9	V
		All Others		$I_{OH} = -400$ μ A	2.7	3.1	
V_{OL}	Low-level output voltage	A, \overline{RAS}	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 12$ mA	0.25	0.4	V
				$I_{OL} = 24$ mA	0.35	0.5	
		All Others		$I_{OL} = 4$ mA	0.25	0.4	
					$I_{OL} = 8$ mA	0.35	
I_{OZH}	Off-state output current, high-level voltage applied	A, \overline{RAS}	$V_{CC} = 5.25$ V REF REQ at $V_{IL} = 0.8$ V	$V_O = 2.7$ V	20	μ A	
I_{OZL}	Off-state output current, low-level voltage applied			$V_O = 0.4$ V	-20	μ A	
I_I	Input current at maximum input voltage	$V_{CC} = 5.25$ V, $V_I = 7$ V			0.1	mA	
I_{IH}	High-level input current	$V_{CC} = 5.25$ V, $V_I = 2.7$ V			20	μ A	
I_{IL}	Low-level input current	$V_{CC} = 5.25$ V, $V_I = 0.4$ V			0.4	mA	
I_{OS}	Short-circuit output current [§]	A, \overline{RAS}	$V_{CC} = 5.25$ V		-30	-130	mA
		All others			-20	-100	
I_{CC}	Supply current	$V_{CC} = 5.25$ V, RC \overline{RAS} LO and REF REQ at 0 V			50	85	mA

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

TYPES SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{QHBL}	REF REQ \dagger	BUS \ddagger	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	30	45		ns
t_{SLBH}^\dagger	RAS \dagger	BUS \ddagger		245	300		ns
t_{QHSV}	REF REQ \dagger	RAS	$C_L = 320\text{ pF}$, $R_L = 667\Omega$	47	70		ns
t_{SHSZ}^\dagger	RAS \dagger	RAS	$C_L = 5\text{ pF}$, $R_L = 667\Omega$	245	300		ns
t_{QHAV}	REF REQ \dagger	ADDRESS	$C_L = 160\text{ pF}$, $R_L = 667\Omega$	38	65		ns
t_{SHAZ}^\dagger	RAS \dagger	ADDRESS	$C_L = 5\text{ pF}$, $R_L = 667\Omega$	245	300		ns
t_{RHCL}	RESET LATCHED	LATCHED	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	37	55		ns
t_{SHYH}	RCO \dagger	RCO		64	85		ns
t_{SLSH}^\dagger	RAS \dagger	READY	$C_L = 320\text{ pF}$, $R_L = 667\Omega$	210			ns
t_{SHSL}^\dagger	RAS \dagger	RAS		245			ns
t_{DHDL}^\S	HOLD \dagger	HOLD	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	3.56			ms
t_{LYL}^\dagger	READY \dagger	READY		27			μs

† Depends on RC network at pin 11 (4 k Ω , 200 pF used for testing).

‡ Depends on RC network at pin 12 (4 k Ω , 200 pF used for testing).

§ Depends on RC network at pin 19 (680 k Ω , 0.022 μF used for testing).

† Depends on RC network at pin 18 (10 k Ω , 0.01 μF used for testing).

NOTE 3: See General Information Section for load circuits and voltage waveforms.

explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

t_{AB-CD}

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high

L = low or transition to low

V = a valid steady-state level

X = unknown, changing, or "don't care" level

Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A or C SUBSCRIPT
BUS \ddagger	B
HOLD	D
RAS \dagger	S
A0 - A7	A
READY \dagger	Y
LATCHED RCO	C
RESET LATCHED RCO	R
REF REQ \dagger	Q

3 TTL DEVICES

TYPES SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

TIMING DIAGRAMS

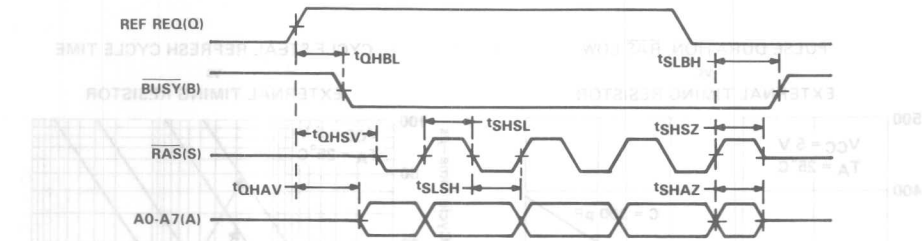


FIGURE 1 - TRANSPARENT REFRESH

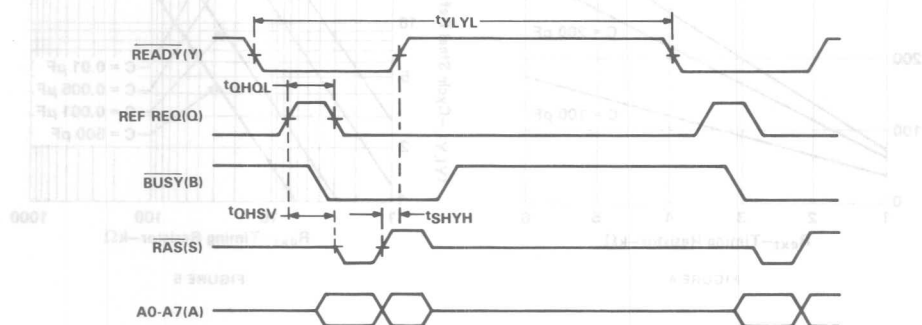
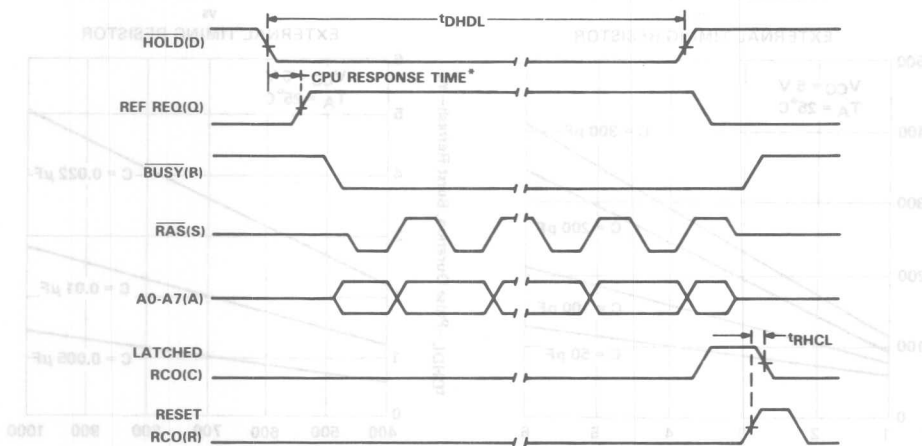


FIGURE 2 - CYCLE STEAL REFRESH



* During testing, an 'LS04 is used to invert $\overline{\text{HOLD}}$ to provide the REF REQ input.

FIGURE 3 - BURST MODE REFRESH

TYPES SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

TYPICAL CHARACTERISTICS

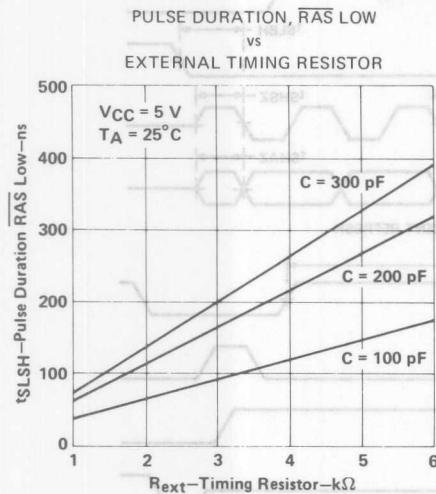


FIGURE 4

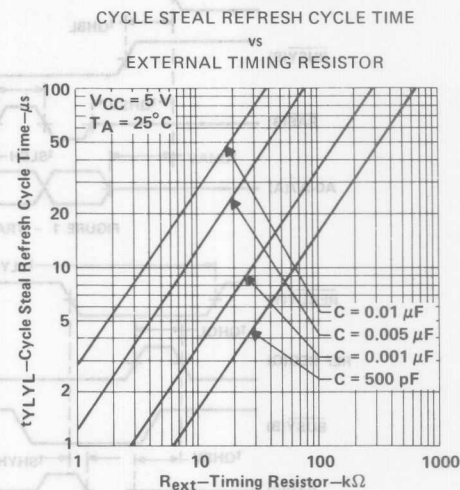


FIGURE 5

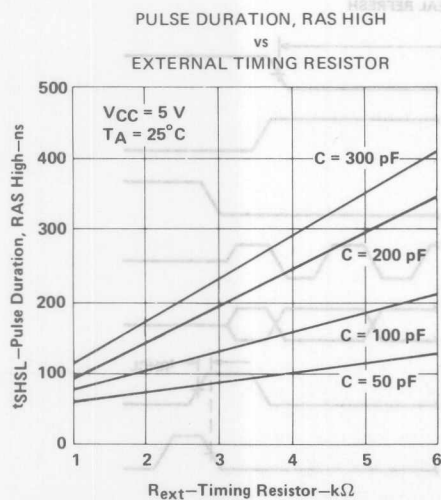


FIGURE 6

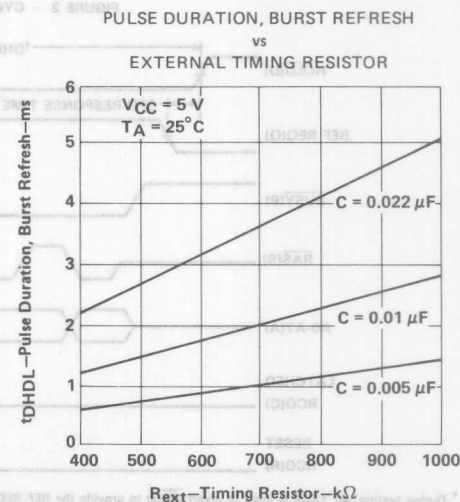


FIGURE 7

3

TTL DEVICES

TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES

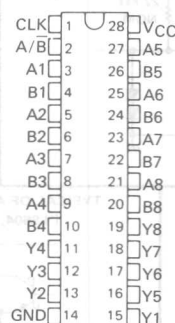
D2545, JULY 1979 — REVISED DECEMBER 1983

(TIM99604 THRU TIM99607)

- Choice of Outputs:
Three-State ('LS604, 'LS606)
Open-Collector ('LS605, 'LS607)
- 16 D-Type Registers, One for each Data Input
- Multiplexer Selects Stored Data from Either A Bus or B Bus
- Application Oriented:
Maximum Speed ('LS604, 'LS605)
Glitch-Free Operation ('LS606, 'LS607)

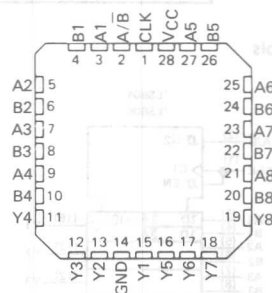
SN54LS604 thru SN54LS607 ... JD PACKAGE
SN74LS604 thru SN74LS607 ... JD OR N PACKAGE

(TOP VIEW)



SN54LS604 thru SN54LS607 ... FK PACKAGE
SN74LS604 thru SN74LS607

(TOP VIEW)



description

The 'LS604 through 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 and 'LS605 are optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

The SN54LS604 through SN54LS607 are characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS604 through SN74LS607 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS				OUTPUTS
A1-A8	B1-B8	SELECT A/B	CLOCK	Y1-Y8
A data	B data	L	\uparrow	B data
A data	B data	H	\uparrow	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = high level (steady state)

L = low level (steady state)

X = irrelevant

Z = high-impedance state

Off = H if pull-up resistor is connected to open-collector output

\uparrow = transition from low to high level

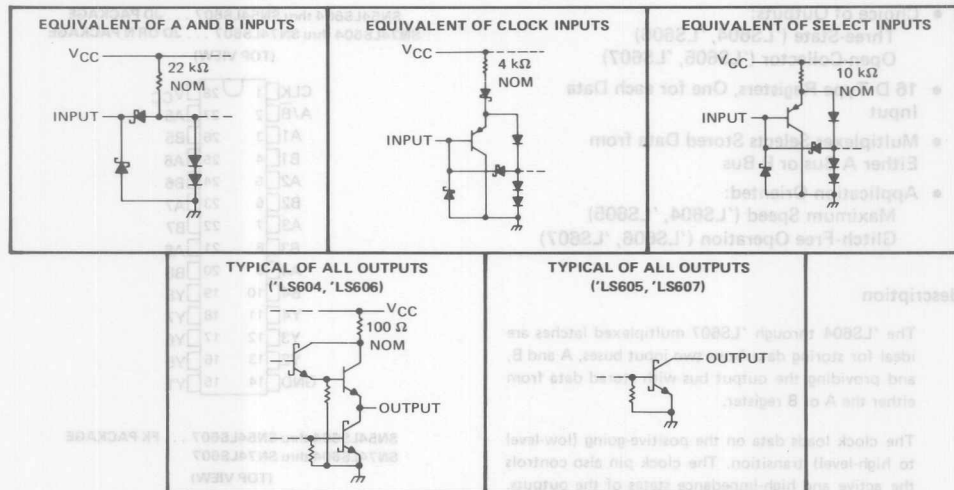
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES

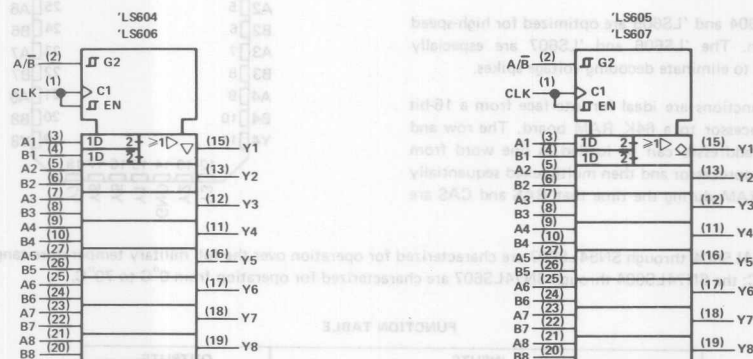
schematics of inputs and outputs



3

TTL DEVICES

logic symbols



Pin numbers shown on logic notation are for JD or N packages.

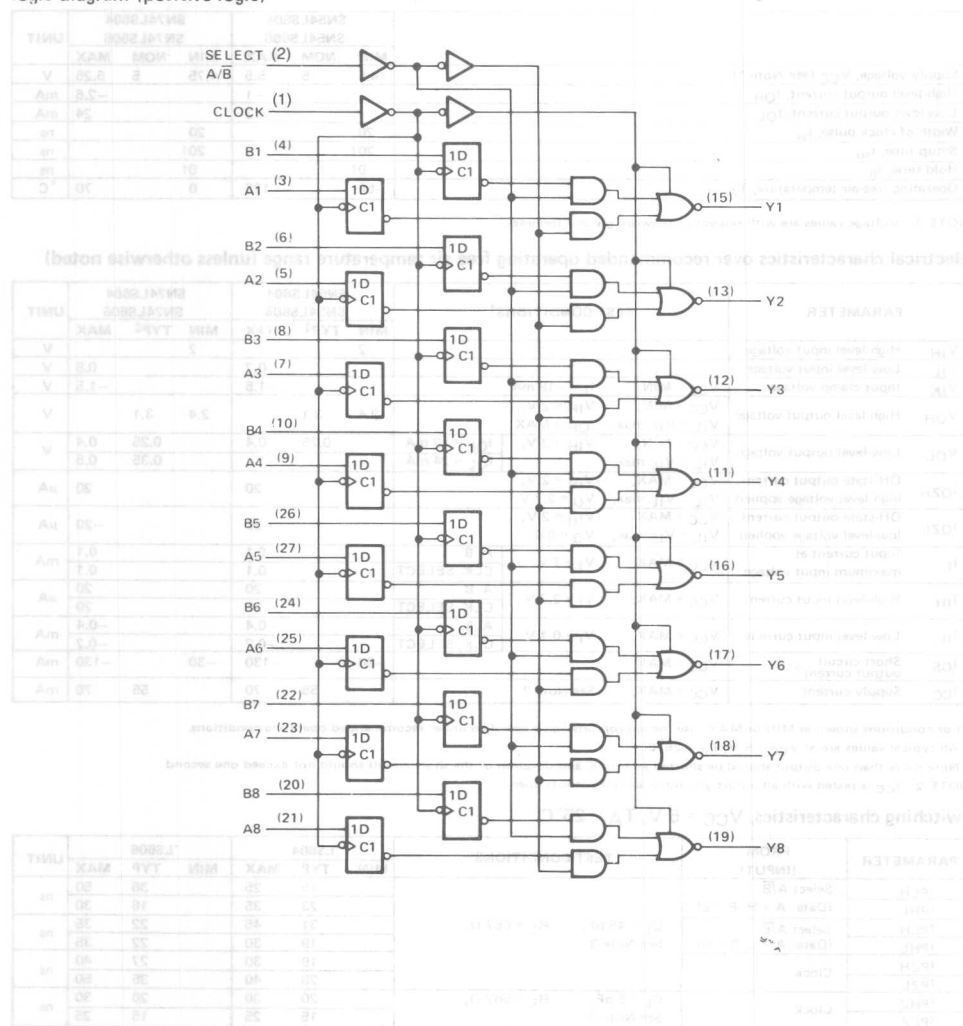
SELECT A/B	SELECT B	SELECT C	SELECT D
0	0	0	0
0	1	0	0
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

0 = low-level (steady state)
1 = high-level (steady state)
X = unknown
OH = M, H, full-up resistor is connected to open-collector output
I = transition from low to high level

TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607

OCTAL 2-INPUT MULTIPLEXED LATCHES

logic diagram (positive logic)



3

TTL DEVICES

TYPES SN54LS604, SN54LS606, SN74LS604, SN74LS606

OCTAL 2-INPUT MULTIPLEXED LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_W	20			20			ns
Setup time, t_{su}	20†			20†			ns
Hold time, t_h	0†			0†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = \text{MAX}$	2.4	3.1		2.4	3.1		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_O = 2.7 \text{ V}$			20			20	µA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_O = 0.4 \text{ V}$			-20			-20	µA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.1			0.1		mA
	CLK, SELECT		0.1			0.1		
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		20			20		µA
	CLK, SELECT		20			20		
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
	CLK, SELECT		-0.2			-0.2		
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-30		-130	-30		-130	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	55	70		55	70		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS604			'LS606			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select A/B	$C_L = 45 \text{ pF}$, $R_L = 667 \Omega$, See Note 3	15	25		36	50		ns
t_{PHL}	(Data: A = H, B = L)		23	35		16	30		
t_{PLH}	Select A/B		31	45		22	35		ns
t_{PHL}	(Data: A = L, B = H)		19	30		22	35		
t_{PZH}	Clock	$C_L = 5 \text{ pF}$, $R_L = 667 \Omega$, See Note 3	19	30		27	40		ns
t_{PZL}	Clock		28	40		35	50		
t_{PHZ}	Clock		20	30		20	30		ns
t_{PLZ}	Clock		15	25		15	25		

t_{PLH} propagation delay time, low-to-high-level output

t_{PHL} propagation delay time, high-to-low-level output

t_{PZH} output enable time to high level

t_{PZL} output enable time to low level

t_{PHZ} output disable time from high level

t_{PLZ} output disable time from low level

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS605, SN54LS607, SN74LS605, SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_W	20			20			ns
Setup time, t_{SU}	20†			20†			ns
Hold time, t_H	0†			0†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA				−1.5			−1.5	V
I _{OH}	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _{OH} = 5.5 V				250			250	µA
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max		I _{OL} = 12 mA		0.25	0.4	I _{OL} = 12 mA		V
				I _{OL} = 24 mA				I _{OL} = 24 mA		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V		A, B		0.1		0.1		mA
				CLK, SELECT		0.1		0.1		
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V		A, B		20		20		µA
				CLK, SELECT		20		20		
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V		A, B		−0.4		−0.4		mA
				CLK, SELECT		−0.2		−0.2		
I _{CC}	Supply current	V _{CC} = MAX,	See Note 2			40	60	40	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS605			'LS607			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Select A/ \overline{B}	C _L = 45 pF, R _L = 667 Ω , See Note 3	28	40		51	70	ns	
t _{PHL}	(Data: A = H, B = L)		28	40		21	30		
t _{PLH}	Select A/ \overline{B}		39	60		28	40	ns	
t _{PHL}	(Data: A = L, B = H)		25	40		28	40		
t _{PLH}	Clock		27	40		30	45	ns	
t _{PHL}			25	40		32	45		

t_{PLH} = propagation delay time, low to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS608, SN74LS608 (TIM99608) MEMORY CYCLE CONTROLLERS

D2548, JANUARY 1981 — REVISED DECEMBER 1981

- Provides Correct Timing for Memory Cycles

- Read Cycle
- Write Cycle
- Read-Modify-Write Cycle
- RAS-Only Refresh Cycle

- Page or Normal Modes

- Stand-Alone Controller for CPU-to-Memory Interface

- Also Designed to be Part of a Three-Chip Set Consisting of 'LS600 thru 'LS603, 'LS604 thru 'LS607, and 'LS608

- RAS Output is 3-State to Share Bus With 'LS600 thru 'LS603

- Critical Times Are User RC-Programmable to Optimize System Performance

description

The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

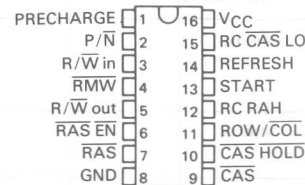
The 'LS608 can operate as a stand-alone interface but it is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper RAS, CAS, and READ/WRITE output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

MEMORY CYCLE	MODE	INPUT CONDITIONS						
		P/N IN	R/W IN	RMW IN	RAS ENABLE IN	CAS HOLD IN	START IN	REFRESH IN
READ	PAGE	H	H	H	L	H	↑	L
WRITE		H	L	H	L	H	↑	L
READ-MODIFY-WRITE		H	H	L	L	H	↑	L
READ	NORMAL	L	H	H	L	H	↑	L
WRITE		L	L	H	L	H	↑	L
READ-MODIFY-WRITE		L	H	L	L	H	↑	L
REFRESH	REFRESH	x	x	x	L	H	↑	H
EXTERNAL REFRESH		x	x	x	H	H	x	L

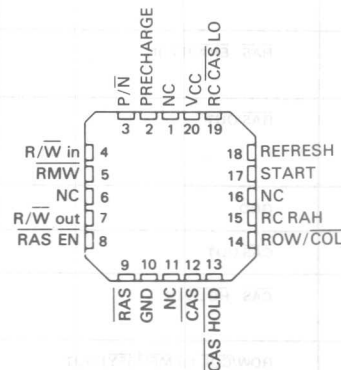
H = High, L = Low, x = irrelevant, ↑ = low-to-high transition

SN54LS608 ... J PACKAGE SN74LS608 ... D, J OR N PACKAGE (TOP VIEW)



SN54LS608 ... FK PACKAGE SN74LS608

(TOP VIEW)



NC — No internal connection

3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-1029

TYPES SN54LS608, SN74LS608 MEMORY CYCLE CONTROLLERS

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	RC PRECHARGE	User-programmable timing node* for precharge ($\overline{\text{CAS}}$ high and $\overline{\text{RAS}}$ high).
2	$\overline{\text{P}}/\overline{\text{N}}$ IN	When high, initiates a ready cycle (holds $\overline{\text{R}}/\overline{\text{W}}$ OUT high) and, when low, page mode read or write cycle holds $\overline{\text{RAS}}$ continuously low while $\overline{\text{CAS}}$ and column addresses are sequenced.
3	$\overline{\text{R}}/\overline{\text{W}}$ IN	When high, initiates a ready cycle (holds $\overline{\text{R}}/\overline{\text{W}}$ OUT high) and, when low, initiates a write cycle (holds $\overline{\text{R}}/\overline{\text{W}}$ OUT low) if pin 4 is high and pin 14 is low.
4	RMW IN	When low, enables read-modify-write cycle. $\overline{\text{R}}/\overline{\text{W}}$ IN must be high at the start of the RMW cycle.
5	$\overline{\text{R}}/\overline{\text{W}}$ OUT	When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally, ties to a W memory input in a system.
6	$\overline{\text{RAS}}$ ENABLE IN	When low, enables $\overline{\text{RAS}}$ output. When high, $\overline{\text{RAS}}$ is in the high-impedance or third state.
7	$\overline{\text{RAS}}$ OUT	3-state row-address-strobe output controlled by $\overline{\text{RAS}}$ ENABLE IN. In the three-chip controller set, the $\overline{\text{RAS}}$ output of the 'LS608 ties to the $\overline{\text{RAS}}$ output of the refresh controller ('LS600 thru 'LS603).
8	GND	Device and substrate ground.
9	$\overline{\text{CAS}}$ OUT	Column-address-strobe output.
10	$\overline{\text{CAS}}$ HOLD IN	When low, allows $\overline{\text{CAS}}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle.
11	ROW/ $\overline{\text{COL}}$ (or MEMBSY) OUT	In a system where the 'LS608 is a stand-alone controller, this output indicates a memory-busy condition to the microprocessor. When the 'LS608 is used as a part of a three-chip controller set, this pin ties to the SELECT A/B input of the multiplexer ('LS604 thru 'LS607) for selecting row and column in addition to indicating a memory-busy condition to the microprocessor.
12	RC RAH	User-programmable timing node* for row address hold time. (high level at ROW/ $\overline{\text{COL}}$ OUT).
13	START IN	When changed from low to high, initiates a memory cycle.
14	REFRESH IN	When high, enables $\overline{\text{RAS}}$ -only refresh cycle.
15	RC CAS LO	User-programmable timing node* for column-address-strobe low time.
16	V_{CC}	5-volt power supply terminal.

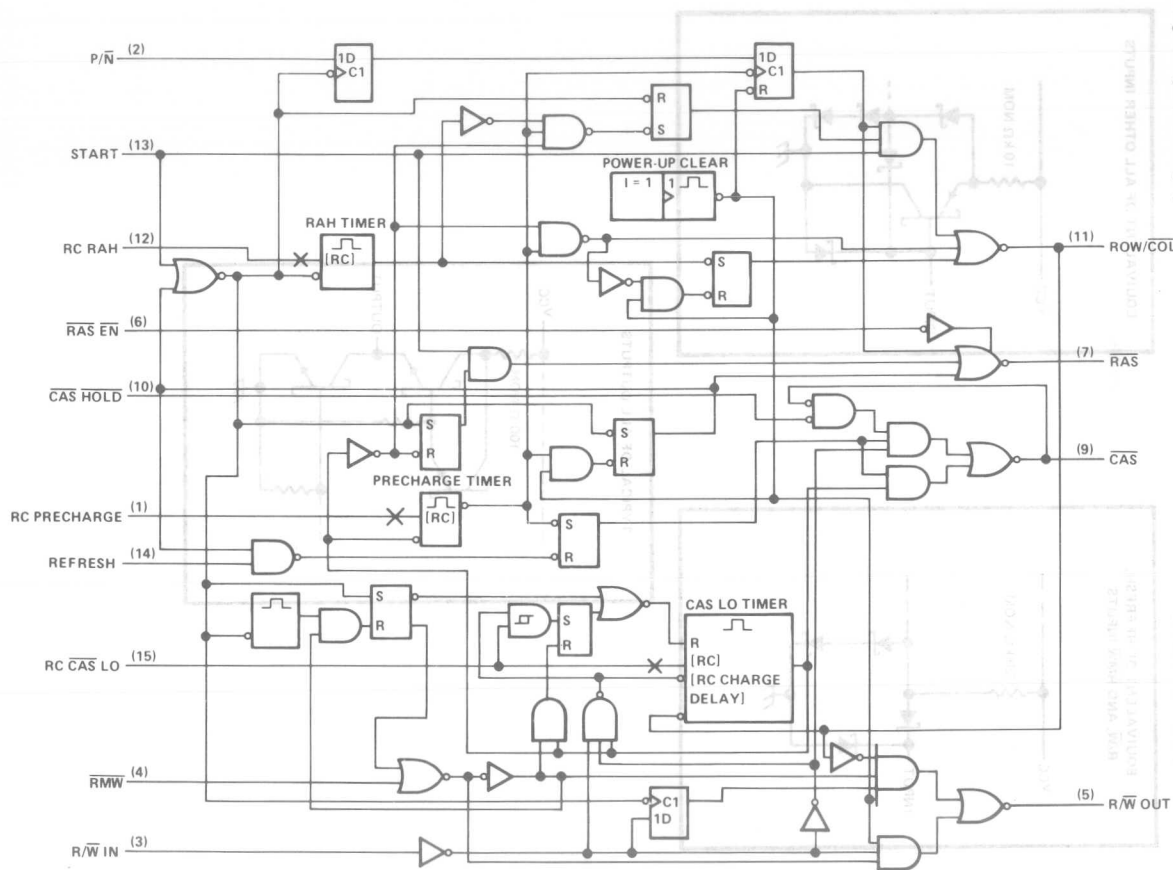
*All timing nodes require a resistor to V_{CC} and a capacitor to ground. Programmed time is approximately 0.29 RC.

3

TTL DEVICES

TYPES SN54LS608, SN74LS608
MEMORY CYCLE CONTROLLERS

logic diagram (positive logic)



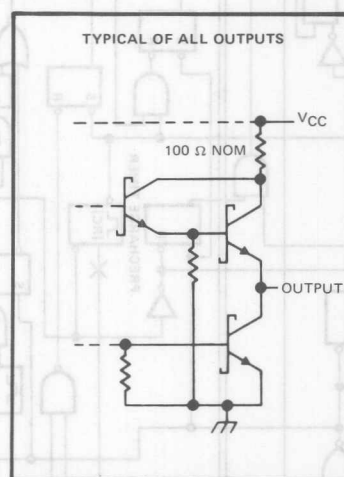
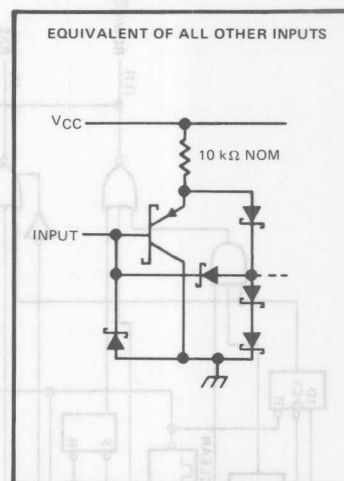
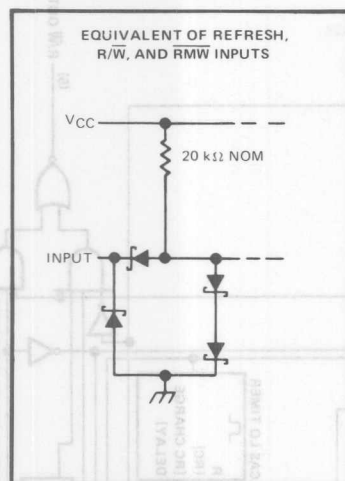
Pin numbers shown on logic notation are for D, J or N packages.

TTL DEVICES



TYPES SN54LS608, SN74LS608 MEMORY CYCLE CONTROLLERS

schematics of inputs and outputs



3

TTL DEVICES

TYPES SN54LS608, SN74LS608 MEMORY CYCLE CONTROLLERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS608	– 55° C to 125° C
SN74LS608	0° C to 70° C
Storage temperature range	– 65° C to 150° C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS608			SN74LS608			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	ROW/COL			– 0.4			– 0.4	mA
		RAS			– 1			– 2.6	
		All others			– 1.2			– 1.2	
I_{OL}	Low-level output current	ROW/COL			4			8	mA
		All others			12			24	
t_{su}	Setup time	R/W, RMW, P/N, or REFRESH to START †	20			20			ns
		CAS HOLD to CAS ‡	20			20			
t_h	Hold time		0			0			ns
R_{ext}	External timing resistor	RC RAH	0.1		2	0.1		2	k Ω
		RC CAS LO, RC PRECHARGE	1		6	1		6	
T_A	Operating free-air temperature		– 55		125	0		70	° C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS608		SN74LS608		UNIT
					MIN	TYP‡	MAX	MIN	
VIK		VCC = MIN II = – 18 mA			– 1.5		– 1.5		V
VOH	ROW/COL	VCC = MIN, VIL = MAX	VIH = 2 V,	IOH = – 400 μA	2.5	3.4	2.7	3.4	V
	IOH = MAX			2.4	3.2	2.4	3.1		
	Others			IOH = – 1.2 mA	2.4	3.2	2.4	3.2	
VOL	ROW/COL	VCC = MIN, VIH = 2 V,	VIL = MAX	IOL = 4 mA	0.25 0.4		0.25 0.4		V
	IOL = 8 mA					0.35 0.5			
	IOL = 12 mA			0.25 0.4		0.25 0.4			
	IOL = 24 mA					0.35 0.5			
IOZH	RAS	VCC = MAX, VIH = 2 V, VIL = MAX, VO = 2.7 V			20		20		μA
IOZL	RAS	VCC = MAX, VIH = 2 V, VIL = MAX, VO = 0.4 V			– 20		– 20		μA
II		VCC = MAX, VI = 7 V			0.1		0.1		mA
IIH		VCC = MAX, VI = 2.7 V			20		20		μA
IIL	REFRESH, R/W, RMW	VCC = MAX, VI = 0.4 V			– 0.4		– 0.4		mA
	Others				– 0.2		– 0.2		
IO	ROW/COL	VCC = MAX		VO = 2.25 V	– 10	– 50	– 10	– 50	mA
	Others			VO = 0 V §	– 30	– 130	– 30	– 130	
ICC		VCC = MAX, Outputs open, All inputs at GND			38 65		38 65		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

TYPES SN54LS608, SN74LS608 MEMORY CYCLE CONTROLLERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$ to GND (see waveforms for more detail)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MODE	MIN	TYP	MAX	UNIT
t_{PHL}^{\dagger}	START \downarrow	RAS	$R_L = 667\ \Omega$ to V_{CC}	NORMAL READ		8	15	ns
t_{PLH}^{\dagger}	START \uparrow	RAS			290	363	435	ns
t_{PHL}^{\ddagger}	START \downarrow	CAS			100	126	150	ns
t_{PLH}^{\ddagger}	START \uparrow	CAS			275	342	410	ns
t_{PHL}^{\ddagger}	START \downarrow	R/W		NORMAL WRITE	90	113	135	ns
t_{PLH}^{\ddagger}	START \uparrow	R/W	303		383	460	ns	
t_{PLH}^{\dagger}	CAS HOLD \downarrow	CAS	$R_L = 2\text{ k}\Omega$ to V_{CC}	NORMAL READ		10	15	ns
t_{PHL}^{\ddagger}	START \downarrow	ROW/COL			75	100	125	ns
t_{PLH}^{\S}	START \uparrow	ROW/COL			485	609	730	ns
t_{PHL}^{\dagger}	R/W \downarrow	R/W	$R_L = 667\ \Omega$ to V_{CC}	NORMAL RMW		13	20	ns
t_{PLH}^{\dagger}	ROW/COL \downarrow	R/W			10	15	ns	
t_{PLH}^{\dagger}	RMW \uparrow	CAS			34	50	ns	
t_{PLH}^{\P}	RMW \downarrow	ROW/COL			240	300	360	ns
t_{PZH}^{\dagger}	RAS EN \downarrow	RAS	$R_L = 667\ \Omega$ to GND	NORMAL READ		13	20	ns
t_{PZL}^{\dagger}	RAS EN \downarrow	RAS	$R_L = 667\ \Omega$ to V_{CC}		14	25	ns	
t_{PHZ}^{\dagger}	RAS EN \uparrow	RAS	$R_L = 667\ \Omega$ to GND		7	15	ns	
t_{PLZ}^{\dagger}	RAS EN \uparrow	RAS	$R_L = 667\ \Omega$ to V_{CC}		16	25	ns	

\dagger Depends on RC network at pin 12 (2 k Ω , 180 pF used for testing) and the RC network at pin 15 (5 k Ω , 180 pF).

\ddagger Depends on RC network at pin 12 (2 k Ω , 180 pF).

\S Depends on RC networks at pin 12 (2 k Ω , 180 pF), pin 15 (5 k Ω , 180 pF), and pin 1 (5 k Ω , 180 pF).

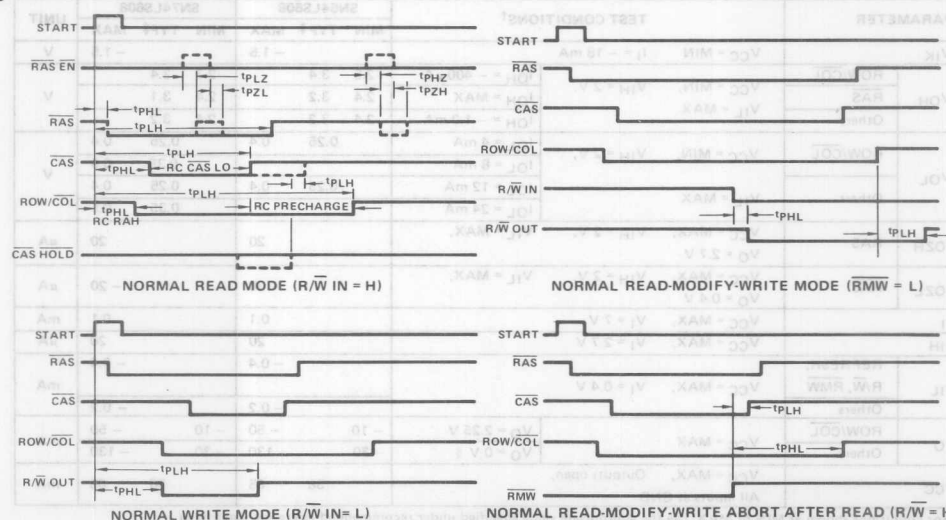
\P Depends on RC network at pin 1 (5 k Ω , 180 pF).

NOTE 2: Measurement point for all t_{PHZ} output pulses is 2.9 V. Measurement point for all t_{PLZ} output pulses is 0.8 V. All other measurement points are 1.3 V.

3

TTL DEVICES

PARAMETER MEASUREMENT INFORMATION



TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

D2549, JANUARY 1981 — REVISED DECEMBER 1983

(TIM99610 THRU TIM99613)

SN54LS'...JD PACKAGE

SN74LS'...JD OR N PACKAGE

(TOP VIEW)

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS 9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

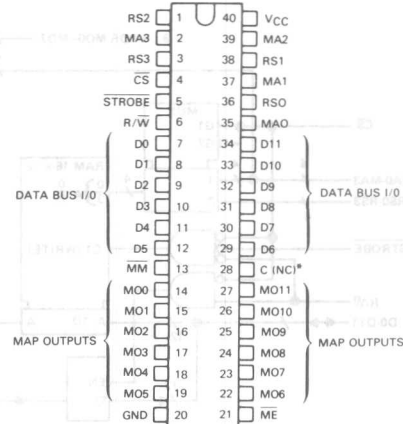
description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see the figure below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

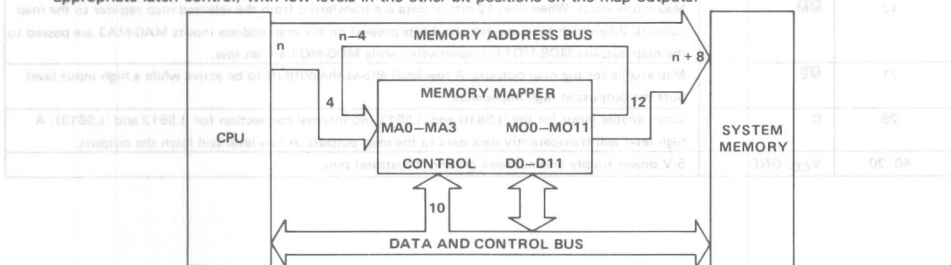
This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU.)

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/W whenever chip select (\overline{CS}) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when \overline{CS} is high and MM (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When \overline{CS} and MM are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8-MO11, respectively (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.



*Note: Pin 28 has no internal connection on 'LS612 and 'LS613.

For chip carrier information, contact the factory.



PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

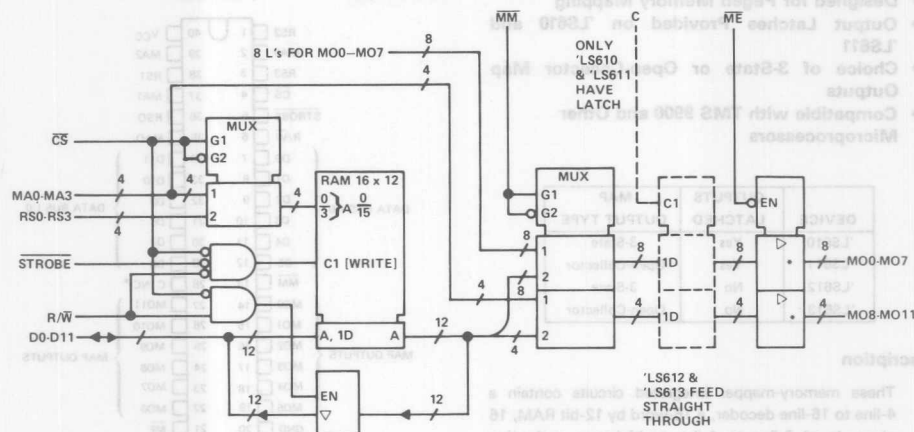
3-1035

3

TTL DEVICES

TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

functional block diagram (positive logic)



*'LS610 and 'LS612 have 3-state (V) map outputs.
'LS611 and 'LS613 have open-collector (Q) map outputs.

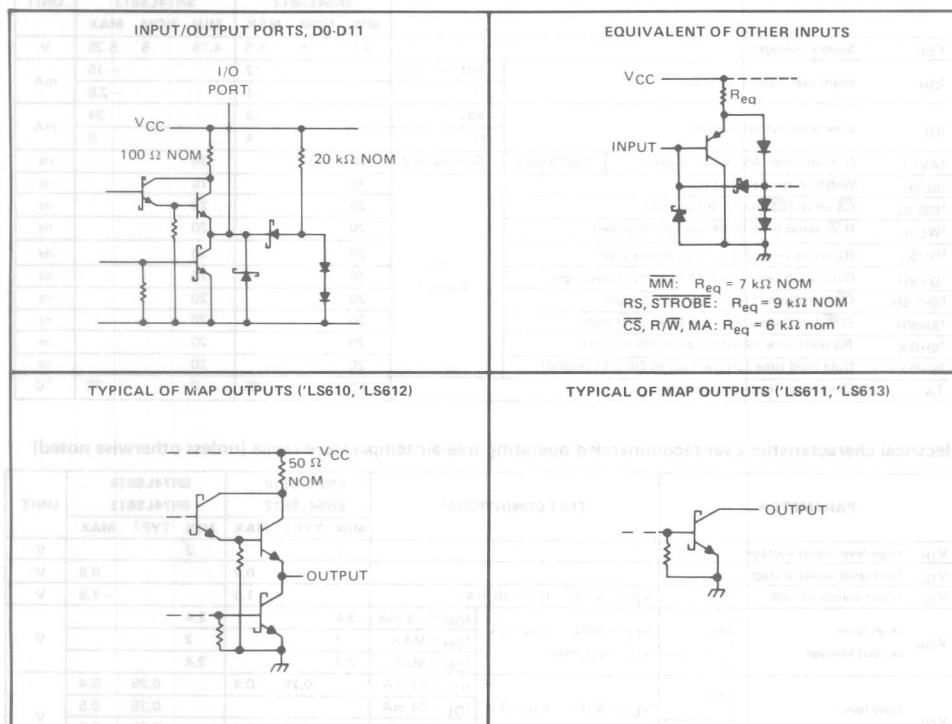
PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7-12, 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when CS is low. Mode controlled by R/W.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/W	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	STROBE	Strobe input used to enter data into the selected map register during I/O operations.
4	CS	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode (MM low and CS high).
14-19, 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
13	MM	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	ME	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V _{CC} , GND	5-V power supply and network ground (substrate) pins.

3
TTL DEVICES

TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage:	5.5 V
Data Bus I/O	
All other inputs	7 V
Operating free-air temperature range: SN54LS610 through SN54LS613	-55°C to 125°C
SN74LS610 through SN74LS613	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

recommended operating conditions

				SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current		MO			-12			-15	mA
			D			-1			-2.6	
I _{OL}	Low-level output current		MO			12			24	mA
			D			4			8	
t _{AVCL}	C setup time (AV before C low)	'LS610 only	See Figure 2	30			30			ns
t _{SLSH}	Width of strobe input pulse			75			75			ns
t _{CSLSL}	CS setup (CS low to strobe low)			20			20			ns
t _{WLSL}	R/W setup time (R/W low to strobe low)			20			20			ns
t _{RVSL}	RS setup time (RS valid to strobe low)			20			20			ns
t _{DVSH}	Data setup time (D0-D11 valid to strobe high)			75			75			ns
t _{SHCSH}	CS hold time (Strobe high to CS high)			20			20			ns
t _{SHWH}	R/W hold time (Strobe high to R/W high)			20			20			ns
t _{SHRX}	RS hold time (Strobe high to RS invalid)			20			20			ns
t _{SHDX}	Data hold time (Strobe high to D0-D11 invalid)			20			20			ns
T _A	Operating free-air temperature			-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	MO	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -3 mA	2.4			2.4			V
			I _{OH} = MAX	2			2			
		D	V _{IH} = V _{IL} max, I _{OH} = MAX	2.4			2.4			
V _{OL}	Low-level output voltage	MO	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 12 mA	0.25	0.4		0.25	0.4		V
			I _{OL} = 24 mA				0.35	0.5		
		D	V _{IH} = V _{IL} max, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		
			I _{OL} = 8 mA				0.35	0.5		
I _{OZH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _O = 2.7 V			20			20	μA
I _{OZL}	Off-state output current, low-level voltage applied	MO	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _O = 0.4 V			-20			-20	μA
		D				-400			-400	
I _I	Input current at maximum input voltage	D	V _I = 5.5 V			100			100	μA
		All others	V _I = 7 V			100			100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS}	Short-circuit output current§	MO	V _{CC} = MAX	-40		-225	-40		-225	mA
		D		-30		-130	-30		-130	
I _{CC}	Supply current		V _{CC} = MAX							mA
			Outputs high	112	180		112	180		
			Outputs low	112	180		112	180		
			Outputs at high impedance	150	230		180	230		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

3

TTL DEVICES

TYPES SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$ to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV} Access (enable) time	\overline{CS}	D 0-11	$R_L = 2\text{ k}\Omega$ See Figure 1, See Notes 3 and 4	28	50		26	50		ns
t_{WHDV} Access (enable) time	R/\overline{W}	D 0-11		20	35		20	35		ns
t_{RVDV} Access time	RS	D 0-11		49	75		39	75		ns
t_{WLDZ} Disable time	R/\overline{W}	D 0-11		32	50		30	50		ns
t_{CSHDZ} Disable time	\overline{CS}	D 0-11	$R_L = 667\ \Omega$, See Figure 2, See Notes 3 and 4	42	65		38	65		ns
t_{ELQV} Access (enable) time	\overline{ME}	MO 0-11		19	30		17	30		ns
t_{CSHQV} Access time	\overline{CS}	MO 0-11		56	85		48	85		ns
t_{MLQV} Access time	\overline{MM}	MO 0-11		25	40		22	40		ns
t_{CHQV} Access time	\overline{C}	MO 0-11		24	40					ns
t_{AVQV1} Access time (MM low)	MA	MO 0-11		46	70		39	70		ns
t_{MHQV} Access time	\overline{MM}	MO 0-11		24	40		22	40		ns
t_{AVQV2} Propagation time (MM high)	MA	MO 8-11		19	30		13	30		ns
t_{EHQZ} Disable time	\overline{ME}	MO 0-11		14	25		14	25		ns

NOTE: 3. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL} . Disable times are tested as t_{PHZ} and t_{PLZ} .
4. See General Information Section for load circuits and voltage waveforms.

explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

where: t_{AB-CD}
subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C SUBSCRIPT
C	C
\overline{CS}	\overline{CS}
D0-11	D
MA0-MA3	A
MO0-MO11	Q
\overline{ME}	E
\overline{MM}	M
R/\overline{W}	W
RS0-RS3	R
STROBE	S

3

TTL DEVICES

TYPES SN54LS611, SN54LS613, SN74LS611, SN74LS613 **MEMORY MAPPERS WITH OPEN-COLLECTOR MAP OUTPUTS**

recommended operating conditions

				SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V _{OH}	High-level output voltage	MO				5.5			5.5	V
I _{OH}	High-level output current	D				-1			-2.6	mA
I _{OL}	Low-level output current	MO				12			24	mA
		D				4			8	mA
t _{AVCL}	C setup time (AV before C low)	'LS611 only	See Figure 2	30			30			ns
t _{SLSH}	Width of strobe input pulse			75			75			ns
t _{CSLSL}	CS setup time (CS low to strobe low)			20			20			ns
t _{WLSL}	R/W setup time (R/W low to strobe low)			20			20			ns
t _{RVSL}	RS setup time (RS valid to strobe low)			20			20			ns
t _{DVSH}	Data setup time (D0-D11 valid to strobe high)		See Figure 1	75			75			ns
t _{SHCSH}	CS hold time (Strobe high to CS high)			20			20			ns
t _{SHWH}	R/W hold time (Strobe high to R/W high)			20			20			ns
t _{SHRX}	RS hold time (Strobe high to RS invalid)			20			20			ns
t _{SHDX}	Data hold time (Strobe high to D0-D11 invalid)			20			20			ns
T _A	Operating free-air temperature			-55		125	0		70	°C

NOTE 2: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	D V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4			2.4			
I _{OH}	High-level output current	MO V _{CC} = MIN, V _{IH} = 2 V, V _{OH} = 5.5 V			100			100	μA
V _{OL}	Low-level output voltage	MO V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max							V
					I _{OL} = 12 mA			0.25	
					I _{OL} = 24 mA			0.35	
					I _{OL} = 4 mA			0.25	
					I _{OL} = 8 mA			0.35	
I _{OZH}	Off-state output current, high-level voltage applied	D V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _O = 2.7 V			20			20	μA
I _{OZL}	Off-state output current, low-level voltage applied	D V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-400			-400	
I _I	Input current at maximum input voltage	D V _{CC} = MAX V _I = 5.5 V			100			100	
		All others V _I = 7 V			100			100	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS}	Short-circuit output current‡	D V _{CC} = MAX	-30		-130	-30		-130	mA
I _{CC}	Supply current	V _{CC} = MAX Outputs high	100		170	100		170	mA
		Outputs low	100		170	100		170	
		Outputs at high impedance	110		200	110		200	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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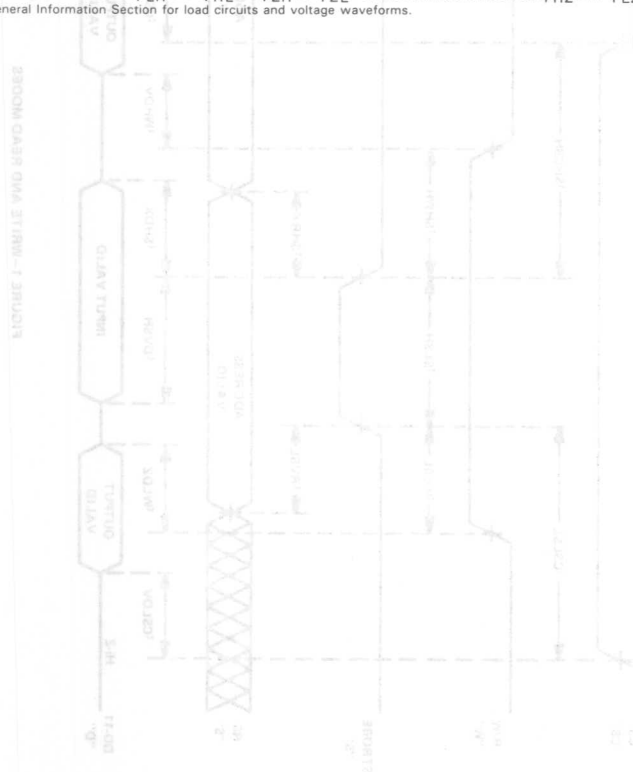
TTL DEVICES

TYPES SN54LS611, SN54LS613, SN74LS611, SN74LS613 MEMORY MAPPERS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$ to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS611			'LS613			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV} Access (enable) time	$\overline{CS}\downarrow$	D 0-11	$R_L = 2\text{ k}\Omega$, See Figure 1, See Notes 3 and 4		31	50		28	50	ns
t_{WHDV} Access (enable) time	R/W \uparrow	D 0-11			23	35		21	35	ns
t_{RVDV} Access time	RS	D 0-11			51	75		47	75	ns
t_{WLDZ} Disable time	R/W \downarrow	D 0-11			32	50		31	50	ns
t_{CSHDZ} Disable time	$\overline{CS}\uparrow$	D 0-11	$R_L = 667\text{ }\Omega$, See Figure 2, See Notes 3 and 4		41	65		40	65	ns
t_{ELQV} Access (enable) time	$\overline{ME}\downarrow$	MO 0-11			21	30		19	30	ns
t_{CSHQV} Access time	$\overline{CS}\uparrow$	MO 0-11			57	90		53	90	ns
t_{MLQV} Access time	MM \downarrow	MO 0-11			25	40		25	40	ns
t_{CHQV} Access time	CI \uparrow	MO 0-11			30	45				ns
t_{AVQV1} Access time (MM low)	MA	MO 0-11			47	70		44	70	ns
t_{MHQV} Access time	MM \uparrow	MO 0-11			31	50		31	50	ns
t_{AVQV2} Propagation time (MM high)	MA	MO 8-11			21	30		20	30	ns
t_{EHQZ} Disable time	$\overline{ME}\uparrow$	MO 0-11			15	25		15	25	ns

NOTE: 3. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL} . Disable times are tested as t_{PHZ} and t_{PLZ} .
4. See General Information Section for load circuits and voltage waveforms.



3

TTL DEVICES

MEMORY MAPPERS

Timing Diagrams

FIGURE 1—WRITE AND READ MODES

3

TTL DEVICES

TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613
MEMORY MAPPERS WITH OPEN-COLLECTOR OUTPUTS

TIMING DIAGRAMS

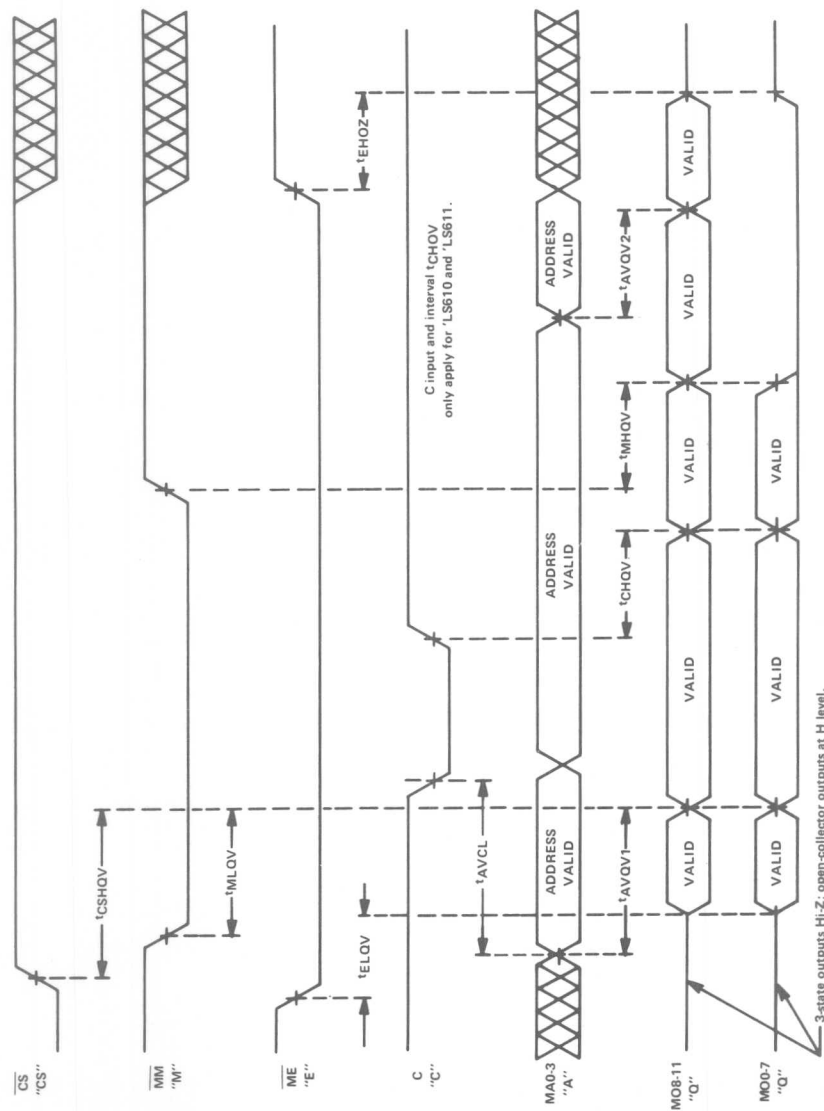
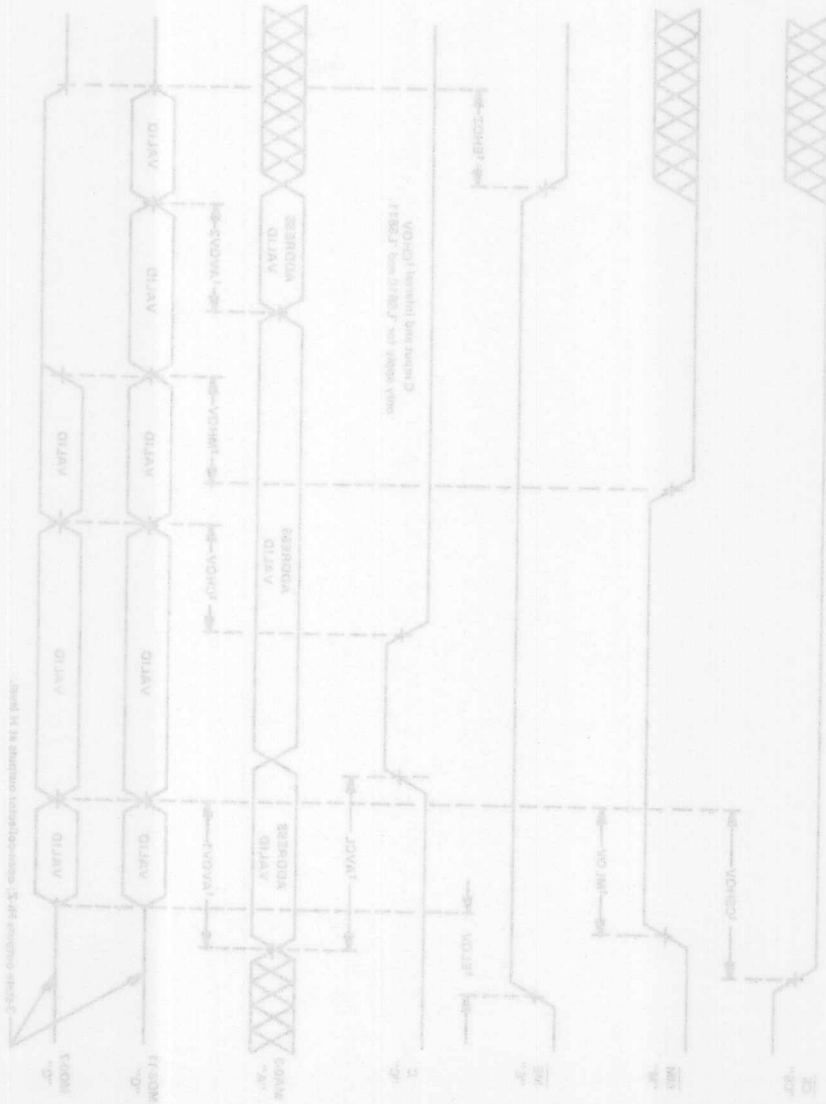


FIGURE 2—MAP AND PASS MODES

TTL DEVICES

3

TIMING DIAGRAMS



2370008 DATA DATA DATA DATA DATA DATA

Based on the data sheet specifications for the SN74LS810 through SN74LS813.

3 TTL DEVICES

TYPES SN54LS620 THRU SN54LS623, SN74LS620 THRU SN74LS623 OCTAL BUS TRANSCEIVERS

D2537, AUGUST 1979 — REVISED DECEMBER 1983

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'LS621	Open-Collector	True
'LS622	Open-Collector	Inverting
'LS623	3-State	True

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

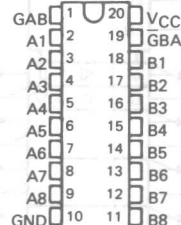
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\bar{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620 thru 'LS623 the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620 and 'LS622.

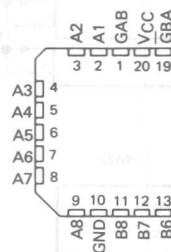
SN54LS620, SN54LS621, SN54LS622
SN54LS623 ... J PACKAGE
SN74LS620, SN74LS621, SN74LS622
SN74LS623 ... DW, J OR N PACKAGE

(TOP VIEW)



SN54LS620, SN54LS621, SN54LS622,
SN54LS623, SN74LS620, SN74LS621,
SN74LS622, SN74LS623 ... FK PACKAGE

(TOP VIEW)



FUNCTION TABLE

ENABLE	INPUTS	OPERATION
$\bar{G}BA$	GAB	'LS620, 'LS622
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus
		'LS621, 'LS623
		B data to A bus
		A data to B bus
		Isolation

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

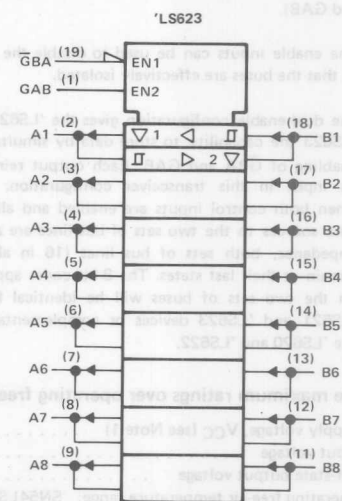
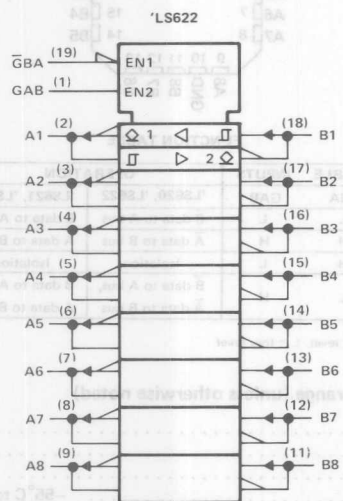
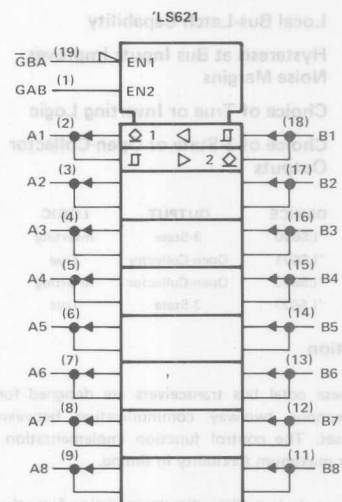
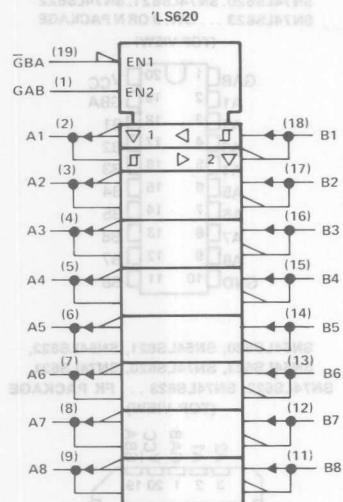
PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

TYPES SN54LS620 THRU SN54LS623, SN74LS620 THRU SN74LS623 OCTAL BUS TRANSCEIVERS

logic symbols



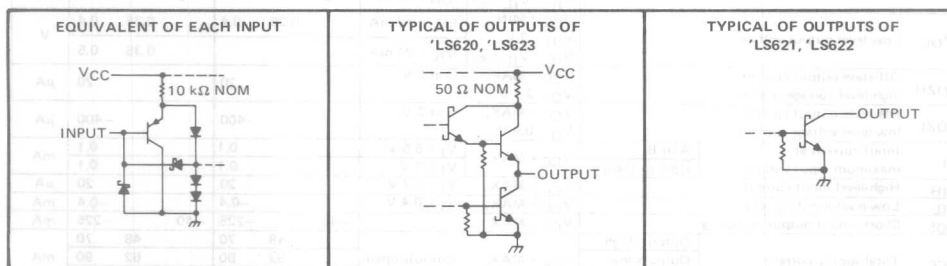
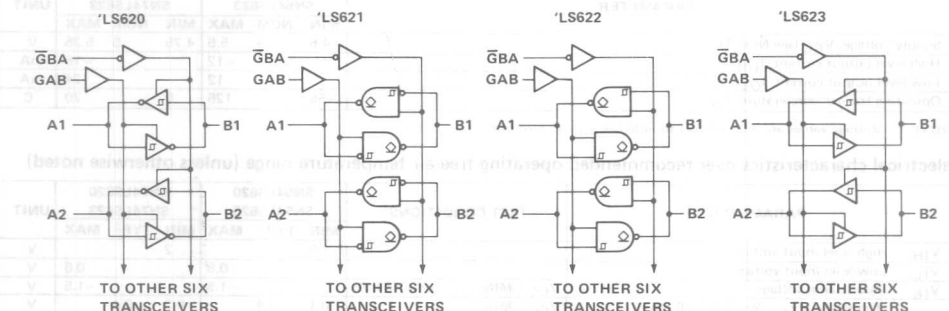
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPE:

recommended operating conditions



TYPES SN54LS620, SN54LS623, SN74LS620, SN74LS623

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

OCTAL BUS TRANSCEIVERS

recommended operating conditions

PARAMETER	SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.5			0.6	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$) A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	2.4	3.4		2.4	3.4		V
	$I_{OH} = -3 \text{ mA}$							
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	2			2			V
	$I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}, \bar{G} \text{ at } 2 \text{ V}$			20			20	μA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}, \bar{G} \text{ at } 2 \text{ V}$			-400			-400	μA
I_I Input current at maximum input voltage	A or B			0.1			0.1	mA
	GBA or GAB			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC} Total supply current	Outputs high		48	70		48	70	mA
	Outputs low		62	90		62	90	mA
	Outputs at Hi-Z		64	95		64	95	mA

[†] For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS620			'LS623			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$		6	10		8	15	ns
	B	A			6	10		8	15	ns
t_{PHL} Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
	B	A			8	15		11	15	ns
t_{PZL} Output enable time to low level	GBA	A	See Note 2		31	40		31	40	ns
	GAB	B			31	40		31	40	ns
t_{PZH} Output enable time to high level	GBA	A			23	40		26	40	ns
	GAB	B			23	40		26	40	ns
t_{PLZ} Output disable time from low level	GBA	A	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$		15	25		15	25	ns
	GAB	B			15	25		15	25	ns
t_{PHZ} Output disable time from high level	GBA	A			15	25		15	25	ns
	GAB	B			15	25		15	25	ns

t_{PLH} Propagation delay time, low-to-high-level output

t_{PHL} Propagation delay time, high-to-low-level output

t_{PZH} Output enable time to high level

NOTE 2: See General Information Section for load circuits and voltage waveforms.

t_{PZL} Output enable time to low level

t_{PHZ} Output disable time from high level

t_{PLZ} Output disable time from low level

3

TTL DEVICES

TYPES SN54LS621, SN54LS622, SN74LS621, SN74LS622 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.5			0.6			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$	100			100			µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5		
I_I	Input current at maximum input voltage	A or B $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ GBA or GAB $V_I = 7.0 \text{ V}$	0.1			0.1			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.4			-0.4			mA
I_{CC}	Total supply current	Outputs high	48	70		48	70		mA
		Outputs low	62	90		62	90		

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS621			'LS622			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	$C_L = 45 \text{ pF},$ $R_L = 667 \Omega,$	17	25		19	25		ns
		B	A		17	25		19	25		
t_{PHL}	Propagation delay time, high-to-low-level output	A	B		16	25		14	25		ns
		B	A		16	25		14	25		
t_{PLH}	Output disable time from low level	GBA	A	See Note 2	23	40		26	40		ns
		GAB	B		25	40		28	40		
t_{PHL}	Output enable time from high level	GBA	A		34	50		43	60		ns
		GAB	B		37	50		39	60		

t_{PLH} = Propagation delay time, low-to-high-level input.

t_{PHL} = Propagation delay time, high-to-low-level input.

NOTE 2: See General Information Section for load circuits and voltage waveforms.

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS SN74LS251, SN74LS252, SN74LS253, SN74LS254, SN74LS255

recommended operating conditions

PARAMETER	SN74LS251	SN74LS252	SN74LS253	SN74LS254	SN74LS255
Supply voltage, V_{CC} (see Note 1)	4.5	4.5	4.5	4.5	4.5
High-level output voltage, V_{OH}	2.4	2.4	2.4	2.4	2.4
Low-level output voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4
Low-level output current, I_{OL}	10	10	10	10	10
Operating free-air temperature, T_A	-55	-55	-55	-55	-55

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74LS251	SN74LS252	SN74LS253	SN74LS254	SN74LS255
V_{IH} High-level input voltage		2	2	2	2	2
V_{IL} Low-level input voltage		0.8	0.8	0.8	0.8	0.8
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN.}$, $I_I = -18 \text{ mA}$	-1.5	-1.5	-1.5	-1.5	-1.5
Hysteresis ($V_{H1} - V_{H2}$) at 1 A or 2 mA	$V_{CC} = \text{MIN.}$	0.1	0.4	0.3	0.4	0.4
High-level output current	$V_{CC} = \text{MIN.}$, $V_{OH} = 2.4 \text{ V}$, $V_{IH} = V_{IL} = \text{MAX.}$	100	100	100	100	100
Low-level output voltage	$V_{CC} = \text{MIN.}$, $V_{OH} = 2.4 \text{ V}$, $V_{IH} = V_{IL} = \text{MAX.}$	0.4	0.4	0.4	0.4	0.4
Input current at maximum input voltage	$V_{CC} = \text{MAX.}$, $V_I = 2.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$	0.1	0.1	0.1	0.1	0.1
High-level input current	$V_{CC} = \text{MAX.}$, $V_I = 2.4 \text{ V}$	20	20	20	20	20
Low-level input current	$V_{CC} = \text{MAX.}$, $V_I = 0.4 \text{ V}$	-0.4	-0.4	-0.4	-0.4	-0.4
Total supply current	$V_{CC} = \text{MAX.}$	48	48	48	48	48
Output low		65	65	65	65	65
Output high		65	65	65	65	65

For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
 All voltage values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN74LS251	SN74LS252	SN74LS253	SN74LS254	SN74LS255
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 50 \text{ pF}$	17	17	17	17	17
t_{PLH} Propagation delay time, high-to-low-level output	A	B		17	17	17	17	17
t_{PLH} Propagation delay time, low-to-high-level output	A	B		17	17	17	17	17
t_{PLH} Propagation delay time, high-to-low-level output	A	B		17	17	17	17	17
Output disable time	0	1	$R_L = 800 \Omega$	23	23	23	23	23
Output enable time	1	0		23	23	23	23	23
Output disable time	0	1		23	23	23	23	23
Output enable time	1	0		23	23	23	23	23

t_{PLH} = Propagation delay time, low-to-high-level output.
 t_{PLH} = Propagation delay time, high-to-low-level output.
 NOTE 2: See General Information Section for test circuits and voltage waveform.

3 TTL DEVICES

TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

D2501, JANUARY 1980 — REVISED DECEMBER 1983

- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges

DEVICE TYPE	SIMILAR TO	NUMBER VCO's	COMP'L Z OUT	ENABLE	RANGE INPUT	R _{ext}
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

description

These voltage-controlled oscillators (VCO's) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCO's in a single monolithic chip. The 'LS624, 'LS625, 'LS626 and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external capacitor in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

The 'LS628 offers more precise temperature compensation than its 'LS624 counterpart. The 'LS624 features a 600 ohm internal timing resistor. The 'LS628 requires a timing resistor to be connected externally across R_{ext} pins. Temperature compensation will be improved due to the temperature coefficient of the external resistor.

Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

A single 5-volt supply can be used; however, one set of supply voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set (OSC V_{CC} and OSC GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS626 and 'LS627 can be achieved by removing the appropriate OSC V_{CC}. An enable input is provided on the 'LS624, 'LS626, 'LS628, and 'LS629. When the enable input is low, the output is enabled; when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627 and 'LS629) when both VCO's are operated simultaneously.

The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS624 thru SN74LS629 are characterized for operation from 0°C to 70°C.

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TTL DEVICES

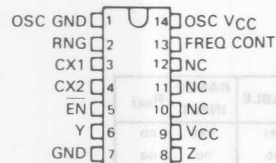
PRODUCTION DATA

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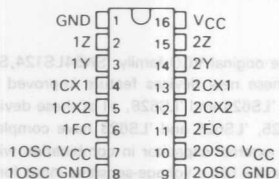


TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

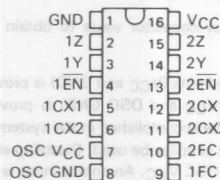
SN54LS624 ... J OR W PACKAGE
SN74LS624 ... D, J OR W PACKAGE
(TOP VIEW)



SN54LS625 ... J OR W PACKAGE
SN74LS625 ... D, J OR N PACKAGE
(TOP VIEW)

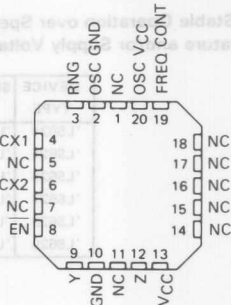


SN54LS626 ... J OR W PACKAGE
SN74LS626 ... D, J OR N PACKAGE
(TOP VIEW)

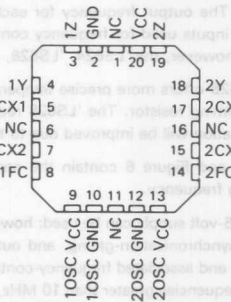


NC No internal connection

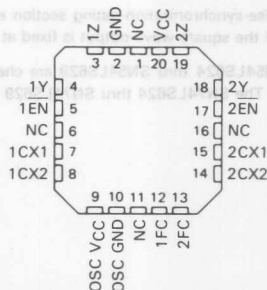
SN54LS624 ... FK PACKAGE
SN74LS624
(TOP VIEW)



SN54LS625 ... FK PACKAGE
SN74LS625
(TOP VIEW)



SN54LS626 ... FK PACKAGE
SN74LS626
(TOP VIEW)

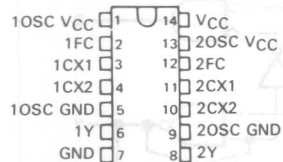


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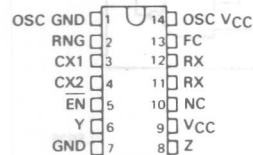
TTL DEVICES

TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

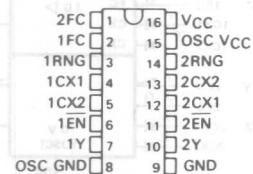
SN54LS627 ... J OR W PACKAGE
SN74LS627 ... D, J OR N PACKAGE
(TOP VIEW)



SN54LS628 ... J OR W PACKAGE
SN74LS628 ... D, J OR N PACKAGE
(TOP VIEW)

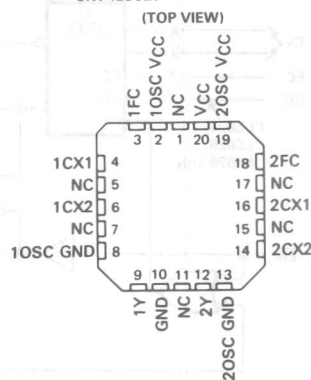


SN54LS629 ... J OR W PACKAGE
SN74LS629 ... D, J OR N PACKAGE
(TOP VIEW)

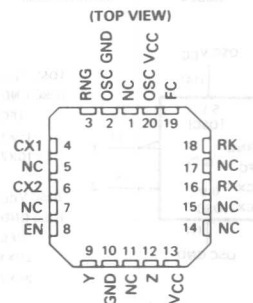


NC-No internal connection

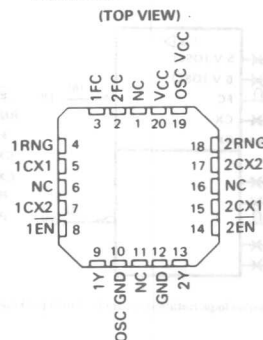
SN54LS627 ... FK PACKAGE
SN74LS627



SN54LS628 ... FK PACKAGE
SN74LS628



SN54LS629 ... FK PACKAGE
SN74LS629



3

TTL DEVICES

3 TTL DEVICES

3 TTL DEVICES



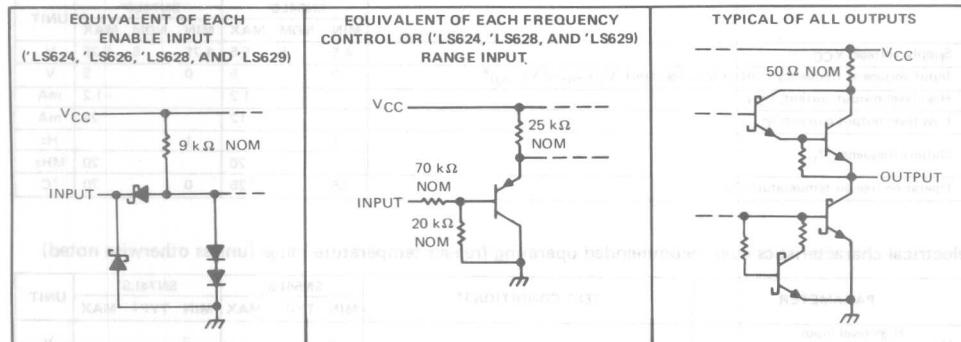
3 TTL DEVICES



3 TTL DEVICES

TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2)	7 V
Input voltage: Enable input [†]	7 V
Frequency control or range input [‡]	V_{CC}
Operating free-air temperature range: SN54LS [†] Circuits	-55°C to 125°C
SN74LS [†] Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] The enable input is provided only on the [†]LS624, [†]LS626, [†]LS628, and [†]LS629.

[‡] The range input is provided only on [†]LS624, [†]LS628, and [†]LS629.

NOTE: 1. Voltage values are with respect to the appropriate ground terminal.
2. Throughout the data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and OSC V_{CC} terminals, unless otherwise noted.

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

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TTL DEVICES

**TYPES SN54LS624 THRU SN54LS629,
SN74LS624 THRU SN74LS629
VOLTAGE-CONTROLLED OSCILLATORS**

recommended operating conditions

	SN54LS ¹			SN74LS ¹			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$ ²	0		5	0		5	V
High-level output current, I_{OH}			-1.2			-1.2	mA
Low-level output current, I_{OL}			12			24	mA
Output frequency, f_o	1			1			Hz
		20			20		MHz
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ¹	SN54LS ¹			SN74LS ¹			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V_{IH}	High-level input voltage at enable ³		2			2			V
V_{IL}	Low-level input voltage at enable ³				0.7			0.8	V
V_{IK}	Input clamp voltage at enable ³	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -1.2 \text{ mA}$, EN at V_{IL} max, See Note 3	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 12 \text{ mA}$, EN at V_{IL} max, See Note 3		0.25	0.4		0.25	0.4	V
							0.35	0.5	
I_I	Input current	Freq control or range ⁴ $V_{CC} = \text{MAX}$							μA
				50	250		50	250	
				10	50		10	50	
I_I	Input current at maximum input voltage	Enable ³ $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.2			0.2	mA
I_{IH}	High-level input current	Enable ³ $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			40			40	μA
I_{IL}	Low-level input current	Enable ³ $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.8			-0.8	mA
I_{OS}	Short-circuit output current ⁵	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC}	Supply current, total into V_{CC} and OSC V_{CC} pins	$V_{CC} = \text{MAX},$ Enable ³ = 4.5 V See Note 4	'LS624	20	35	20	35		mA
			'LS625	35	55	35	55		
			'LS626	35	55	35	55		
			'LS627	35	55	35	55		
			'LS628	20	35	20	35		
			'LS629	35	55	35	55		

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

² All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

³ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

⁴ The range input is provided only on the 'LS624, 'LS628, and 'LS629.

⁵ The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTES: 3. V_{OH} for Y outputs and V_{OL} for Z outputs are measured while enable inputs are at V_{IL} MAX, with individual 1-kΩ resistors connected from CX1 to V_{CC} and from CX2 to ground. The resistor connections are reversed for testing V_{OH} for Z outputs and V_{OL} for Y inputs.

4. For 'LS624, 'LS626, 'LS628, and 'LS629, I_{CC} is measured with the outputs disabled and open. For 'LS625 and 'LS627, I_{CC} is measured with one OSC $V_{CC} = \text{MAX}$, and with the other OSC V_{CC} and outputs open.

TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

switching characteristics, $V_{CC} = 5\text{ V}$ (unless otherwise noted), $R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	'LS624, 'LS628, 'LS629			'LS625, 'LS626, 'LS627			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
f _O Output frequency	C _{ext} = 50 pF	V _I (freq) = 5 V, V _I (rng) = 0 V			15	20	25	MHz	
		V _I (freq) = 1 V, V _I (rng) = 5 V			1.1	1.6	2.1		
		V _I (freq) = 5 V				7	9.5		12
		V _I (freq) = 0 V				0.9	1.2		1.5

TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY

vs

FREQUENCY-CONTROL INPUT VOLTAGE†

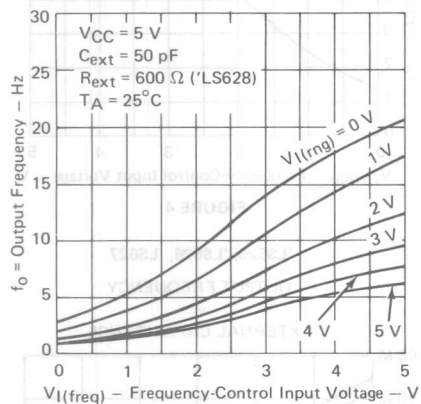


FIGURE 1

† Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY

vs

FREQUENCY-CONTROL INPUT VOLTAGE†

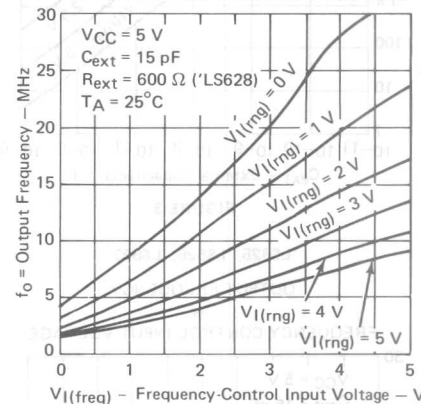


FIGURE 2

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TTL DEVICES

**TYPES SN54LS624 THRU SN54LS629,
SN74LS624 THRU SN74LS629
VOLTAGE-CONTROLLED OSCILLATORS**

TYPICAL CHARACTERISTICS

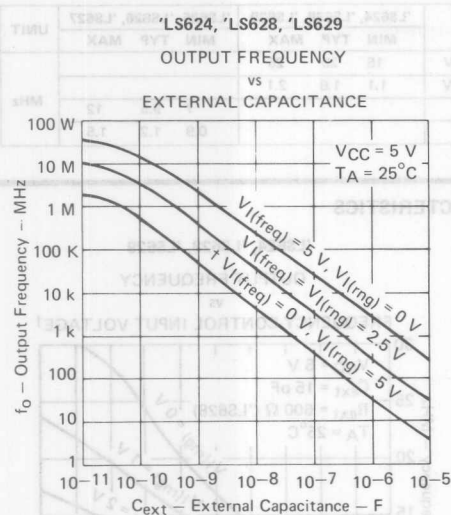


FIGURE 3

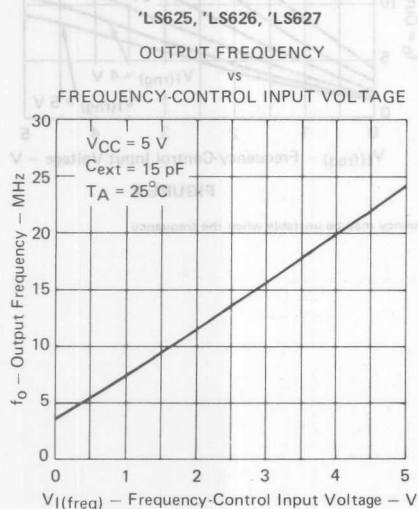


FIGURE 5

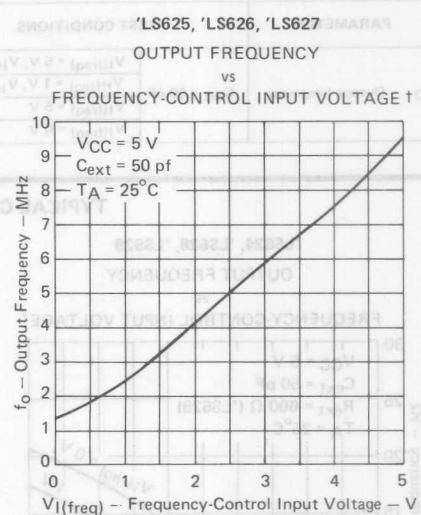


FIGURE 4

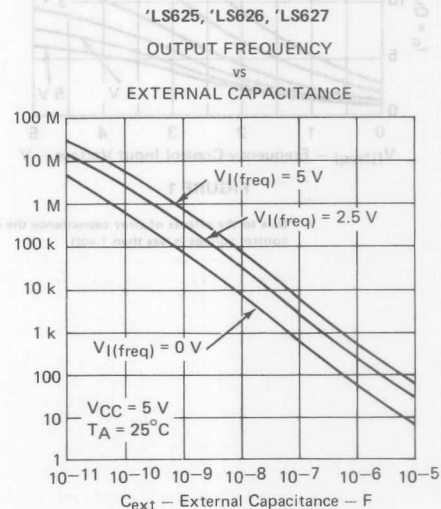


FIGURE 6

[†] Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

TYPES SN54LS624 THRU SN54LS629,
SN74LS624 THRU SN74LS629
VOLTAGE-CONTROLLED OSCILLATORS

TYPICAL CHARACTERISTICS

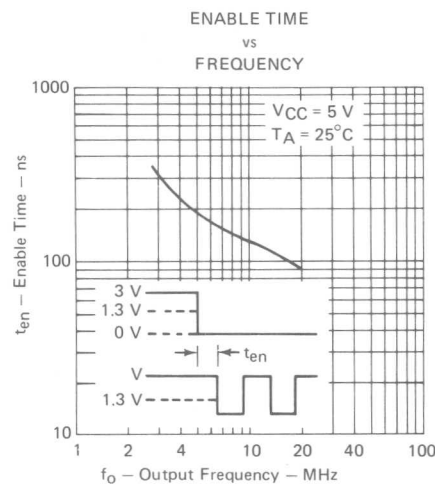
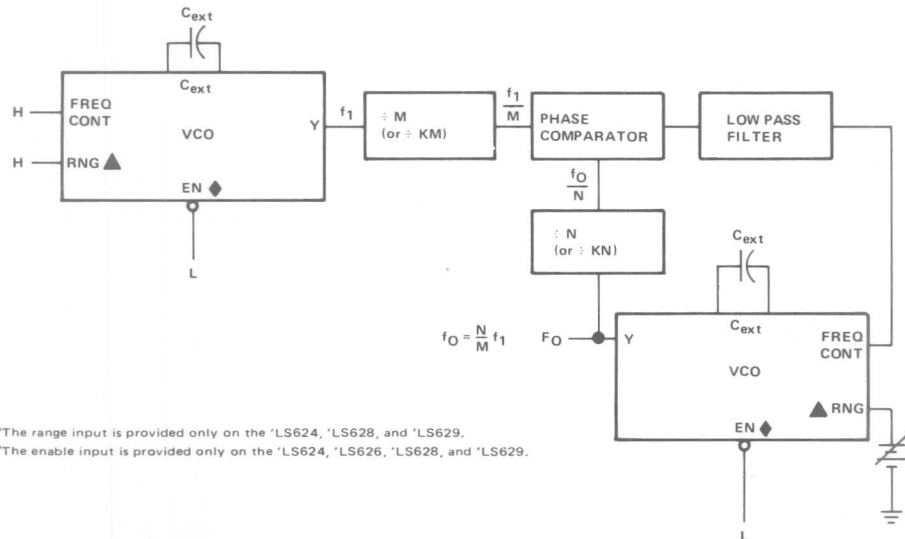


FIGURE 7

TYPICAL APPLICATIONS DATA



*The range input is provided only on the 'LS624, 'LS628, and 'LS629.

*The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

FIGURE A—PHASE-LOCKED LOOP

TYPICAL CHARACTERISTICS

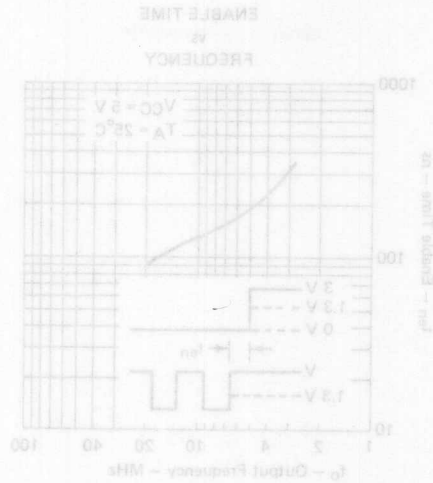


FIGURE 7

TYPICAL APPLICATIONS DATA

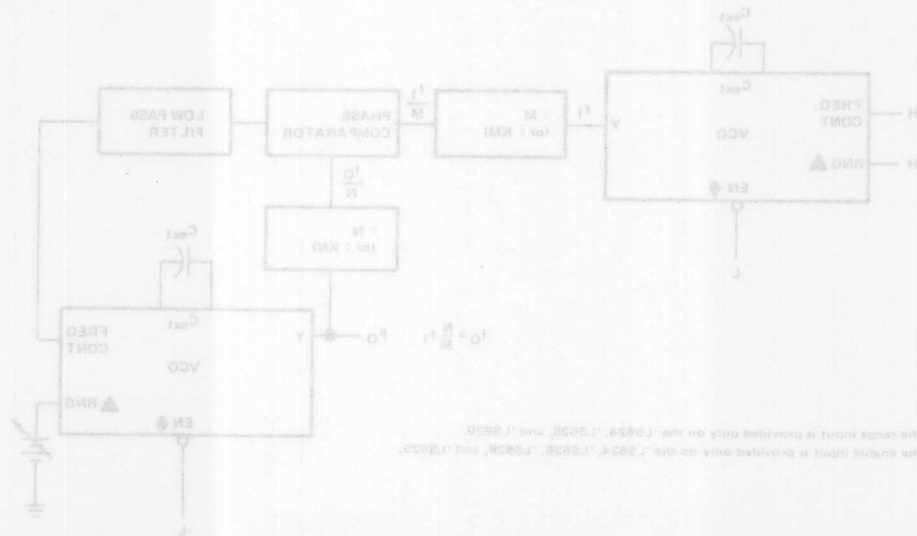


FIGURE 8—PHASE-LOCKED LOOP

3 TTL DEVICES

TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2550, MARCH 1980 – REVISED APRIL 1985

(TIM99630, TIM99631)

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Fast Processing Times:
 - Write Cycle: Generates Check Word in 45 ns Typical
 - Read Cycle: Flags Errors in 27 ns Typical
- Power Dissipation 600 mW Typical
- Choice of Output Configurations:
 - 'LS630 . . . 3-State
 - 'LS631 . . . Open-Collector

description

The 'LS630 and 'LS631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

CONTROL FUNCTION TABLE

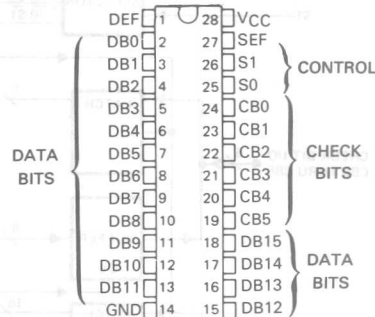
Memory Cycle	Control		EDAC Function	Data I/O	Check Word I/O	Error Flags	
	S1	S0				SEF	DEF
WRITE	L	L	Generate Check Word	Input Data	Output Check Word	L	L
READ	L	H	Read Data & Check Word	Input Data	Input Check Word	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Check Word	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

PRODUCTION DATA

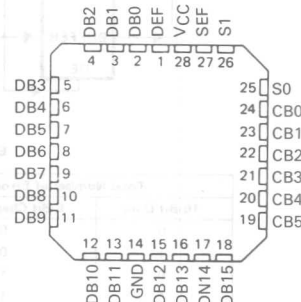
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN54LS630, SN54LS631 . . . JD PACKAGE
SN74LS630, SN74LS631 . . . JD OR N PACKAGE
(TOP VIEW)



SN54LS630, SN54LS631 . . . FK PACKAGE
SN74LS630, SN74LS631
(TOP VIEW)

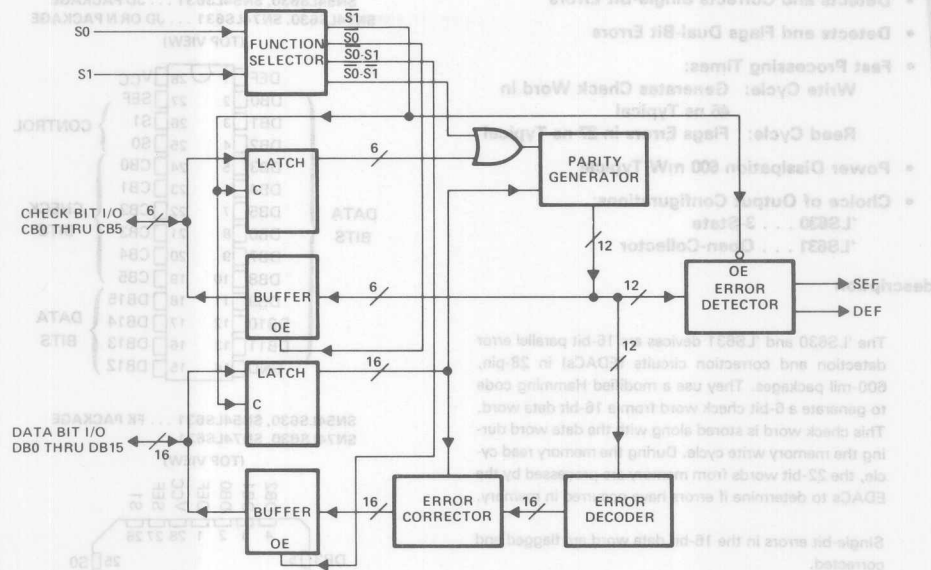


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TTL DEVICES

TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

functional block diagram



ERROR FUNCTION TABLE

Total Number of Errors		Error Flags		Data Correction
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

error detection and correction details

During a memory write cycle, six check bits (CB0-CB5) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

CHECKWORD		16-BIT DATA WORD															
BIT		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0		x	x		x	x				x	x	x			x		
CB1		x		x	x		x	x		x		x		x		x	
CB2			x	x		x	x		x		x		x		x		x
CB3		x	x	x				x	x			x	x	x			
CB4					x	x	x	x							x	x	x
CB5										x	x	x	x	x	x	x	x

The six check bits are parity bits derived from the matrix of data bits as indicated by "x" for each bit.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly three bits of the 6-bit check word. Any single error in the 6-bit check word changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

ERROR SYNDROME TABLE

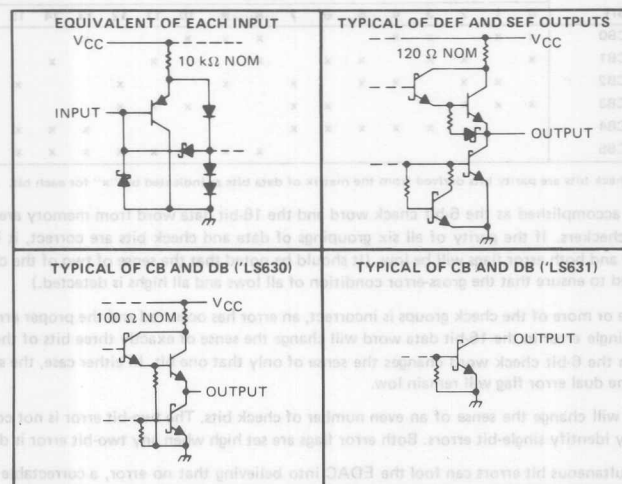
ERROR LOCATION	SYNDROME ERROR CODE					
	CB0	CB1	CB2	CB3	CB4	CB5
DB0	L	L	H	L	H	H
DB1	L	H	L	L	H	H
DB2	H	L	L	L	H	H
DB3	L	L	H	H	L	H
DB4	L	H	L	H	L	H
DB5	H	L	L	H	L	H
DB6	H	L	H	L	L	H
DB7	H	H	L	L	L	H
DB8	L	L	H	H	H	L
DB9	L	H	L	H	H	L
DB10	L	H	H	L	H	L
DB11	H	L	H	L	H	L
DB12	H	H	L	L	H	L
DB13	L	H	H	H	L	L
DB14	H	L	H	H	L	L
DB15	H	H	L	H	L	L
CB0	L	H	H	H	H	H
CB1	H	L	H	H	H	H
CB2	H	H	L	H	H	H
CB3	H	H	H	L	H	H
CB4	H	H	H	H	L	H
CB5	H	H	H	H	H	L
NO ERROR	H	H	H	H	H	H

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TTL DEVICES

TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631 **16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS**

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: S0 and S1	7 V
CB and DB	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS630, SN54LS631	-55°C to 125°C
SN74LS630, SN74LS631	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS630			SN74LS630			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current	CB or DB, 'LS630 only			-1			-1	mA
		DEF or SEF			-0.4			-0.4	
V _{OH}	High-level output voltage	CB or DB, 'LS631 only			5.5			5.5	V
I _{OL}	Low-level output current	CB or DB			12			24	mA
		DEF or SEF			4			8	
t _{su}	Setup time	CB or DB before S1††	15			15			ns
		CB or DB before S1††	45			45			
t _h	Hold time	CB or DB after S1†	15			15			ns
T _A	Operating free-air temperature		-55		125	0		70	°C

† This time guarantees the input data and checkword will be latched for generating a checkword and read data only.

† This time guarantees the input data and checkword will be latched plus that no glitch will occur on SEF or DEF flags.

† The upward-pointing arrow indicates a transition from low to high.

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TTL DEVICES

TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS †	SN54LS630			SN74LS630			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage			0.7			0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	High-level output voltage	CB or DB	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = MAX		2.4	3.3	2.4	3.2	V
		DEF or SEF	V _{IL} = V _{IL} min, I _{OH} = -400 µA		2.5	3.4	2.7	3.4	
V _{OL}	Low-level output voltage	CB or DB	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA				0.35	0.5	
		DEF or SEF	V _{IL} = V _{IL} max, I _{OL} = 4 mA		0.25	0.4	0.25	0.4	
			I _{OL} = 8 mA				0.35	0.5	
I _{OZH}	Off-state output current, high-level voltage applied	CB or DB	V _{CC} = MAX, S ₀ and S ₁ at 2 V, V _O = 2.7 V,		20		20		µA
I _{OZL}	Off-state output current, low-level voltage applied	CB or DB	V _{CC} = MAX, S ₀ and S ₁ at 2 V, V _O = 0.4 V,		-200		-200		µA
I _I	Input current at maximum input voltage	CB or DB	V _{CC} = MAX, V _I = 5.5 V		0.1		0.1		mA
		S ₀ or S ₁	V _{IH} = 4.5 V, V _I = 7 V		0.1		0.1		
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V		20		20		µA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V		-0.2		-0.2		mA
I _{OS} §	Short-circuit output current	CB or DB	V _{CC} = MAX		-30	-130	-30	-130	mA
		DEF or SEF			-20	-100	-20	-100	
I _{CC}	Supply current		V _{CC} = MAX, S ₀ and S ₁ at 4.5 V, All CB and DB pins grounded, DEF and SEF open		143	230	143	230	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54LS631			SN74LS631			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage			0.7			0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	High-level output voltage	DEF or SEF	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -400 µA, V _{IL} = V _{IL} max		2.5	3.4	2.7	3.4	V
I _{OH}	High-level output current	CB or DB	V _{CC} = MIN, V _{IH} = 2 V, V _{OL} = 5.5 V, V _{IL} = V _{IL} max		100		100		µA
V _{OL}	Low-level output voltage	CB or DB	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA				0.35	0.5	
		DEF or SEF	V _{IL} = V _{IL} max, I _{OL} = 4 mA		0.25	0.4	0.25	0.4	
			I _{OL} = 8 mA				0.35	0.5	
I _I	Input current at maximum input voltage	CB or DB	V _{CC} = MAX, V _I = 5.5 V		0.1		0.1		mA
		S ₀ or S ₁	V _{IH} = 4.5 V, V _I = 7 V		0.1		0.1		
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V		20		20		µA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V		-0.2		-0.2		mA
I _{OS} §	Short-circuit output current	DEF or SEF	V _{CC} = MAX		-20	-100	-20	-100	mA
I _{CC}	Supply current		V _{CC} = MAX, S ₀ and S ₁ at 4.5 V, All CB and DB grounded, SEF and DEF open		113	180	113	180	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

TYPES SN54LS630, SN54LS631, SN74LS630, AND SN74LS631 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS630			UNIT
				MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output [◇]	DB	CB	S0 at 0 V, S1 at 0 V, $R_L = 667\ \Omega$, See Figure 1	31	65		ns
t_{PHL} Propagation delay time, high-to-low-level output [◇]				45	65		ns
t_{PLH} Propagation delay time, low-to-high-level output [*]	S1↑	DEF	S0 at 3 V, $R_L = 2\text{ k}\Omega$, See Figure 1	27	40		ns
		SEF		20	30		ns
t_{PZH} Output enable time to high level [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 2	24	40		ns
t_{PZL} Output enable time to low level [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 1	30	45		ns
t_{PHZ} Output disable time from high level [▲]	S0↑	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 2	43	65		ns
t_{PLZ} Output disable time from low level [▲]	S0↑	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 1	31	65		ns

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$, see Figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS631			UNIT
				MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high level output [◇]	DB	CB	S0 at 0 V, S1 at 0 V, $R_L = 667\ \Omega$	38	55		ns
t_{PHL} Propagation delay time, high-to-low-level output [◇]				45	65		ns
t_{PLH} Propagation delay time, low-to-high-level output [*]	S1↑	DEF	S0 at 3 V, $R_L = 2\text{ k}\Omega$	27	40		ns
		SEF		20	30		ns
t_{PHL} Propagation delay time, high-to-low-level output [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$	28	45		ns
t_{PLH} Propagation delay time, low-to-high-level output [▲]	S0↑	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$	33	50		ns

3

TTL DEVICES

These parameters describe the time intervals taken to generate the check word during the memory write cycle.
^{*}These parameters describe the time intervals taken to flag errors during the memory read cycle.
[#]These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
[▲]These parameters describe the time intervals taken to disable the CB and DB buses in preparation for a new data word during the memory read cycle.

PARAMETER MEASUREMENT INFORMATION

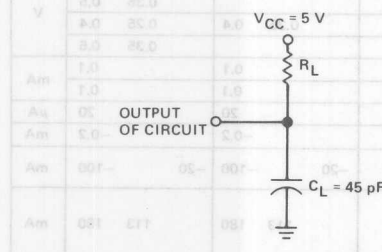


FIGURE 1—OUTPUT LOAD CIRCUIT

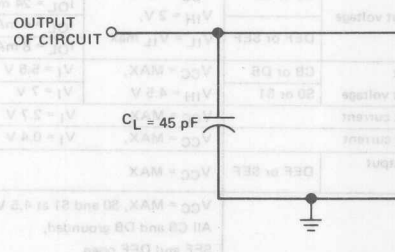
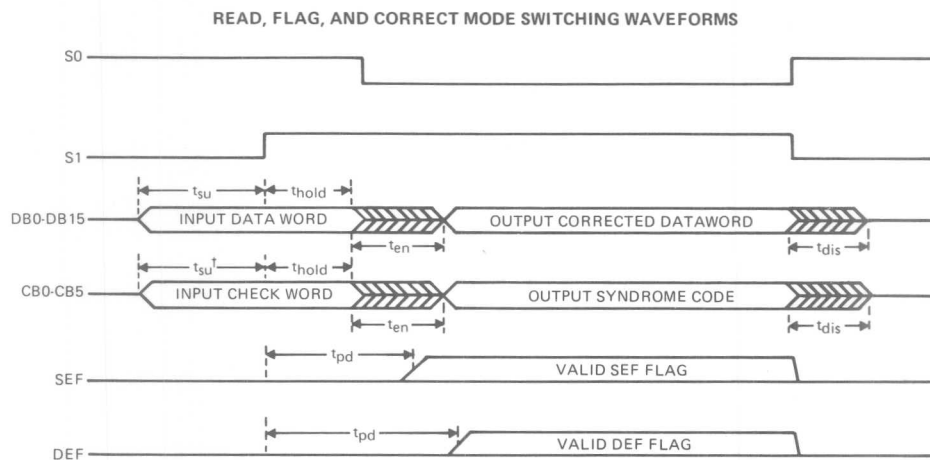


FIGURE 2—OUTPUT LOAD CIRCUIT

TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

typical operating sequences



† NOTE: There are two conditions specified for t_{su} of Data or Checkword before $S1$ † See recommended operating conditions for details.

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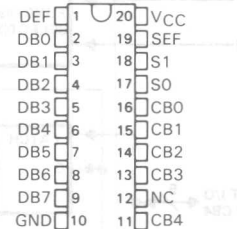
TTL DEVICES

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637 8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

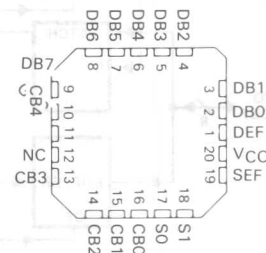
D2728, APRIL 1983, REVISED DECEMBER 1983

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Fast Processing Times:
Write Cycle: Generates Check Word in
45 ns Typical
Read Cycle: Flags Errors in 27 ns
Typical
- Power Dissipation 500 mW Typical
- Choice of Output Configurations:
'LS636 . . . 3-State
'LS637 . . . Open Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
SN74LS' . . . (TOP VIEW)



NC No internal connection.

description

The 'LS636 and 'LS637 devices are 8-bit parallel error detection and correction circuits (EDACs) in 20-pin, 300-mil packages. They use a modified Hamming code to generate a 5-bit check word from an 8-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 13-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 8-bit data word are flagged and corrected.

Single-bit errors in the 5-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 8-bit word is not in error. The correction cycle will simply pass along the original 8-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 13-bit word from memory (two errors in the 8-bit data word, two errors in the 5-bit check word, or one error in each word).

The gross-error condition of all highs from memory will be detected. Otherwise, errors in three or more bits of the 13-bit word are beyond the capabilities of these devices to detect.

CONTROL FUNCTION TABLE

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECK WORD I/O	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	L	L	Generate Check Word	Input Data	Output Check Word	L	L
READ	L	H	Read Data & Check Word	Input Data	Input Check Word	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Check Word	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

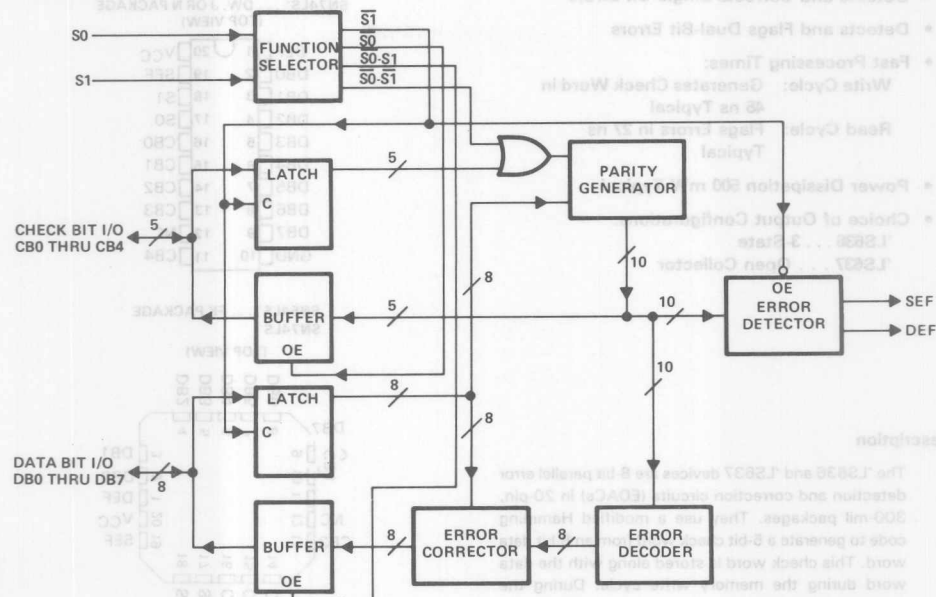
3-1069

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TTL DEVICES

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637 8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

functional block diagram



ERROR FUNCTION TABLE

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA
8-BIT DATA	5-BIT CHECKWORD	SEF	DEF	CORRECTION
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 8-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

error detection and correction details

During a memory write cycle, five check bits (CB0-CB4) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 5-bit check word is retrieved along with the 8-bit data word.

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637 8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

CHECKWORD BIT	8-BIT DATA WORD							
	0	1	2	3	4	5	6	7
CB0	X	X		X	X			
CB1	X		X	X		X	X	
CB2		X	X		X			X
CB3	X	X	X				X	X
CB4				X	X	X	X	X

The five check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

Error detection is accomplished as the 5-bit check word and the 8-bit data word from memory are applied to internal parity generators/checkers. If the parity of all five groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low.

- If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 8-bit data word will change the sense of exactly three bits of the 5-bit check word. Any single error in the 5-bit check word changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 8-bit data word and 5-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 5-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

ERROR SYNDROME TABLE

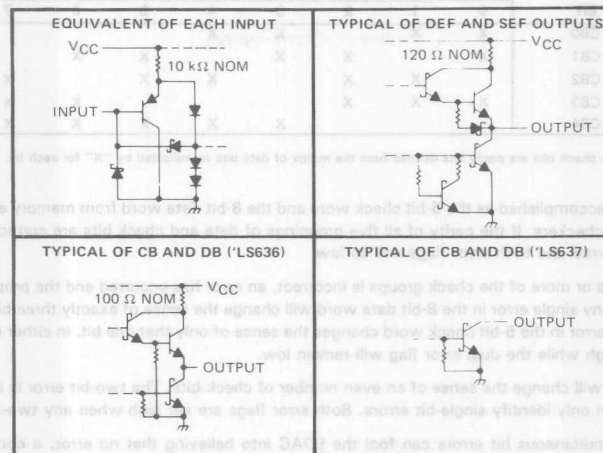
ERROR LOCATION	SYNDROME ERROR CODE				
	CB0	CB1	CB2	CB3	CB4
DB0	L	L	H	L	H
DB1	L	H	L	L	H
DB2	H	L	L	L	H
DB3	L	L	H	H	L
DB4	L	H	L	H	L
DB5	H	L	L	H	L
DB6	H	L	H	L	L
DB7	H	H	L	L	L
CB0	L	H	H	H	H
CB1	H	L	H	H	H
CB2	H	H	L	H	H
CB3	H	H	H	L	H
CB4	H	H	H	H	L
NO ERROR	H	H	H	H	H

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TTL DEVICES

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637 8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: S0 and S1	7 V
CB and DB	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS636, SN54LS637	-55°C to 125°C
SN74LS636, SN74LS637	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS636			SN74LS636			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	CB or DB, 'LS636 only			-1			-1	mA
		DEF or SEF			-0.4			-0.4	
V_{OH}	High-level output voltage	CB or DB, 'LS637 only			5.5			5.5	V
I_{OL}	Low-level output current	CB or DB			12			24	mA
		DEF or SEF			4			8	
t_{su}	Setup time	CB or DB before S1††	15			15			ns
		CB or DB before S1†	45			45			
t_h	Hold time	CB or DB after S1†	15			15			ns
T_A	Operating free-air temperature		-55		125	0		70	C

† This time guarantees the input data and checkword will be latched.

†† This time guarantees the input data and checkword will be latched plus that no glitch will occur on SEF or DEF flags.

† The upward-pointing arrow indicates a transition from low to high.

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637 8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS†	SN54LS636			SN74LS636			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	CB or DB DEF or SEF V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} min	I _{OH} = MAX I _{OH} = -400 µA	2.4 2.5	3.3 3.4	2.4 2.7	3.2 3.4		V
V _{OL}	Low-level output voltage	CB or DB DEF or SEF V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 4 mA I _{OL} = 8 mA	0.25 0.35 0.25	0.4 0.5 0.4	0.25 0.35 0.25	0.4 0.5 0.4		V
I _{OZH}	Off-state output current, high-level voltage applied	CB or DB V _{CC} = MAX, S ₀ and S ₁ at 2 V			20			20	µA
I _{OZL}	Off-state output current, low-level voltage applied	CB or DB V _{CC} = MAX, S ₀ and S ₁ at 2 V			-0.2			-0.2	mA
I _I	Input current at maximum input voltage	CB or DB S ₀ or S ₁ V _{CC} = MAX, V _I = 5.5 V V _I = 7 V			0.1 0.1			0.1 0.1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	µA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.2			-0.2	mA
I _{OS} §	Short-circuit output current	CB or DB DEF or SEF V _{CC} = MAX			-30 -20			-130 -100	mA
I _{CC}	Supply current	V _{CC} = MAX, S ₀ and S ₁ at 4.5 V, All CB and DB pins grounded, DEF and SEF open			100 160			100 160	mA

3

PARAMETER		TEST CONDITIONS†	SN54LS637			SN74LS637			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	DEF or SEF V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OH} = -400 µA	2.5	3.4	2.7	3.4		V
I _{OH}	High-level output current	CB or DB V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	V _{OH} = 5.5 V, V _{IL} = V _{IL} max		0.1			0.1	mA
V _{OL}	Low-level output voltage	CB or DB DEF or SEF V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 4 mA I _{OL} = 8 mA	0.25 0.35 0.25	0.4 0.5 0.4	0.25 0.35 0.25	0.4 0.5 0.4		V
I _I	Input current at maximum input voltage	CB or DB S ₀ or S ₁ V _{CC} = MAX, V _I = 5.5 V V _I = 7 V			0.1 0.1			0.1 0.1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	µA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.2			-0.2	mA
I _{OS} §	Short-circuit output current	DEF or SEF V _{CC} = MAX			-20			-100	mA
I _{CC}	Supply current	V _{CC} = MAX, S ₀ and S ₁ at 4.5 V, All CB and DB grounded, SEF and DEF open			90 144			90 144	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637 8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

'LS636 switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS636			UNIT
				MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output [○]	DB	CB	S0 at 0 V, S1 at 0 V, $R_L = 667\ \Omega$, See Figure 1	31	45		ns
t_{PHL} Propagation delay time, high-to-low-level output [○]			$R_L = 667\ \Omega$, See Figure 1	45	65		ns
t_{PLH} Propagation delay time, low-to-high-level output [*]	S1↑	DEF SEF	S0 at 3 V, $R_L = 2\text{ k}\Omega$, See Figure 1	27	40		ns
t_{PZH} Output enable time to high level [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 2	20	30		ns
t_{PZL} Output enable time to low level [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 1	24	40		ns
t_{PHZ} Output disable time from high level [△]	S0↑	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 2	30	45		ns
t_{PLZ} Output disable time from low level [△]	S0↑	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$, See Figure 1	43	65		ns
				31	45		ns

'LS637 switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$, see Figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS637			UNIT
				MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high level output [○]	DB	CB	S0 at 0 V, S1 at 0 V, $R_L = 667\ \Omega$	38	55		ns
t_{PHL} Propagation delay time, high-to-low-level output [○]			$R_L = 667\ \Omega$	45	65		ns
t_{PLH} Propagation delay time, low-to-high-level output [*]	S1↑	DEF SEF	S0 at 3 V, $R_L = 2\text{ k}\Omega$	27	40		ns
t_{PZH} Output enable time to high level [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$	20	30		ns
t_{PZL} Output enable time to low level [#]	S0↓	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$	28	45		ns
t_{PLH} Propagation delay time, low-to-high-level output [△]	S0↑	CB, DB	S1 at 3 V, $R_L = 667\ \Omega$	33	50		ns

[○]These parameters describe the time intervals taken to generate the check word during the memory write cycle.

^{*}These parameters describe the time intervals taken to flag errors during the memory read cycle.

[#]These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.

[△]These parameters describe the time intervals taken to disable the CB and DB buses in preparation for a new data word during the memory read cycle.

PARAMETER MEASUREMENT INFORMATION

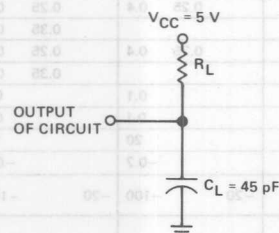


FIGURE 1—OUTPUT LOAD CIRCUIT

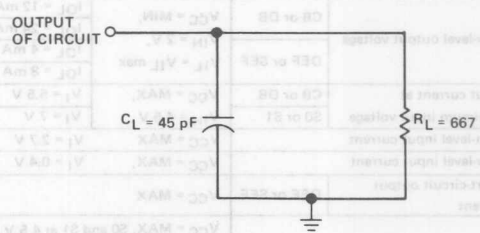


FIGURE 2—OUTPUT LOAD CIRCUIT

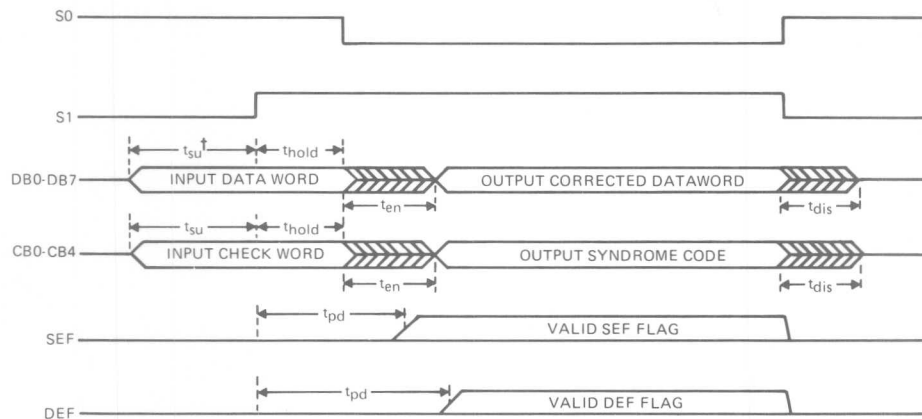
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TTL DEVICES

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637
8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

typical operating sequences

READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS



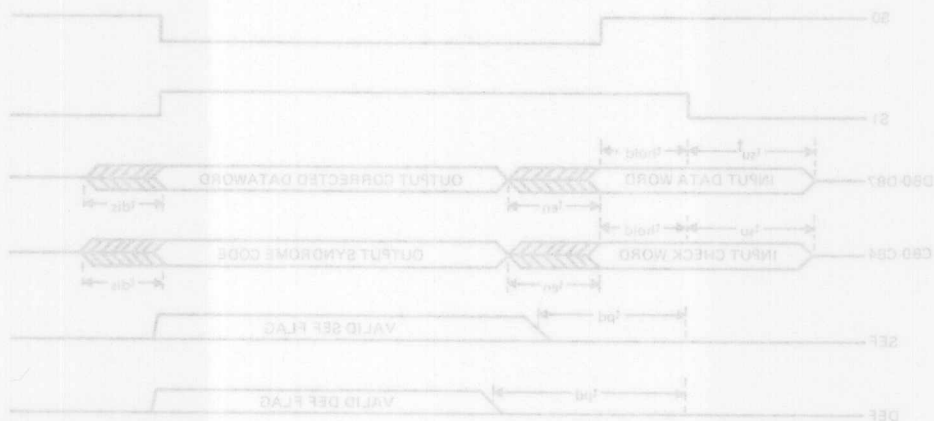
[†] NOTE: There are two conditions specified for t_{su} of Data or Checkword before S1[†]. See recommended operating conditions for detail.

3

TTL DEVICES

typical operating sequences

READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS



NOTE: There are two conditions specified for t_{HD} of Data in Checkword before ZEP. See recommended operating conditions for details.

3

TTL DEVICES

TYPES SN54LS638, SN54LS639, SN74LS638, SN74LS639 OCTAL BUS TRANSCEIVERS

D2636, JANUARY 1981 — REVISED DECEMBER 1983

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- A Bus Outputs are Open-Collector, B Bus Outputs are 3-State

description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so the buses are isolated.

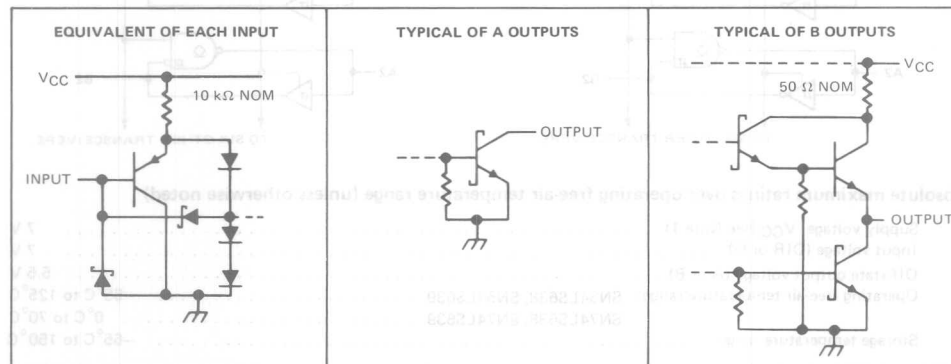
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
\bar{G}	DIR	'LS638	'LS639
L	L	\bar{B} data to A bus	B data to A bus
L	H	\bar{A} data to B bus	A data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS638	Open-Collector	3-State	Inverting
'LS639	Open-Collector	3-State	True

schematics of inputs and outputs

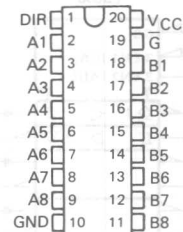


PRODUCTION DATA

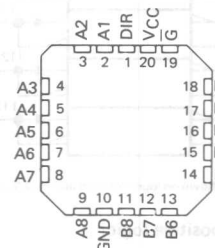
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

SN54LS638, SN54LS639 ... J PACKAGE
SN74LS638, SN74LS639 ... DW, J OR N PACKAGE
(TOP VIEW)



SN54LS638, SN54LS639 ... FK PACKAGE
SN74LS638, SN74LS639
(TOP VIEW)



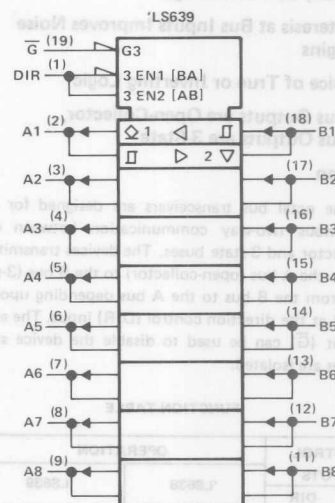
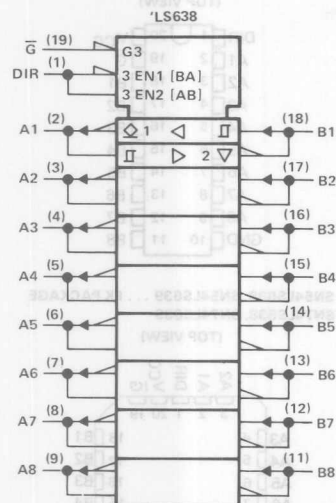
3

TTL DEVICES

3-1077

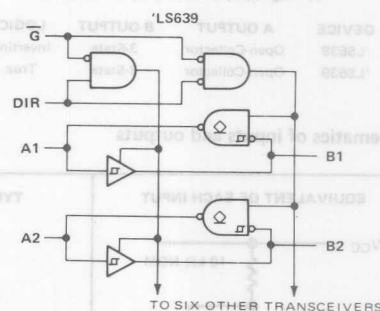
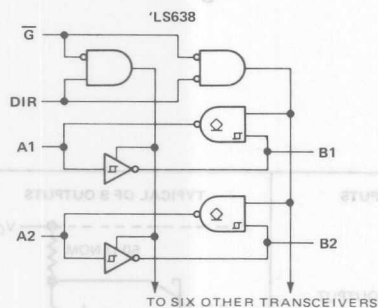
TYPES SN54LS638, SN54LS639, SN74LS638, SN74LS639 OCTAL BUS TRANSCEIVERS

logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (DIR or \bar{G})	7 V
Off-state output voltage (A or B)	5.5 V
Operating free-air temperature range:	
SN54LS638, SN54LS639	-55°C to 125°C
SN74LS638, SN74LS639	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

3

TTL DEVICES

TYPES SN54LS638, SN54LS639, SN74LS638, SN74LS639
OCTAL BUS TRANSCEIVERS

recommended operating conditions

	SN54LS ¹			SN74LS ¹			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH} (A bus)			5.5			5.5	V
High-level output current, I_{OH} (B bus)			-12			-15	mA
Low-level output current, I_{OL} (A or B bus)			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS ¹			SN74LS ¹			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.5			0.6	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	A $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OH}	High-level output voltage	B $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -3 \text{ mA}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4			2.4			V
V_{OL}	Low-level output voltage	A or B $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 12 \text{ mA}, V_{IL} = \text{MAX}, I_{OL} = 24 \text{ mA}$		0.25	0.4		0.25	0.4	V
I_{OZH}	Off-state output current, high-level voltage applied	B $V_{CC} = \text{MAX}, \bar{G}$ at 2 V, $V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	A or B $V_{CC} = \text{MAX}, \bar{G}$ at 2 V, $V_O = 0.4 \text{ V}$		-0.4			-0.4		mA
I_I	Input current at maximum input voltage	A or B $V_{CC} = \text{MAX}$ DIR or \bar{G} $V_I = 5.5 \text{ V}$ $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS}	Short-circuit output current [§]	B $V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = \text{MAX}$, Outputs open		48	70		48	70	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = \text{MAX}$, Outputs open		62	90		62	90	mA
I_{CCZ}	Supply current, outputs off	$V_{CC} = \text{MAX}$, Outputs open		64	95		64	95	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS638			'LS639			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B	$C_L = 45 \text{ pF}, R_L = 667 \Omega$	6	10		8	15		ns
	B	A		17	25		19	25		
t_{PHL}	A	B		8	15		11	15		ns
	B	A		14	25		16	25		
t_{PLH}	\bar{G}	A		26	40		23	40		ns
t_{PHL}	\bar{G}	A		43	60		34	50		ns
t_{PZH}	\bar{G}	B	$C_L = 5 \text{ pF}, R_L = 667 \Omega$	23	40		26	40		ns
t_{PZL}	\bar{G}	B		31	40		31	40		ns
t_{PHZ}	\bar{G}	B		15	25		15	25		ns
t_{PLZ}	\bar{G}	B		15	25		15	25		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS638, SN54LS639, SN74LS638, SN74LS639 OCTAL BUS TRANSCEIVERS

TYPICAL CHARACTERISTICS

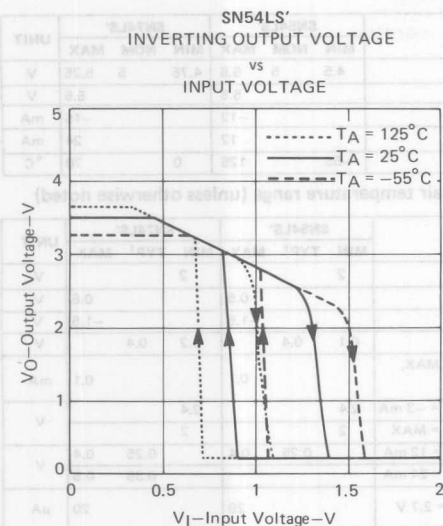


FIGURE 1

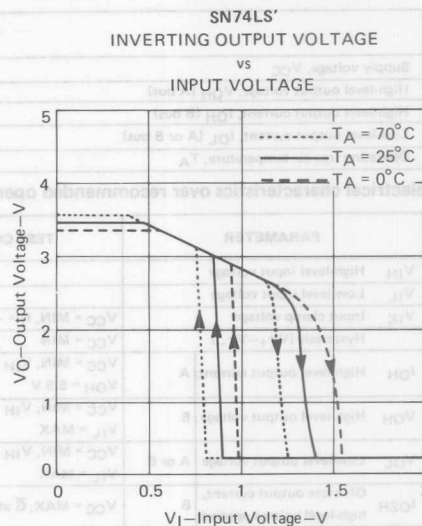


FIGURE 2

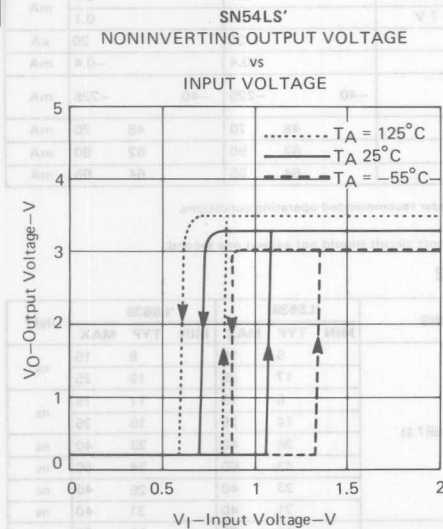


FIGURE 3

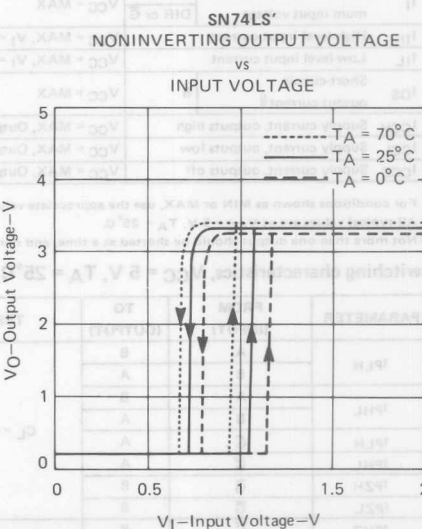


FIGURE 4

3

TTL DEVICES

TYPES SN54LS640 THRU SN54LS645, SN74LS640 THRU SN74LS645 OCTAL BUS TRANSCEIVERS

D2420, APRIL 1979—REVISED DECEMBER 1983

- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS643	3-State	True and inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

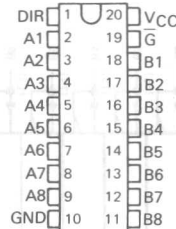
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

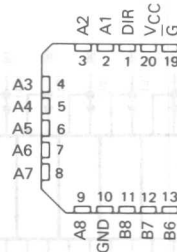
The -1 versions of the SN74LS640 thru SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS645.

The SN54LS640 thru SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS645 are characterized for operation from 0°C to 70°C.

SN54LS' ... J PACKAGE
SN74LS' ... DW, J OR N PACKAGE
(TOP VIEW)



SN54LS' ... FK PACKAGE
SN74LS' ...
(TOP VIEW)



FUNCTION TABLE

CONTROL	OPERATION			
	INPUTS	'LS640	'LS641	'LS643
G	DIR	'LS642	'LS645	'LS644
L	L	B data to A bus	B data to A bus	B data to A bus
L	H	A data to B bus	A data to B bus	A data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

3

TTL DEVICES

PRODUCTION DATA

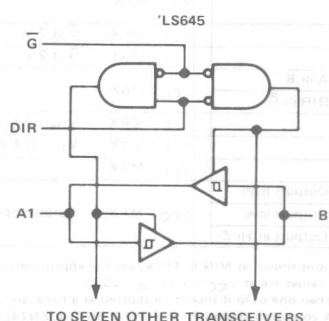
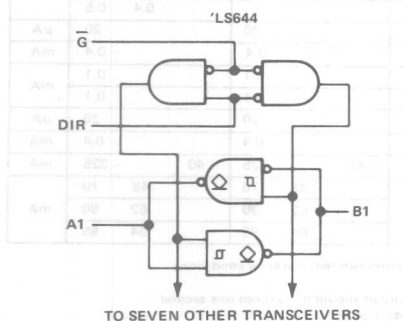
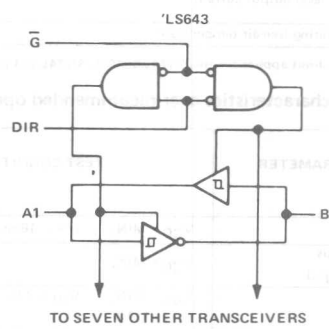
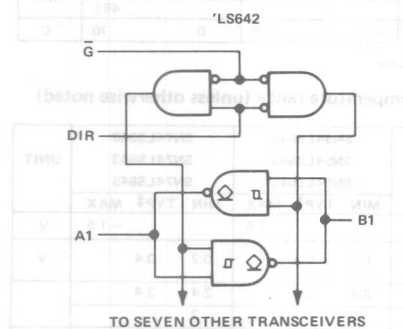
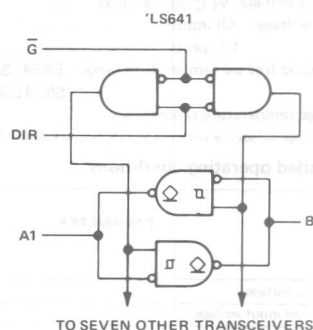
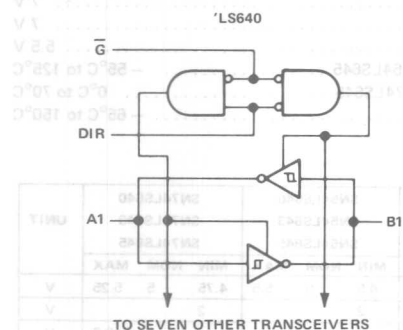
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TEXAS
INSTRUMENTS

logic symbols

TYPES SN54LS640 THRU SN54LS645,
SN74LS640 THRU SN74LS645
OCTAL BUS TRANSCEIVERS

logic diagrams



3

TTL DEVICES

**TYPES SN54LS640, SN54LS643, SN54LS645,
SN74LS640, SN74LS643, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS640, SN54LS643, SN54LS645	–55°C to 125°C
SN74LS640, SN74LS643, SN74LS645	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.5			0.6	V
I_{OH} High-level output current			–12			–15	mA
I_{OL} Low-level output current			12			24	mA
						48 §	
T_A Operating free-air temperature	–55		125	0		70	°C

§ The 48 mA limit applies for the SN74LS640-1, SN74LS643-1, and SN74LS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			UNIT		
				MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IK}		V _{CC} = MIN, I _I = – 18 mA		– 1.5			– 1.5			V		
Hysteresis (V _{T+} – V _{T–})		V _{CC} = MIN, A or B input		0.1	0.4		0.2	0.4		V		
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OH} = – 3 mA		2.4	3.4		2.4	3.4		
				I _{OH} = MAX		2		2				
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX		I _{OL} = 12 mA		0.25		0.4		V		
				I _{OL} = 24 mA				0.35			0.5	
				I _{OL} = 48 mA ¶				0.4			0.5	
I _{OZH}		V _{CC} = MAX, G̅ at 2 V, V _O = 2.7 V		20			20			µA		
I _{OZL}		V _{CC} = MAX, G̅ at 2 V, V _O = 0.4 V		– 0.4			– 0.4			mA		
I _I	A or B	V _{CC} = MAX		V _I = 5.5 V		0.1		0.1		mA		
	DIR or G̅			V _I = 7 V		0.1		0.1				
I _{IH}		V _{CC} = MAX, V _{IH} = 2.7 V		20			20			µA		
I _{IL}		V _{CC} = MAX, V _{IL} = 0.4 V		– 0.4			– 0.4			mA		
I _{OS} §		V _{CC} = MAX		– 40	– 225		– 40	– 225		mA		
I _{CC}	Outputs high	V _{CC} = MAX, Outputs open		48			70	48		70	mA	
	62			90	62		90					
	64			95	64		95					
Outputs at Hi-Z												

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ The 48 mA condition applies for the SN74LS640-1, SN74LS643-1, and SN74LS645-1 only.

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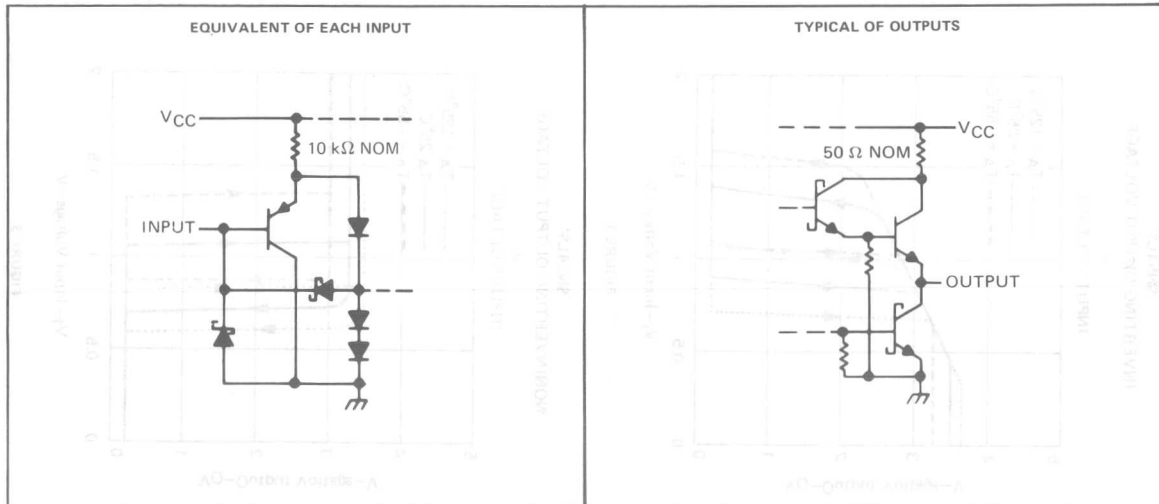
TTL DEVICES

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640-1			'LS643, 'LS643-1			'LS645, 'LS645-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$, See Note 2		6	10		6	10		8	15	ns
t_{PHL} Propagation delay time, high-to-low-level output	B	A			6	10		8	15		8	15	ns
	A	B			8	15		9	15		11	15	ns
	B	A			8	15		11	15		11	15	ns
t_{pZL} Output enable time to low level	\overline{G}	A	See Note 2		31	40		32	45		31	40	ns
	\overline{G}	B			31	40		32	45		31	40	ns
t_{pZH} Output enable time to high level	\overline{G}	A			23	40		27	40		26	40	ns
	\overline{G}	B			23	40		23	40		26	40	ns
t_{PLZ} Output disable time from low level	\overline{G}	A	$C_L = 5\text{ pF}$, $R_L = 667\ \Omega$, See Note 2		15	25		15	25		15	25	ns
	\overline{G}	B			15	25		15	25		15	25	ns
t_{PHZ} Output disable time from high level	\overline{G}	A			15	25		15	25		15	25	ns
	\overline{G}	B			15	25		15	25		15	25	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



TYPES SN54LS640, SN54LS643, SN54LS645,
SN74LS640, SN74LS643, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

**TYPES SN54LS640, SN54LS643, SN54LS645,
SN74LS640, SN74LS643, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

TYPICAL CHARACTERISTICS

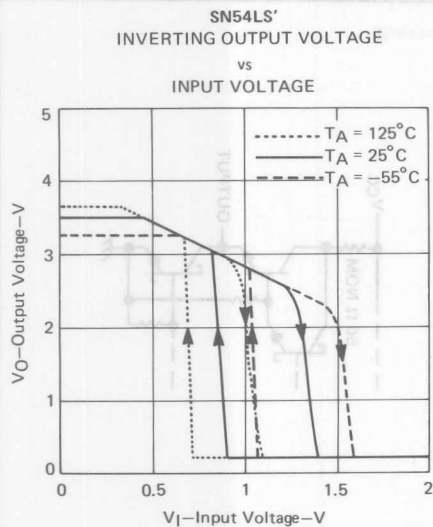


FIGURE 1

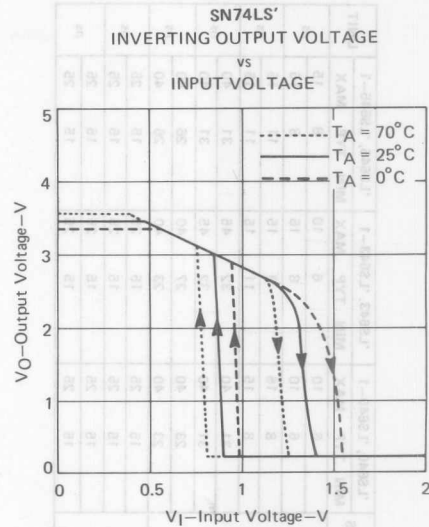


FIGURE 2

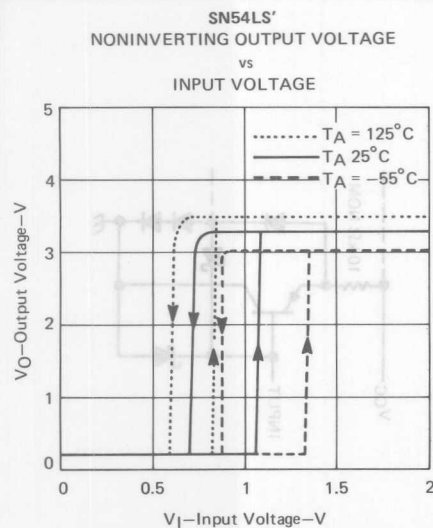


FIGURE 3

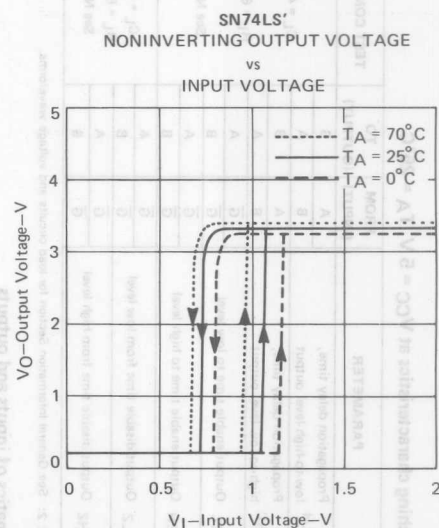


FIGURE 4

**TYPES SN54LS641, SN54LS642, SN54LS644,
SN74LS641, SN74LS642, SN74LS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs and I/O ports	7 V
Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644	– 55° C to 125° C
SN74LS641, SN74LS642, SN74LS644	0° C to 70° C
Storage temperature range	– 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.5			0.6	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			12			24	mA
						48 §	
T_A Operating free-air temperature	– 55		125	0		70	° C

§ The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}, \text{A or B input}$	0.1	0.4		0.2	0.4		V
I_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$			0.25			0.25	V
							0.35	
							0.4	
I_I	A or B			0.1			0.1	mA
	DIR or G			0.1			0.1	
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
I_{CC}	Outputs high			48			48	mA
	Outputs low			62			62	
	Outputs at Hi-Z			64			64	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

3

TTL DEVICES

TYPES SN54LS641, SN54LS642, SN54LS644
SN74LS641, SN74LS642, SN74LS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

TTL DEVICES

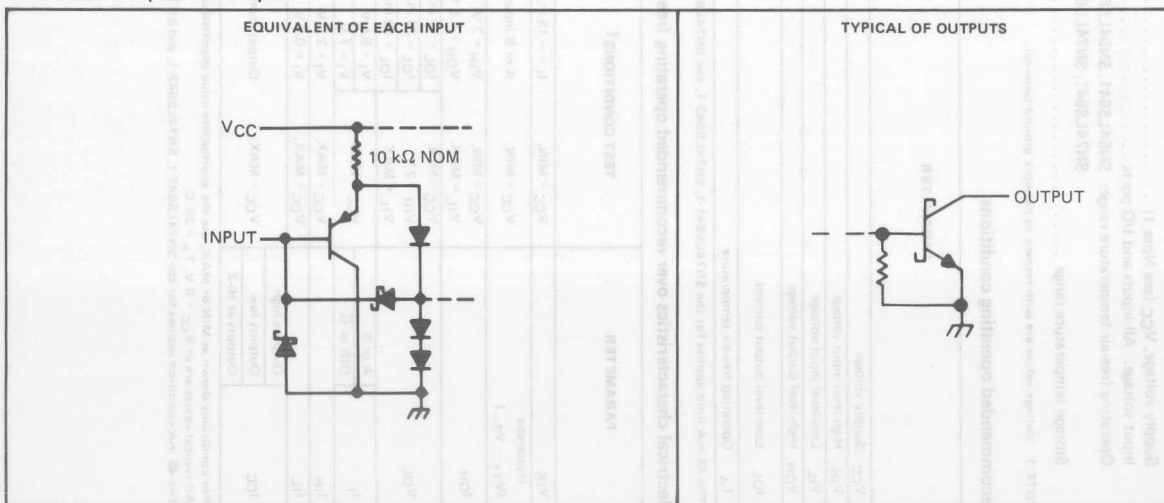
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switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641-1			'LS642, 'LS642-1			'LS644, 'LS644-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$, See Note 2	17	25		19	25		17	25		ns
t_{PHL} Propagation delay time, high-to-low-level output	B	A		17	25		19	25		19	25		ns
t_{PLH} Output disable time from low level	\bar{G} , DIR	A		16	25		14	25		14	25		ns
t_{PLH} Output enable time from low level	\bar{G} , DIR	B		16	25		14	25		16	25		ns
t_{PLH} Output disable time from high level	\bar{G} , DIR	A		23	40		26	40		26	40		ns
t_{PHL} Output enable time from high level	\bar{G} , DIR	B		25	40		28	40		25	40		ns
				34	50		43	60		43	60		ns
				37	50		39	60		37	50		ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



TYPES SN54LS646 THRU SN54LS649 SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1982—REVISED DECEMBER 1983

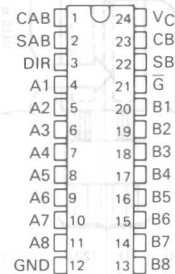
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Included Among the Package Options Are Compact 24-pin 300-mil Wide DIPs and Both 28-pin Plastic and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

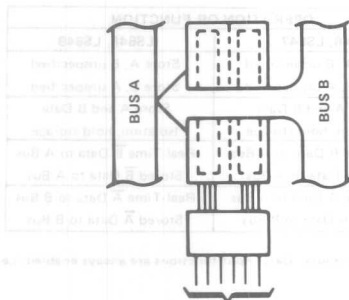
description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

SN54LS' ... JT PACKAGE
SN74LS' ... DW, JT OR NT PACKAGE
(TOP VIEW)

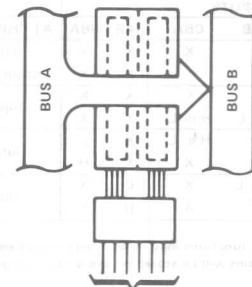


SN54LS' ... FK PACKAGE
SN74LS' ... (TOP VIEW)



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	H	H or L	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

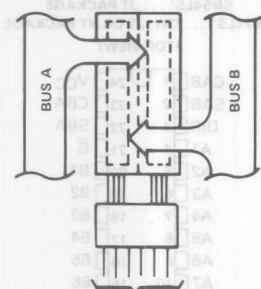
3-1089

3

TTL DEVICES

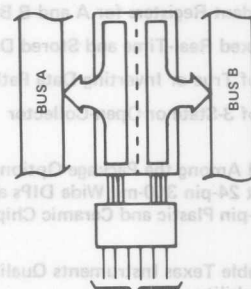
TYPES SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	H
L	H	X	X	H	X

TRANSFER
STORED DATA
TO A OR B

Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0° to 70°C .

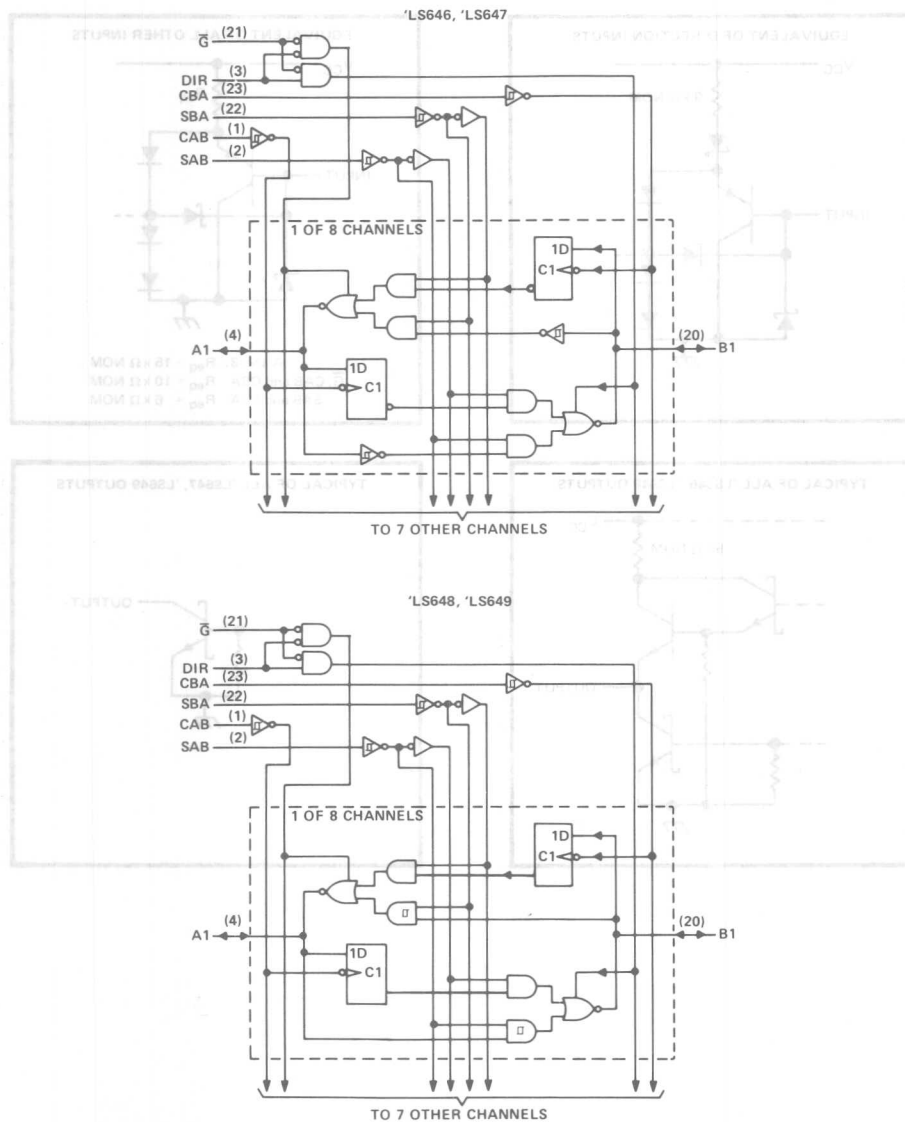
FUNCTION TABLE

INPUTS						DATA I/O [†]		OPERATION OR FUNCTION	
\bar{G}	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	LS646, LS647	LS648, LS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	H or L	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	X	X	H	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus
L	H	H or L	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
L	H	X	X	H	X	Input	Output	Stored A Data to B Bus	Stored A Data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

TYPES SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

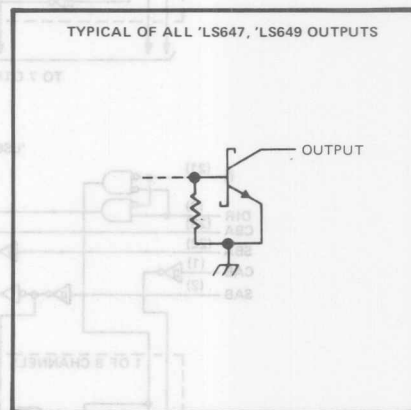
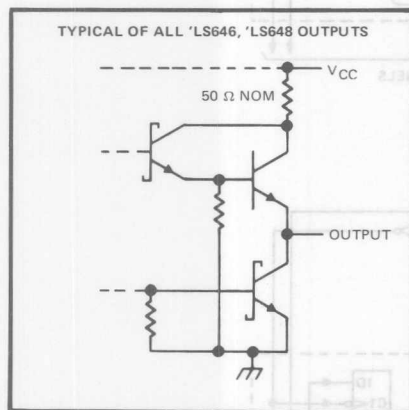
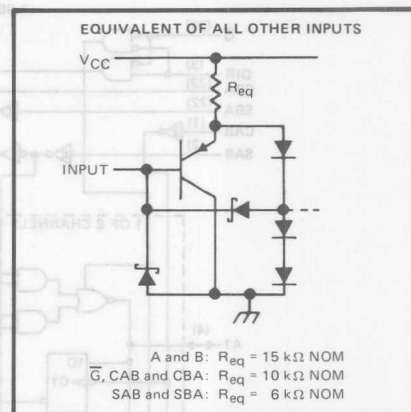
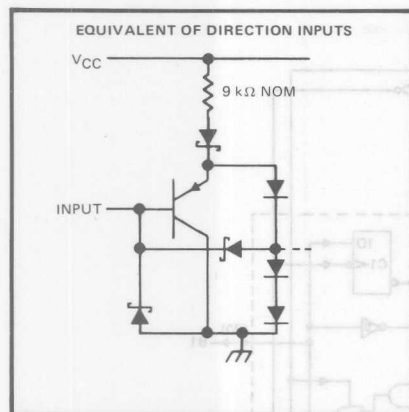
logic diagrams (positive logic)



Pin numbers shown on logic notation are for DW or NT packages.

TYPES SN54LS646 THRU SN54LS649,
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

schematics of inputs and outputs

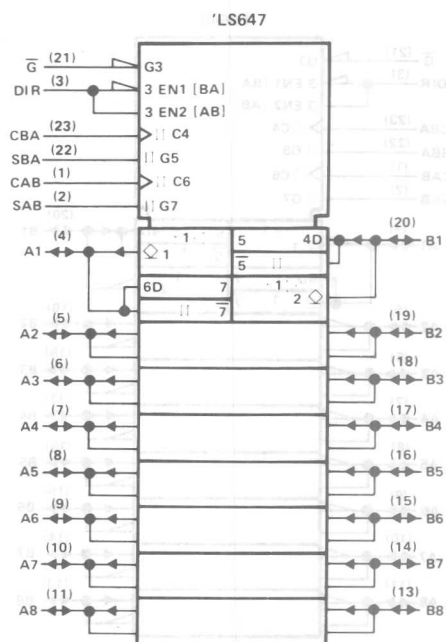
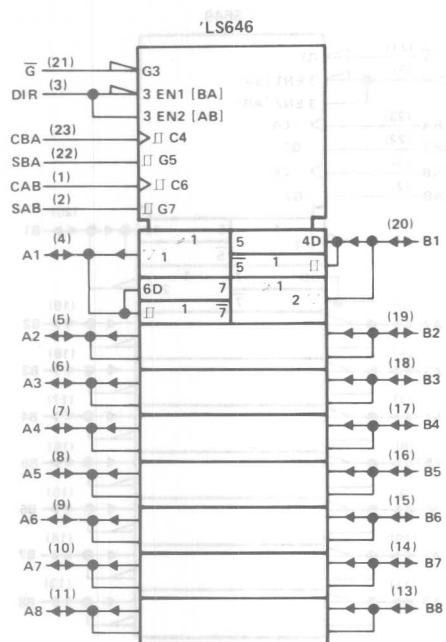


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TTL DEVICES

TYPES SN54LS646, SN54LS647, SN74LS646, SN74LS647 OCTAL BUS TRANSCEIVERS AND REGISTERS

logic symbols

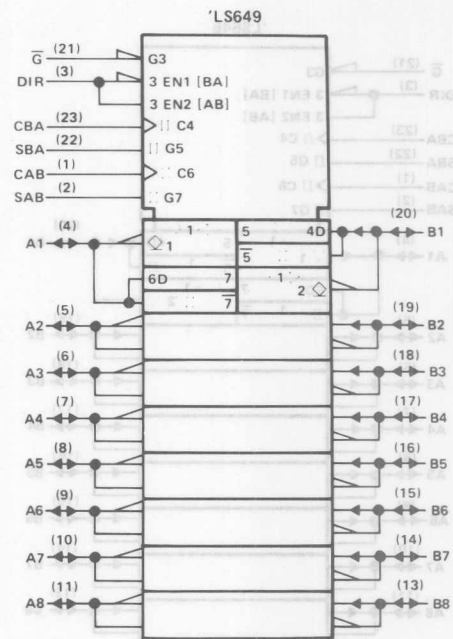
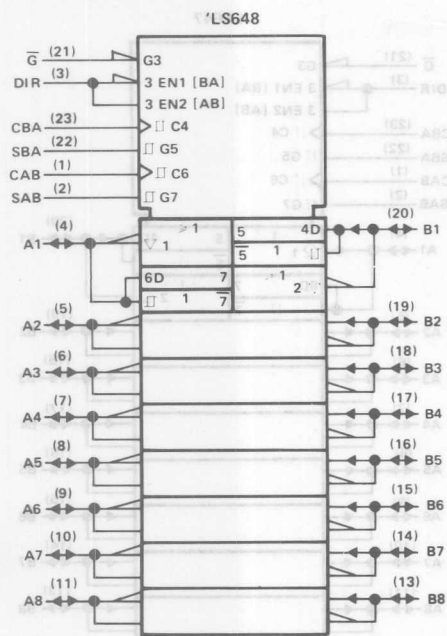


Pin numbers shown on logic notation are for DW or NT packages.

3
TTL DEVICES

TYPES SN54LS648, SN54LS649, SN74LS648, SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

logic symbols (continued)



Pin numbers shown on logic notation are for DW or NT packages.

Logic symbol for LS648 and LS649 is shown in the logic notation.

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TTL DEVICES

TYPES SN54LS646, SN54LS648, SN74LS646, SN74LS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS646, SN54LS648	–55°C to 125°C
SN74LS646, SN74LS648	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

		SN54LS646/648			SN74LS646/648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.5			0.6	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration	CBA or CAB high			15			ns
		CBA or CAB low			30			
		Data high or low			30			
t_{su}	Setup time before CAB† or CBA†	A or B			15			ns
t_h	Hold time after CAB† or CBA†	A or B			0			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS646/648			SN74LS646/648			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}		V _{CC} = MIN, I _I = – 18 mA		– 1.5			– 1.5			V
Hysteresis (V _{T+} – V _{T–})	A or B input	V _{CC} = MIN		0.1	0.4		0.2	0.4		V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = – 3 mA	2.4	3.4		2.4	3.4		V
			I _{OH} = – 12 mA	2						
			I _{OH} = – 15 mA				2			
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25		0.4	0.25		0.4	V
			I _{OL} = 24 mA			0.35		0.5		
I _I	Control inputs	V _{CC} = MAX, V _I = 7 V		0.1			0.1			mA
	A or B ports	V _{CC} = MAX, V _I = 5.5 V		0.1			0.1			
I _{IH}	Control inputs	V _{CC} = MAX, V _I = 2.7 V		20			20			μA
	A or B ports▲			20			20			
I _{IL}	Control inputs	V _{CC} = MAX, V _I = 0.4 V		– 0.4			– 0.4			mA
	A or B ports▲			– 0.4			– 0.4			
I _{OS} ¶		V _{CC} = MAX, V _O = 0 V		– 40	– 225	– 40	– 225		mA	
I _{CC}	LS646	V _{CC} = MAX	Outputs high	91	145		91	145	mA	
			Outputs low	103	165		103	165		
			Outputs disabled	103	165		103	165		
	LS648		Outputs high	91	145		91	145		
			Outputs low	103	165		103	165		
			Outputs disabled	120	180		120	180		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

¶ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

▲ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

TYPES SN54LS646, SN54LS648, SN74LS646, SN74LS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	CAB or CBA	A or B	R _L = 667 Ω, C _L = 45 pF, See Note 2	15	25		15	25		ns
t _{PHL}				23	35		24	40		ns
t _{PLH}	A or B	B or A		12	18		12	18		ns
t _{PHL}				13	20		15	25		ns
t _{PLH}	SAB or SBA† with Bus input high	A or B		26	40		37	55		ns
t _{PHL}				21	35		24	40		ns
t _{PLH}	SAB or SBA† with Bus input low	A or B		33	50		26	40		ns
t _{PHL}				14	25		23	40		ns
t _{PZH}	\overline{G}	A or B	33	55		30	50		ns	
t _{PZL}			42	65		37	55		ns	
t _{PZH}	DIR	A or B	28	45		23	40		ns	
t _{PZL}			39	60		30	45		ns	
t _{PHZ}	\overline{G}	A or B	23	35		28	45		ns	
t _{PLZ}			22	35		22	35		ns	
t _{PHZ}	DIR	A or B	20	30		24	35		ns	
t _{PLZ}			19	30		19	30		ns	

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{OL}	0.1	0.2	0.4	V	$V_{CC} = \text{MIN}$, $I_L = -10\text{ mA}$
V_{OH}	2.4	2.7	3.0	V	$V_{CC} = \text{MIN}$, $I_{OH} = -10\text{ mA}$
V_{OL}	0.1	0.2	0.4	V	$V_{CC} = \text{MAX}$, $I_L = -10\text{ mA}$
V_{OH}	2.4	2.7	3.0	V	$V_{CC} = \text{MAX}$, $I_{OH} = -10\text{ mA}$
I_{OL}	10	20	30	mA	$V_{OL} = 0.4\text{ V}$, $V_{CC} = \text{MAX}$
I_{OH}	10	20	30	mA	$V_{OH} = 2.4\text{ V}$, $V_{CC} = \text{MAX}$
I_{IL}	10	20	30	mA	$V_{OL} = 0.4\text{ V}$, $V_{CC} = \text{MAX}$
I_{IH}	10	20	30	mA	$V_{OH} = 2.4\text{ V}$, $V_{CC} = \text{MAX}$
t_{PLH}	15	25	35	ns	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$
t_{PHL}	23	35	45	ns	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$
t_{PZH}	33	55	65	ns	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$
t_{PZL}	42	65	75	ns	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$
t_{PHZ}	23	35	45	ns	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$
t_{PLZ}	22	35	45	ns	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$

1. For conditions shown as MIN or MAX, the characteristic is guaranteed only under recommended operating conditions.
2. All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
3. For more than one output shown as MIN or MAX, the output shown as MIN or MAX is the worst case.
4. For I_{OL} and I_{OH} , the parameter is the average of the output current.

TYPES SN54LS647, SN54LS649, SN74LS647, SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649	–55°C to 125°C
SN74LS647, SN74LS649	–0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V_{IH}	High-level input voltage	2			2			V	
V_{IL}	Low-level input voltage			0.5			0.6	V	
V_{OH}	High-level output voltage			5.5			5.5	V	
I_{OL}	Low-level output voltage			12			24	mA	
t_w	Pulse duration	CBA or CAB high			15			ns	
		CBA or CAB low			30				
		Data high or low			30				
t_{su}	Setup time before CAB \uparrow or CBA \uparrow	A or B			15			ns	
t_h	Hold time after CAB \uparrow or CBA \uparrow	A or B			0			ns	
T_A	Operating free-air temperature				− 55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS647 SN54LS649		SN74LS647 SN74LS649		UNIT	
			MIN	TYP‡ MAX	MIN	TYP‡ MAX		
V _{IK}		V _{CC} = MIN, I _I = − 18 mA	− 1.5		− 1.5		V	
Hysteresis (V _{T+} − V _{T−})	A or B input	V _{CC} = MIN	0.1	0.4	0.2	0.4	V	
I _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 5.5 V	0.1		0.1		mA	
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX I _{OL} = 12 mA I _{OL} = 24 mA	0.25	0.4	0.25	0.4 0.35 0.5	V	
I _I	A or B	V _{CC} = MAX	0.1		0.1		mA	
	All others		0.1		0.1			
I _{IH}		V _{CC} = MAX, V _I = 2.7 V	20		20		μA	
I _{IL}		V _{CC} = MAX, V _I = 0.4 V	− 0.4		− 0.4		mA	
I _{CC}	'LS647	V _{CC} = MAX, Outputs open	Outputs high	79	130	79	130	mA
			Outputs low	94	150	94	150	
	'LS649	V _{CC} = MAX, Outputs open	Outputs high	79	130	79	130	
			Outputs low	94	150	94	150	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

3

TTL DEVICES

TYPES SN54LS647, SN54LS649, SN74LS647, SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	CAB or CBA	A or B	R _L = 667 Ω, C _L = 45 pF, See Note 2	22	35	17	30	ns		
t _{PHL}				28	45	28	45	ns		
t _{PLH}	A or B	B or A		17	26	15	25	ns		
t _{PHL}				18	27	20	30	ns		
t _{PLH}	SAB or SBA† with Bus input high	A or B		33	50	37	55	ns		
t _{PHL}				29	45	28	45	ns		
t _{PLH}	SAB or SBA† with Bus input low			39	60	30	45	ns		
t _{PHL}				19	30	26	40	ns		
t _{PLH}	G	A or B		25	40	21	40	ns		
t _{PHL}				33	50	34	50	ns		
t _{PLH}	DIR			23	35	19	30	ns		
t _{PHL}				25	40	27	45	ns		

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

PARAMETER	TEST CONDITIONS		UNIT	
	MIN	MAX	MIN	MAX
V_{IH}	$V_{CC} = \text{MIN}$	$V_{CC} = \text{MIN}$	V	V
V_{IL}	$V_{CC} = \text{MIN}$	$V_{CC} = \text{MIN}$	V	V
I_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 5\text{ V}$, $V_{OL} = \text{MAX}$	$V_{CC} = \text{MIN}$, $V_{IH} = 5\text{ V}$, $V_{OL} = \text{MAX}$	mA	mA
I_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 5\text{ V}$, $V_{OL} = \text{MAX}$	$V_{CC} = \text{MIN}$, $V_{IH} = 5\text{ V}$, $V_{OL} = \text{MAX}$	mA	mA
I_{IH}	$V_{CC} = \text{MAX}$	$V_{CC} = \text{MAX}$	mA	mA
I_{IL}	$V_{CC} = \text{MAX}$	$V_{CC} = \text{MAX}$	mA	mA
t_{PLH}	$V_{CC} = \text{MAX}$, $V_{IH} = 5\text{ V}$	$V_{CC} = \text{MAX}$, $V_{IH} = 5\text{ V}$	ns	ns
t_{PHL}	$V_{CC} = \text{MAX}$, $V_{IH} = 5\text{ V}$	$V_{CC} = \text{MAX}$, $V_{IH} = 5\text{ V}$	ns	ns

† For conditions shown as MIN or MAX, use the appropriate value specified with recommended operating free-air temperature range. All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

TYPES SN54LS651 THRU SN54LS654 SN74LS651 THRU SN74LS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

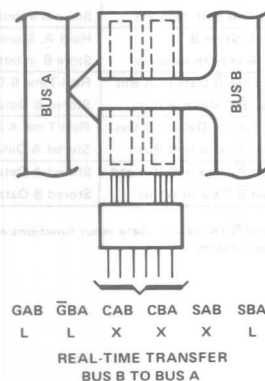
D2637, JANUARY 1981 - REVISED DECEMBER 1983

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Dependable Texas Instruments Quality and Reliability

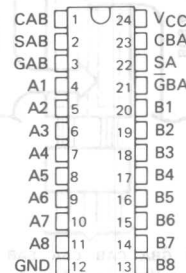
DEVICE	A OUTPUT	B OUTPUT	LOGIC
LS651	3-State	3-State	Inverting
LS652	3-State	3-State	True
LS653	Open-collector	3-State	Inverting
LS654	Open-collector	3-State	True

description

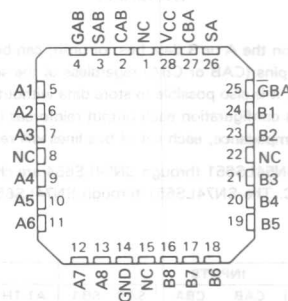
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651, 'LS652, 'LS653, and 'LS654.



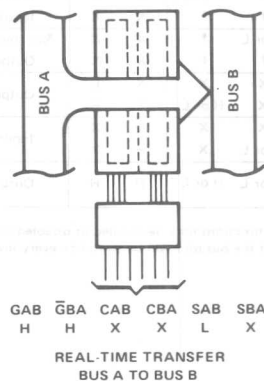
SN54LS' ... JT PACKAGE
SN74LS' ... DW, JT OR NT PACKAGE
(TOP VIEW)



SN54LS' ... FK PACKAGE
SN74LS' ...
(TOP VIEW)



NC — No internal connection



PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

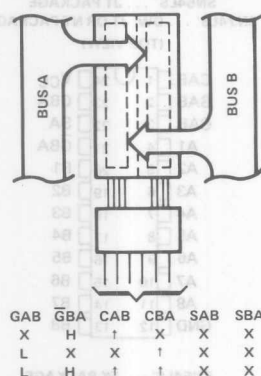
TEXAS
INSTRUMENTS

3-1099

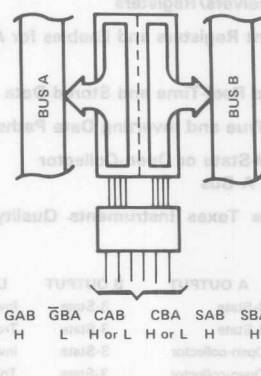
3

TTL DEVICES

TYPES SN54LS651 THRU SN54LS654 SN74LS651 THRU SN74LS654 OCTAL BUS TRANSCEIVERS AND REGISTERS



STORAGE FROM
A AND/OR B



TRANSFER
STORED DATA
TO A AND/OR B

Data on the A or B data bus, or both, can be stored in the internal D flip-flop by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54LS651 through SN54LS654 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS651 through SN74LS654 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS					DATA I/O*		OPERATION OR FUNCTION	
GAB	GBA	CAB	CBA	SAB SBA	A1 THRU A8	B1 THRU B8	'LS651, 'LS653	'LS652, 'LS654
L	H	H or L	H or L	X X	Input	Input	Isolation	Isolation
L	H	↑	↑	X X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X X	Input		Store A in both registers	Store A in both registers
L	X	H or L	↑	X X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X X			Store B in both registers	Store B in both registers
L	L	X	X	X L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X H			Stored B Data to A Bus	Stored B Data to A Bus
H	H	X	X	L X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H X			Stored A Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

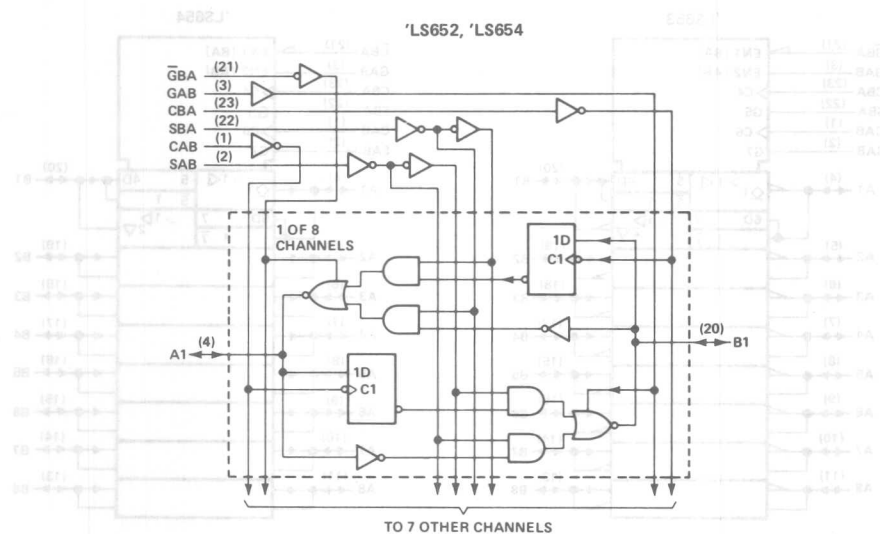
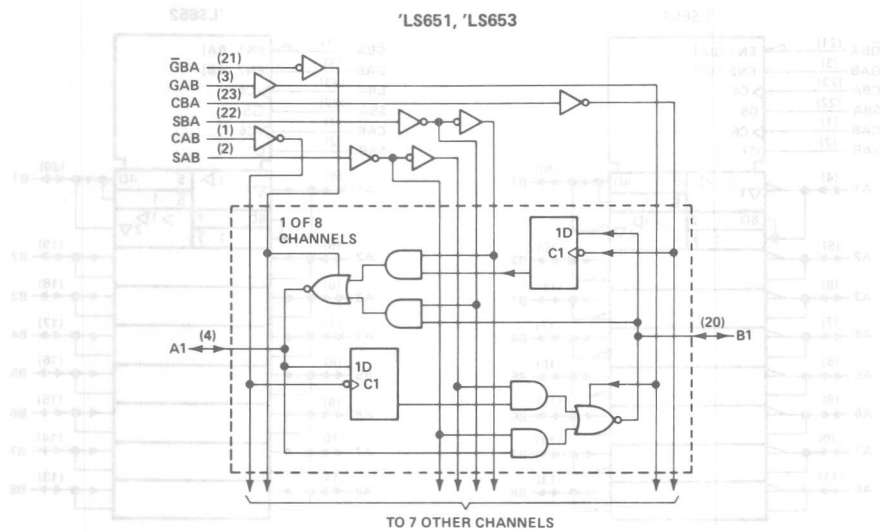
3

TTL DEVICES

TYPES SN54LS651 THRU SN54LS654 SN74LS651 THRU SN74LS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

logic diagrams (positive logic)

logic symbols



Pin numbers shown on logic notation are for DW, JT or NT packages.

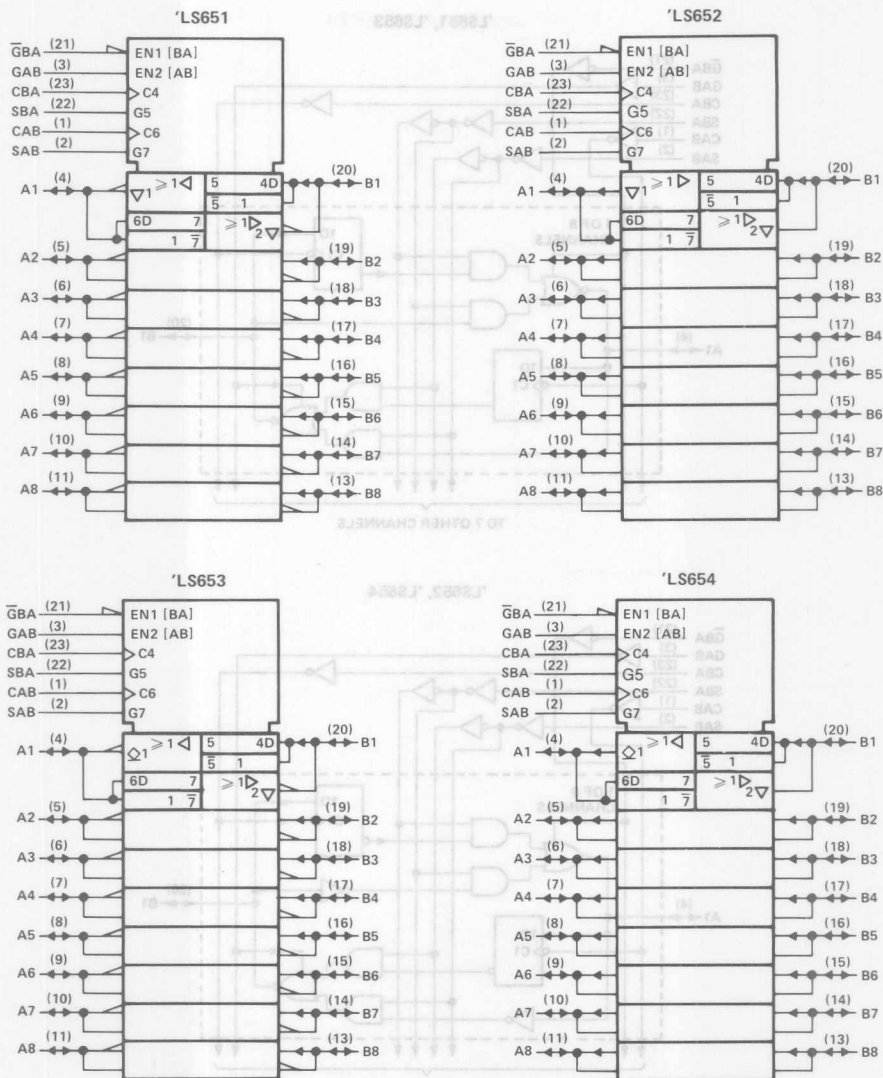
3

TTL DEVICES

**TYPES SN54LS651 THRU SN54LS654
SN74LS651 THRU SN74LS654
OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols

(signal invert) anmrsib signal



Pin numbers shown on logic notation are for DW, JT or NT packages.

3

TTL DEVICES

TYPES SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS651, SN54LS652	– 55°C to 125°C
SN74LS651, SN74LS652	0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

		SN54LS651 SN54LS652				SN74LS651 SN74LS652				UNIT
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage			0.7			0.8	V		
I _{OH}	High-level output current			– 12			– 15	mA		
I _{OL}	Low-level output current			12			24	mA		
t _w	Pulse duration			CBA or CAB high	15			15	ns	
				CBA or CAB low	30			30		
				Data high or low	30			30		
t _{su}	Setup time before CAB ↑ or CBA ↑	A or B			15			15	ns	
t _h	Hold time after CAB ↑ or CBA ↑	A or B			0			0	ns	
T _A	Operating free-air temperature				– 55	125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$					– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}$	$I_{OH} = -3 \text{ mA}$		2.4	3.4		2.4	3.4		V
		$I_{OH} = -12 \text{ mA}$		2						
		$I_{OH} = -15 \text{ mA}$					2			
V_{OL}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}$	$I_{OL} = 12 \text{ mA}$			0.25	0.4		0.25	0.4	V
		$I_{OL} = 24 \text{ mA}$						0.35	0.5	
I_I	Control inputs	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$				0.1			0.1	mA
	A or B ports	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				0.1			0.1	
I_{IH}	Control inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				20			20	μA
	A or B ports \blacktriangle					20			20	
I_{IL}	Control inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				– 0.4			– 0.4	mA
	A or B ports \blacktriangle					– 0.4			– 0.4	
I_{OS}		$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$		– 40		– 225	– 40		– 225	mA
I_{CC}	LS651 LS652	$V_{CC} = \text{MAX}$	Outputs high		95	145		95	145	mA
			Outputs low		103	165		103	165	
			Outputs disabled		103	165		103	165	
			Outputs high		95	145		95	145	
			Outputs low		103	165		103	165	
			Outputs disabled		120	180		120	180	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[¶] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[▲] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

3

TTL DEVICES

TYPES SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS651			'LS652			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus		14	24		15	25		ns
t_{PHL}				23	35		24	36		ns
t_{PLH}	Bus	Bus		9	18		12	18		ns
t_{PHL}				20	30		13	20		ns
t_{PLH}	Select, with bus input	Bus	$R_L = 667\ \Omega$, See Note 2 $C_L = 45\text{ pF}$	31	47		23	35		ns
t_{PHL}	high [†]			22	33		21	32		ns
t_{PLH}	Select, with bus input			23	35		33	50		ns
t_{PHL}	low [†]			19	30		15	23		ns
t_{PZH}	$\overline{\text{G}}\text{BA}$	A Bus		29	44		30	45		ns
t_{PZL}				40	60		36	54		ns
t_{PZH}	GAB	B Bus		19	29		20	30		ns
t_{PZL}				26	40		25	38		ns
t_{PHZ}	$\overline{\text{G}}\text{BA}$	A Bus	$R_L = 667\ \Omega$, See Note 2 $C_L = 5\text{ pF}$	25	38		25	38		ns
t_{PLZ}				19	30		19	30		ns
t_{PHZ}	GAB	B Bus		25	38		25	38		ns
t_{PLZ}				19	30		19	30		ns

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

t_{PZH} = output enable time to high level.

t_{PZL} = output enable time to low level.

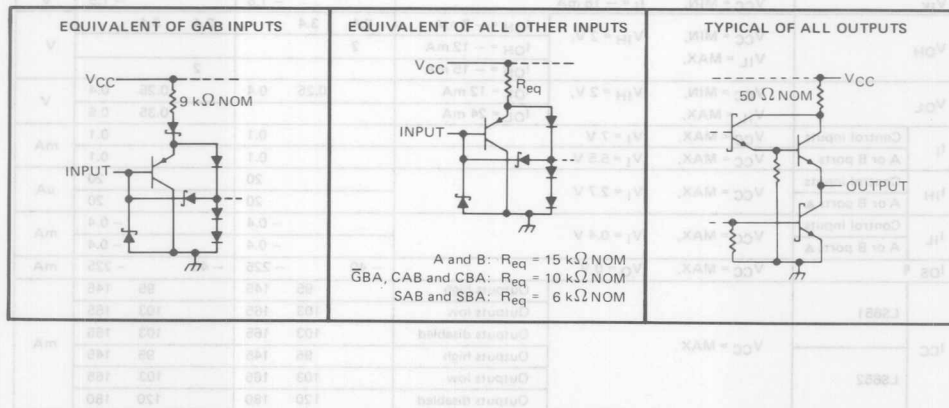
t_{PHZ} = output disable time from high level.

t_{PLZ} = output disable time from low level.

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs



3
TTL DEVICES

TYPES SN54LS653, SN54LS654, SN74LS653, SN74LS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and A I/O ports	7 V
B I/O ports	5.5 V
Operating free-air temperature range: SN54LS653, SN54LS654	– 55°C to 125°C
SN74LS653, SN74LS654	0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

			SN54LS653 SN54LS654			SN74LS653 SN74LS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			– 12			– 15	mA
I_{OL}	Low-level output current				12			24	mA
t_W	Pulse duration	CBA or CAB high		15			15		ns
		CBA or CAB low		30			30		
		Data high or low		30			30		
t_{su}	Setup time before CAB † or CBA †	A or B		15			15		ns
t_h	Hold time after CAB † or CBA †	A or B		0			0		ns
T_A	Operating free-air temperature			– 55	125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54LS653 SN54LS654			SN74LS653 SN74LS654			UNIT
			MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	B ports	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$							V
		$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		
		$I_{OH} = -12 \text{ mA}$	2						
I_{OH}	A ports	$I_{OH} = -15 \text{ mA}$				2			mA
		$V_{CC} = \text{MIN}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$							V
		$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
I_{OL}		$I_{OL} = 24 \text{ mA}$					0.35	0.5	mA
		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	
I_I	Control inputs A or B ports	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1			0.1	mA
		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	
I_{IH}	Control inputs A or B ports ▲	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			20			20	μA
		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	
I_{IL}	Control inputs A or B ports ▲	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	
$I_{OS} ¶$	B ports	$V_{CC} = \text{MAX}, V_O = 0 \text{ V}$	– 40		– 225	– 40		– 225	mA
I_{CC}	LS653 LS654	$V_{CC} = \text{MAX}$							mA
					95			95	
					145			145	
					103			103	
					165			165	
					103			103	
I_{CC}	LS653 LS654	$V_{CC} = \text{MAX}$			95			95	mA
					145			145	
					105			105	
					170			170	
I_{CC}	LS653 LS654	$V_{CC} = \text{MAX}$			120			120	mA
					180			180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

¶ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

▲ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

TYPES SN54LS653, SN54LS654, SN74LS653, SN74LS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LS653			LS654			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	CBA	A Bus	RL = 667 Ω, See Note 2	CL = 45 pF,	25	38	22	33	ns	
tPHL					26	39	24	36		
tPLH	CAB	B Bus			15	23	14	21	ns	
tPHL					24	36	22	33		
tPLH	A Bus	B Bus			10	18	10	18	ns	
tPHL					20	30	20	30		
tPLH	B Bus	A Bus			21	32	18	27	ns	
tPHL					16	24	14	21		
tPLH	SBA† (with B high)	A Bus			38	57	32	48	ns	
tPHL					26	39	21	32		
tPLH	SBA† (with B low)	A Bus			34	51	36	54	ns	
tPHL					23	35	19	29		
tPLH	SAB† (with A high)	B Bus			32	48	23	35	ns	
tPHL					22	33	18	27		
tPLH	SAB† (with A low)	B Bus			24	36	30	45	ns	
tPHL					20	30	14	21		
tPLH	GBA	A Bus			23	35	23	35	ns	
tPHL					37	55	35	53		
tPZH	GAB	B Bus			19	29	19	29	ns	
tPZL					25	38	22	33		
tPHZ	GAB	B Bus			26	39	26	39	ns	
tPLZ					19	29	19	29		

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs

EQUIVALENT OF GAB INPUTS	EQUIVALENT OF ALL OTHER INPUTS	TYPICAL OF B OUTPUTS	TYPICAL OF A OUTPUTS
	<p>A and B: $R_{eq} = 15\text{ k}\Omega\text{ NOM}$ GAB, CAB and CBA: $R_{eq} = 10\text{ k}\Omega\text{ NOM}$ SAB and SBA: $R_{eq} = 6\text{ k}\Omega\text{ NOM}$</p>		

TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

D2351, APRIL 1977—REVISED APRIL 1985

'LS668 ... SYNCHRONOUS UP/DOWN DECADE COUNTERS 'LS669 ... SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	32 MHz	32 MHz	100 mW

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

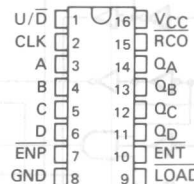
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (\bar{P} and \bar{T}) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input \bar{T} is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse when the count is maximum counting up or zero counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable \bar{P} or \bar{T} inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable \bar{P} , enable \bar{T} , load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL} , and all buffered outputs.

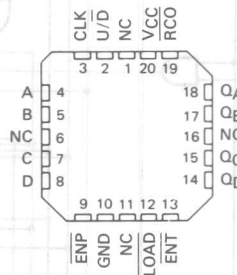
SN54LS668, SN54LS669 ... J PACKAGE SN74LS668, SN74LS669 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS668, SN54LS669 ... FK PACKAGE SN74LS668, SN74LS669

(TOP VIEW)



NC — No internal connection

3

TTL DEVICES

PRODUCTION DATA

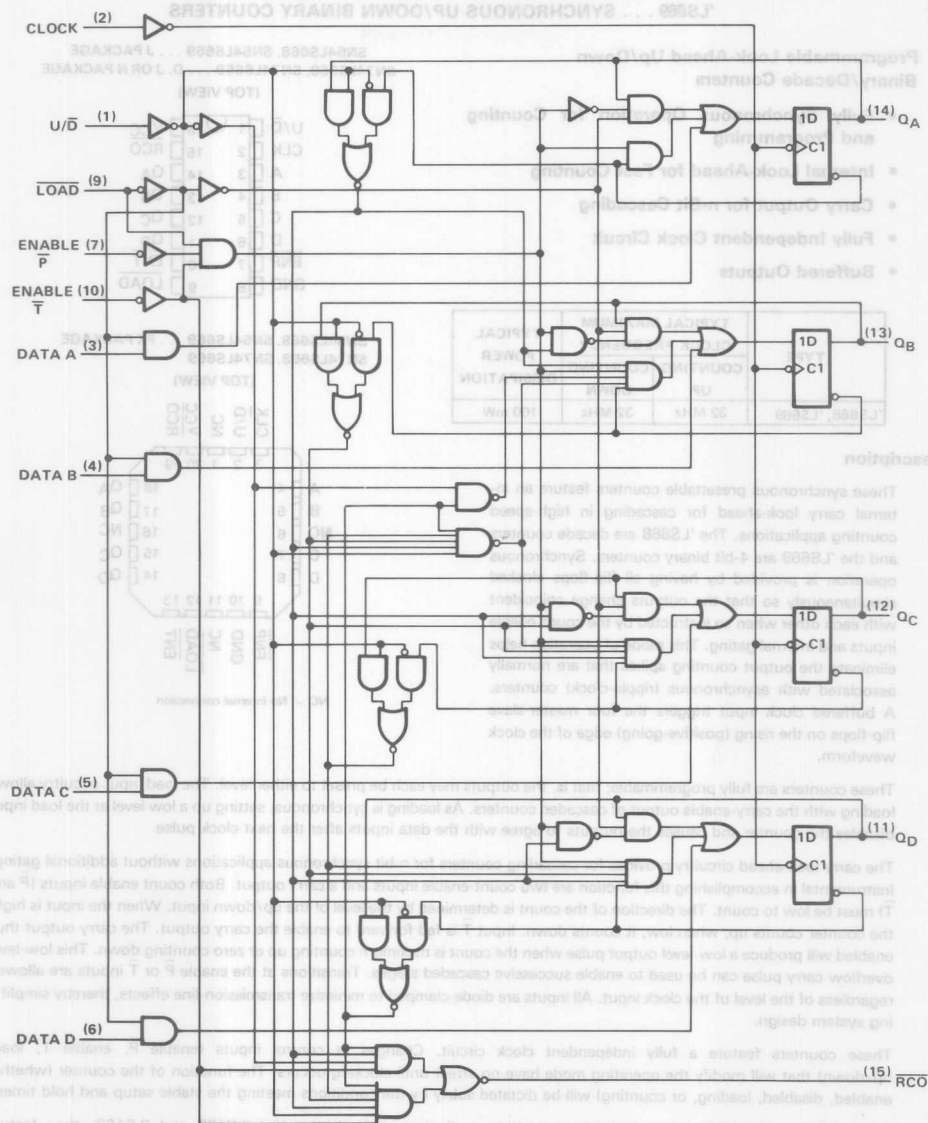
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3-1107

logic diagram

SN54LS668, SN74LS668, DECADE COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

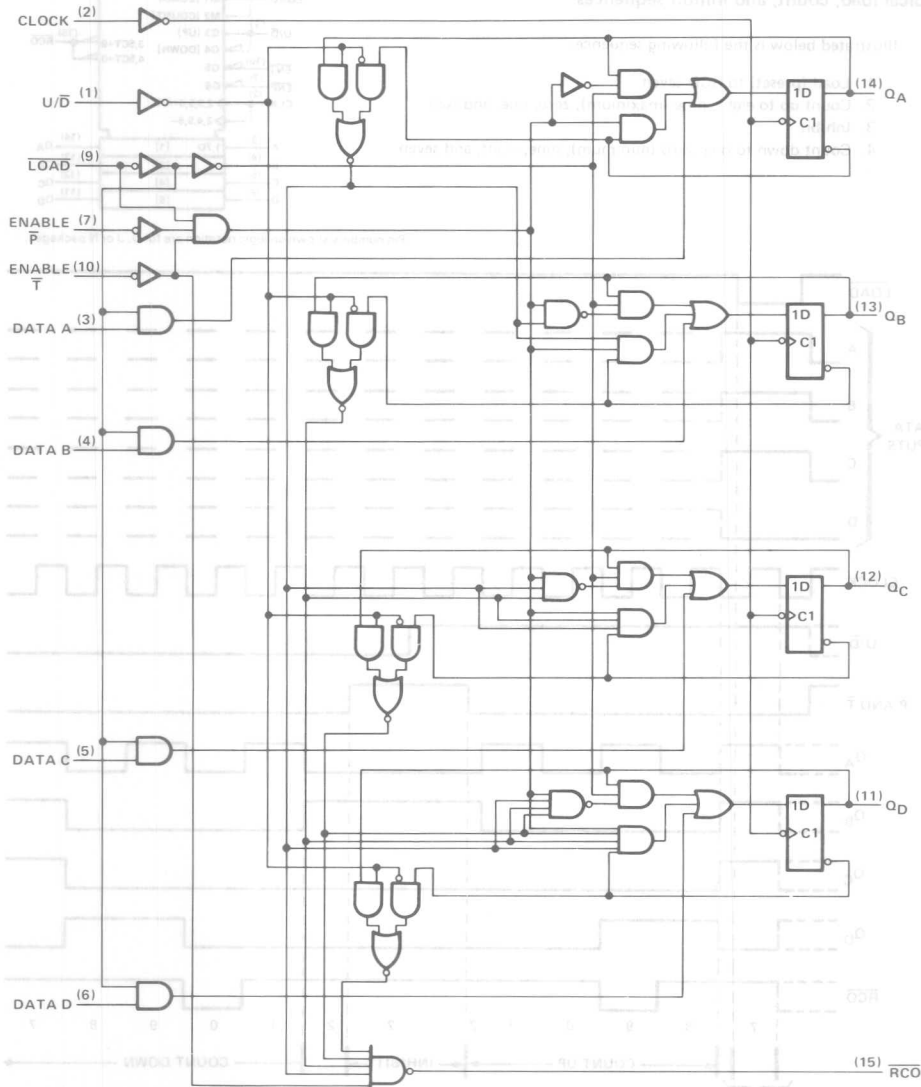
3

TTL DEVICES

TYPES SN54LS669, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

logic diagram (continued)

SN54LS669, SN74LS669, BINARY COUNTERS



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54LS668, SN74LS668 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

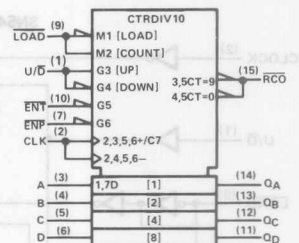
'LS668 DECADE COUNTERS

logic symbol

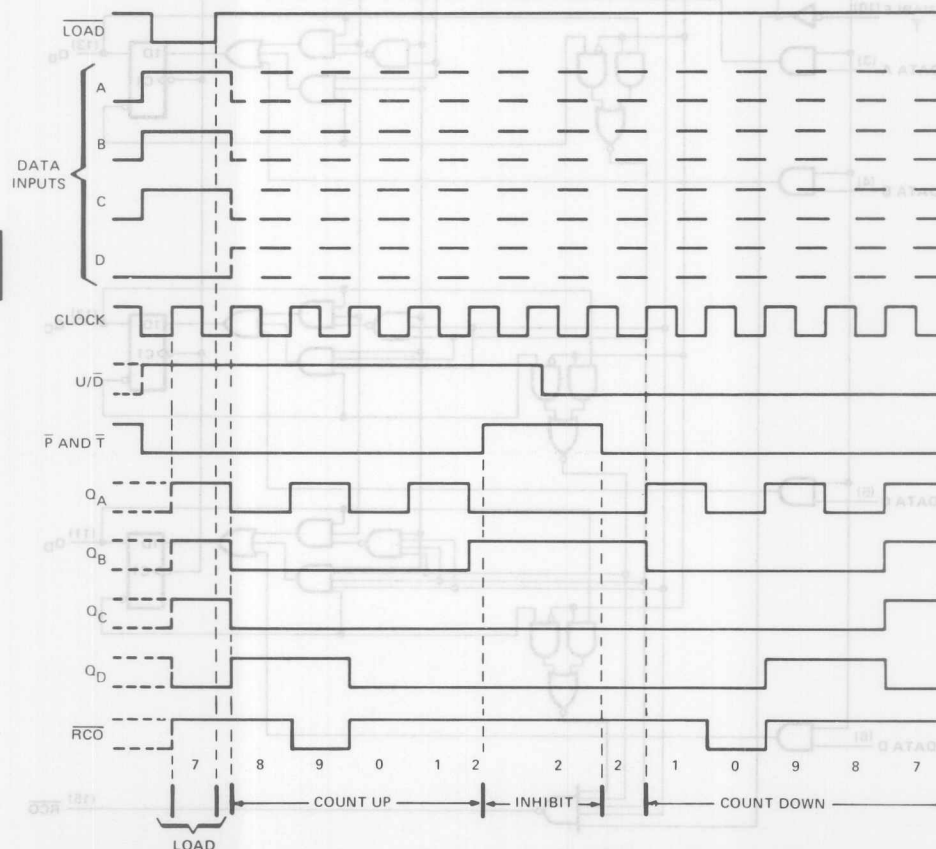
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



Pin numbers shown on logic notation are for D, J or N packages.



3

TTL DEVICES

TYPES SN54LS669, SN74LS669 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

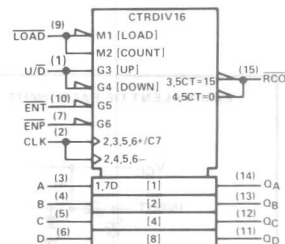
'LS669 BINARY COUNTERS

typical load, count, and inhibit sequences

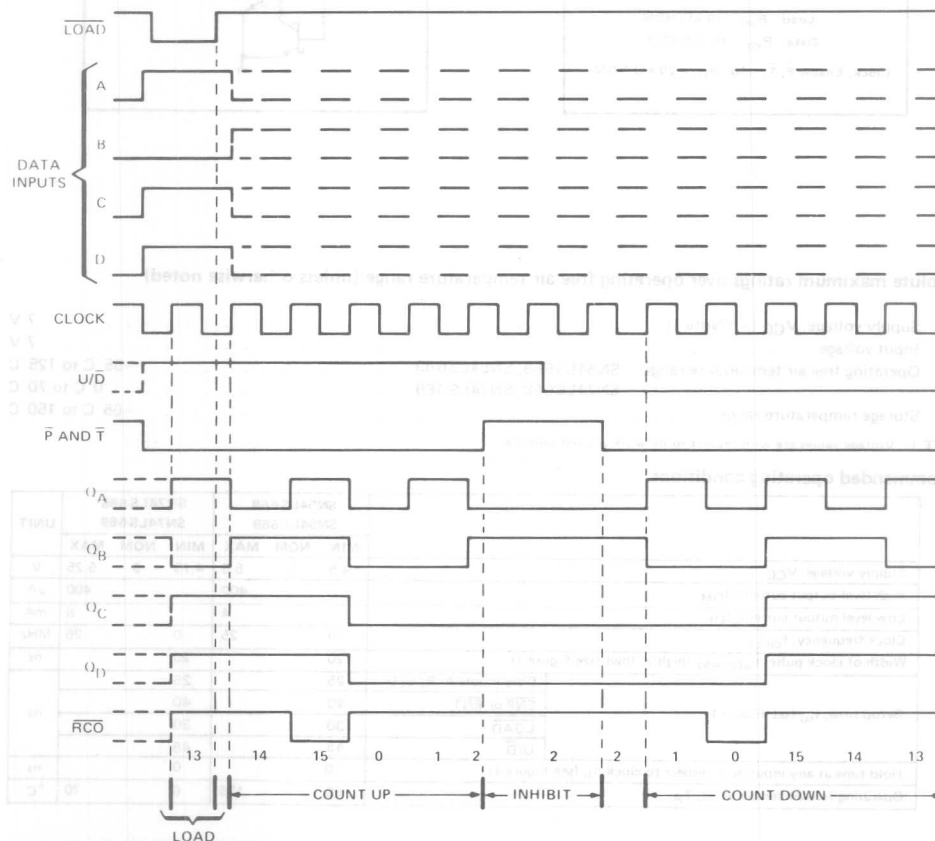
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen

logic symbol



Pin numbers shown on logic notation are for D, J or N packages

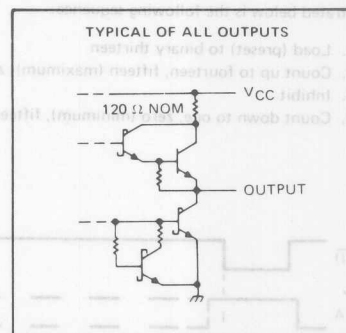
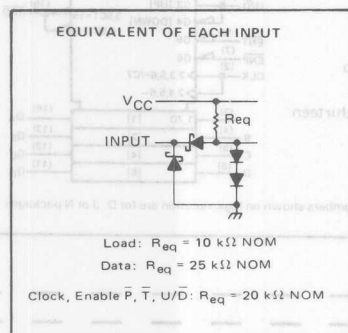


3

TTL DEVICES

TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

schematics of inputs and outputs



3

TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS668, SN54LS669	-55°C to 125°C
SN74LS668, SN74LS669	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			400			400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)	20			20			ns
Setup time, t_{SU} (see Figure 1)	Data inputs A, B, C, D	25		25			ns
	ENP or ENT	40		40			
	LOAD	30		30			
	U/D	45		45			
Hold time at any input with respect to clock, t_H (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage			0.7			0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 4 mA	0.25	0.4		0.25	0.4		V
		I _{OL} = 8 mA				0.35	0.5		V
I _I	Input current at maximum input voltage	A, B, C, D, \bar{P} , U/ \bar{D} Clock, \bar{T} LOAD V _{CC} = MAX, V _I = 7 V		0.1			0.1		mA
				0.1			0.1		
I _{IH}	High-level input current	A, B, C, D, \bar{P} , U/ \bar{D} Clock, \bar{T} LOAD V _{CC} = MAX, V _I = 2.7 V		20			20		µA
				20			20		
I _{IL}	Low-level input current	A, B, C, D, \bar{P} , U/ \bar{D} Clock, \bar{T} LOAD V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4		mA
				-0.4			-0.4		
I _{OS}	Short-circuit output current‡	V _{CC} = MAX	-20	-100		-20	-100		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 2	20	34		20	34		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				25	32		MHz
t _{PLH}	CLK	RCO	C _L = 15 pF, R _L = 2 kΩ, See Figures 2 and 3	26	40		ns
t _{PHL}		Any		40	60		
t _{PLH}	CLK	Q		18	27		ns
t _{PHL}		RCO		18	27		
t _{PLH}	ENT	RCO		11	17		ns
t _{PHL}		RCO		29	45		
t _{PLH}	U/ \bar{D}	RCO		22	35		ns
t _{PHL}		RCO		26	40		

* f_{max} Maximum clock frequency

t_{PLH} propagation delay time, low to high level output.

t_{PHL} propagation delay time, high to low level output.

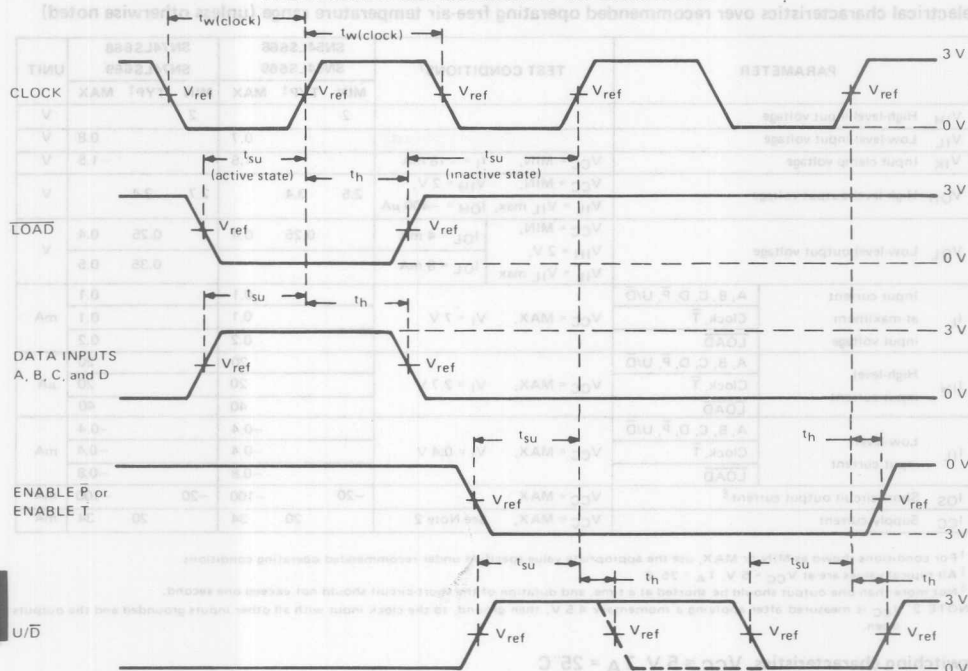
† Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.

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TTL DEVICES

TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

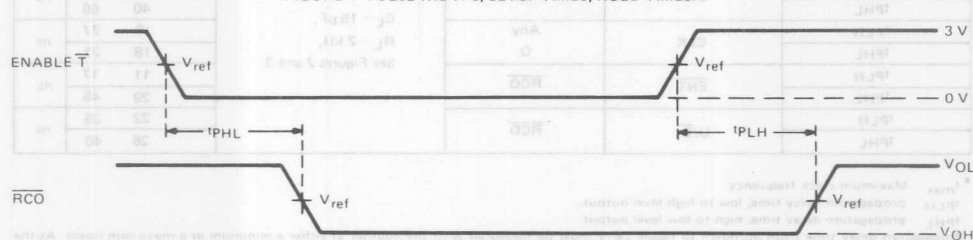
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≥ 1 MHz, duty cycle $\geq 50\%$, $Z_{out} \geq 50 \Omega$, $t_r = 15$ ns, $t_f = 6$ ns.
B. $V_{ref} = 1.3$ V.

FIGURE 1—PULSE WIDTHS, SETUP TIMES, HOLD TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≥ 1 MHz, duty cycle $\geq 50\%$, $Z_{out} \geq 50 \Omega$, $t_r = 15$ ns, $t_f = 6$ ns.
B. t_{PLH} and t_{PHL} from enable \bar{T} input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'LS668, all Q outputs high for 'LS669).
C. $V_{ref} = 1.3$ V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

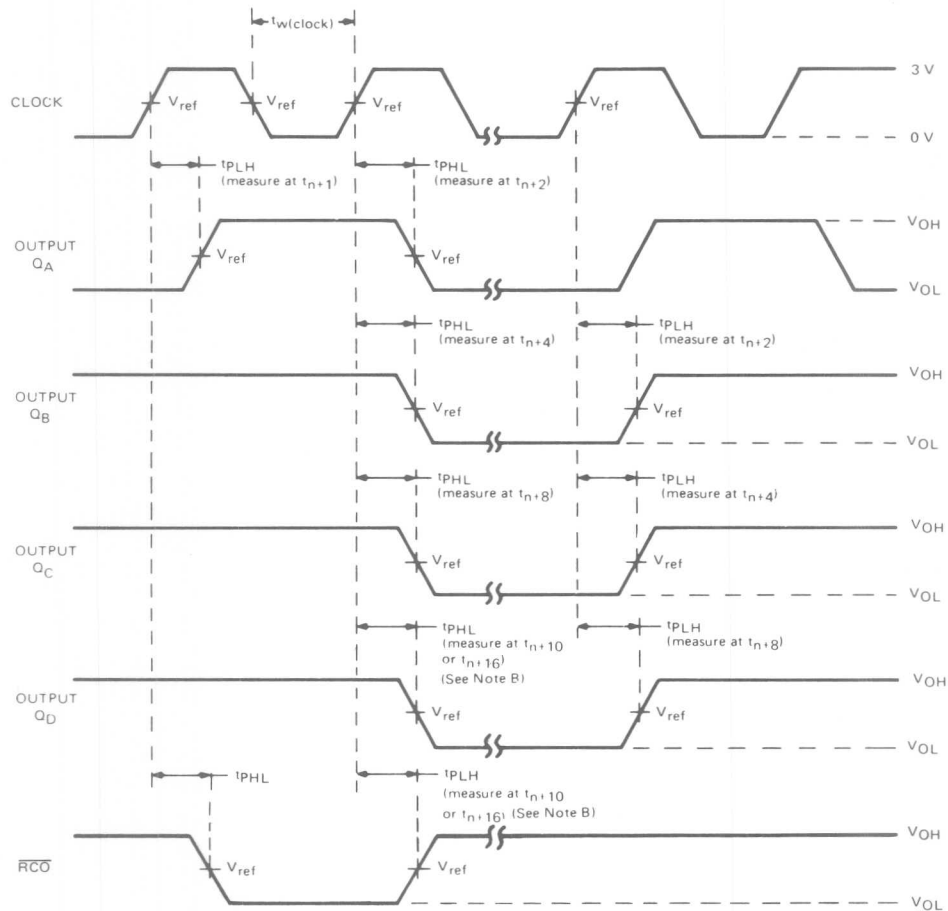
FIGURE 2—PROPAGATION DELAY TIMES TO CARRY OUTPUT

3

TTL DEVICES

TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

PARAMETER MEASUREMENT INFORMATION



3

TTL DEVICES

UP-COUNT VOLTAGE WAVEFORMS

- NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $Z_{OUT} \approx 50 \Omega$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$. Vary PRR to measure t_{max} .
B. Outputs Q_D and carry are tested at t_{N+10} for the 'LS668, and at t_{N+16} for the 'LS669, where t_N is the bit-time when all outputs are low.
C. $V_{ref} = 1.3 \text{ V}$.

FIGURE 3—PROPAGATION DELAY TIMES FROM CLOCK

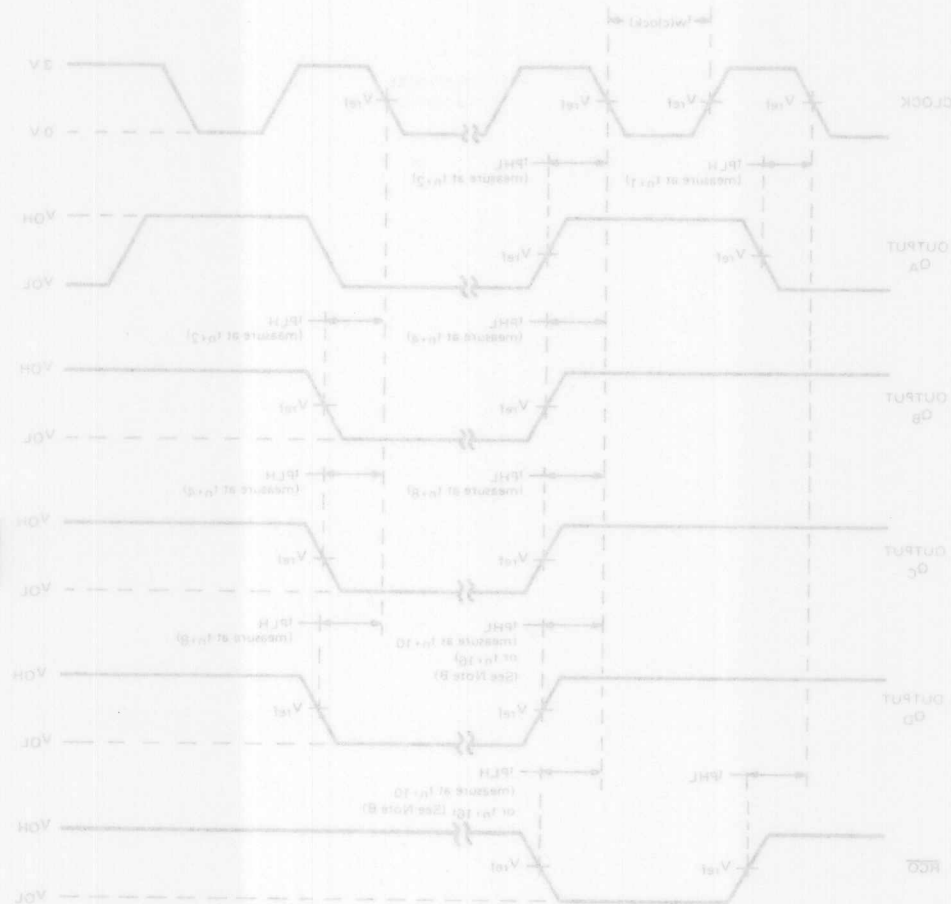


FIGURE 3-PROPAGATION DELAY TIMES FROM CLOCK

NOTES: A. The output signal is shown as a square wave having the following characteristics: $f_{CLK} = 1 \text{ MHz}$, duty cycle = 50%, $t_{CLK} = 50 \text{ ns}$, $V_{OH} = 1.5 \text{ V}$, $V_{OL} = 0 \text{ V}$, $V_{IH} = 1.5 \text{ V}$, $V_{IL} = 0 \text{ V}$.
 B. Outputs A, B, C, and D are shown as square waves. The output signal is shown as a square wave having the following characteristics: $f_{CLK} = 1 \text{ MHz}$, duty cycle = 50%, $t_{CLK} = 50 \text{ ns}$, $V_{OH} = 1.5 \text{ V}$, $V_{OL} = 0 \text{ V}$, $V_{IH} = 1.5 \text{ V}$, $V_{IL} = 0 \text{ V}$.
 C. $V_{OH} = 1.5 \text{ V}$, $V_{OL} = 0 \text{ V}$.

TYPES SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

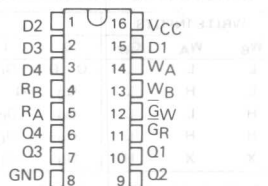
BULLETIN NO. DL-S 7612122, MARCH 1974-REVISED DECEMBER 1983

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- For Use as:
Scratch-Pad Memory
Buffer Storage between Processors
Bit Storage in Fast Multiplication Designs

- 3-State Outputs
- SN54LS170 and SN74LS170 Are Similar But Have Open-Collector Outputs

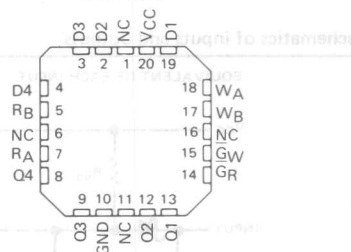
SN54LS670 . . . J OR W PACKAGE
SN74LS670 . . . D, J OR N PACKAGE

(TOP VIEW)



SN54LS670 . . . FK PACKAGE
SN74LS670

(TOP VIEW)



NC — No internal connection.

description

The SN54LS670 and SN74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, \overline{GW} , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, \overline{GR} , is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement — data-entry addressing separate from data-read addressing and individual sense line — eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be bus connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54LS670 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS670 is characterized for operation from 0°C to 70°C .

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-1117

3

TTL DEVICES

TYPES SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-OUTPUTS

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

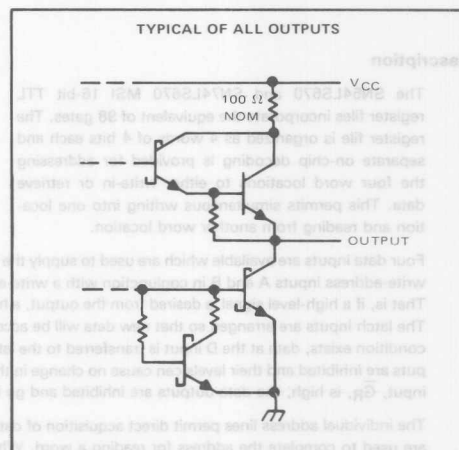
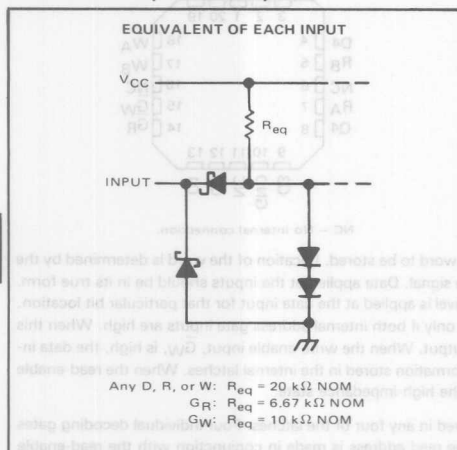
WRITE INPUTS			WORD			
\overline{W}_B	\overline{W}_A	\overline{G}_W	0	1	2	3
L	L	L	$Q = D$	Q_0	Q_0	Q_0
L	H	L	Q_0	$Q = D$	Q_0	Q_0
H	L	L	Q_0	Q_0	$Q = D$	Q_0
H	H	L	Q_0	Q_0	Q_0	$Q = D$
X	X	H	Q_0	Q_0	Q_0	Q_0

- NOTES:
- H = high level, L = low level, X = irrelevant, Z = high impedance (off)
 - $(Q = D)$ = The four selected internal flip flop outputs will assume the states applied to the four external data inputs.
 - Q_0 = the level of Q before the indicated input conditions were established.
 - W0B1 = The first bit of word 0, etc.

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
\overline{R}_B	\overline{R}_A	\overline{G}_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

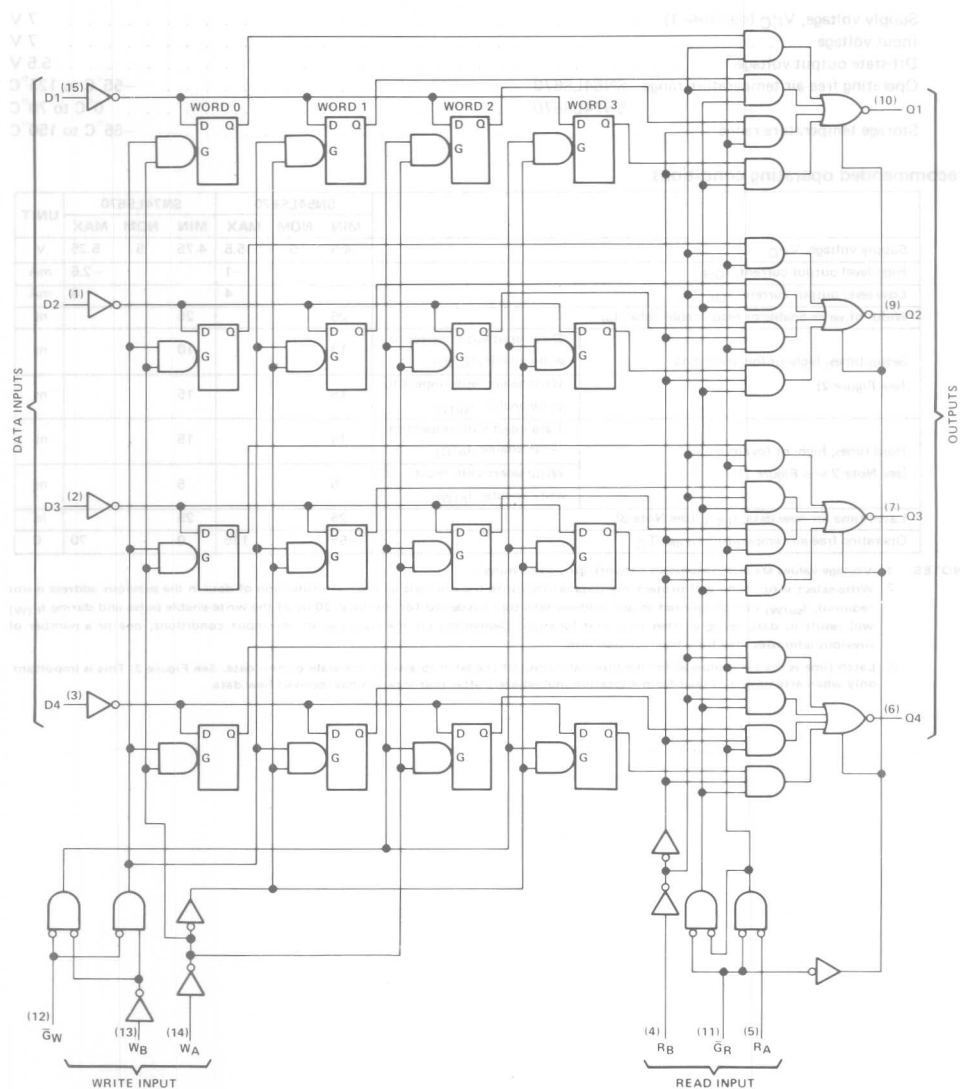
schematics of inputs and outputs



3 TTL DEVICES

TYPES SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

TYPES SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

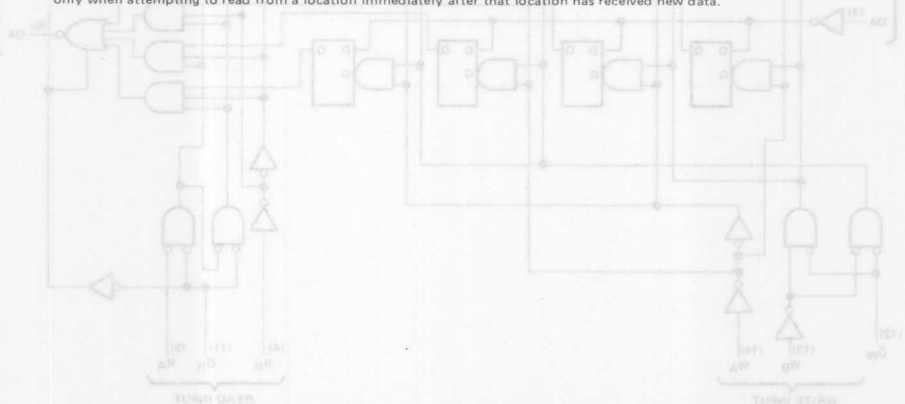
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS670	-55°C to 125°C
SN74LS670	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54LS670			SN74LS670			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-1			-2.6	mA
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_W		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su}(D)$	10			10			ns
	Write select with respect to write enable, $t_{su}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_h(D)$	15			15			ns
	Write select with respect to write enable, $t_h(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temperature range, T_A		-55		125	0		70	°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_h(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.



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TTL DEVICES

TYPES SN54LS670, SN74LS670
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS670			SN74LS670			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.7			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -1 mA V _{IL} = V _{IL} max I _{OH} = -2.6 mA	2.4	3.4		2.4	3.1		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA V _{IL} = V _{IL} max I _{OL} = 8 mA		0.25	0.4		0.25	0.4	V
I _{OZH} Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V			20			20	μA
I _{OZL} Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-20			-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V	Any D, R, or W		0.1			0.1	mA
		\overline{G}_W		0.2			0.2	
		\overline{G}_R		0.3			0.3	
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V	Any D, R, or W		20			20	μA
		\overline{G}_W		40			40	
		\overline{G}_R		60			60	
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V	Any D, R, or W		-0.4			-0.4	mA
		\overline{G}_W		-0.8			-0.8	
		\overline{G}_R		-1.2			-1.2	
I _{OS} Short-circuit output current [§]	V _{CC} = MAX	-30		-130	-30		-130	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 4		30	50		30	50	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Read select	Any Q	C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 2	23	40		ns
t _{PHL}				25	45		
t _{PLH}	Write enable	Any Q	C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 3	26	45		ns
t _{PHL}				28	50		
t _{PLH}	Data	Any Q		25	45		ns
t _{PHL}				23	40		
t _{PZH}	Read enable	Any Q	C _L = 15 pF, R _L = 2 kΩ, See Figures 1 and 4	15	35		ns
t _{PZL}				22	40		
t _{PHZ}				30	50		
t _{PLZ}			C _L = 5 pF, R _L = 2 kΩ, See Figures 1 and 4	16	35		ns

[†]t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

TYPES SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

UNIT	MIN	TYP	MAX	TEST POINT	PARAMETER
V	0.0	0.0	0.0	V _{CC}	V _{ih} High-level input voltage
V	0.0	0.0	0.0	V _{CC}	V _{il} Low-level input voltage
V	0.0	0.0	0.0	V _{CC}	V _{oh} High-level output voltage
V	0.0	0.0	0.0	V _{CC}	V _{ol} Low-level output voltage
A	0.0	0.0	0.0	V _{CC}	I _{oh} High-level output current
A	0.0	0.0	0.0	V _{CC}	I _{ol} Low-level output current
A	0.0	0.0	0.0	V _{CC}	I _{cc} Supply current
A	0.0	0.0	0.0	V _{CC}	I _q Standby current

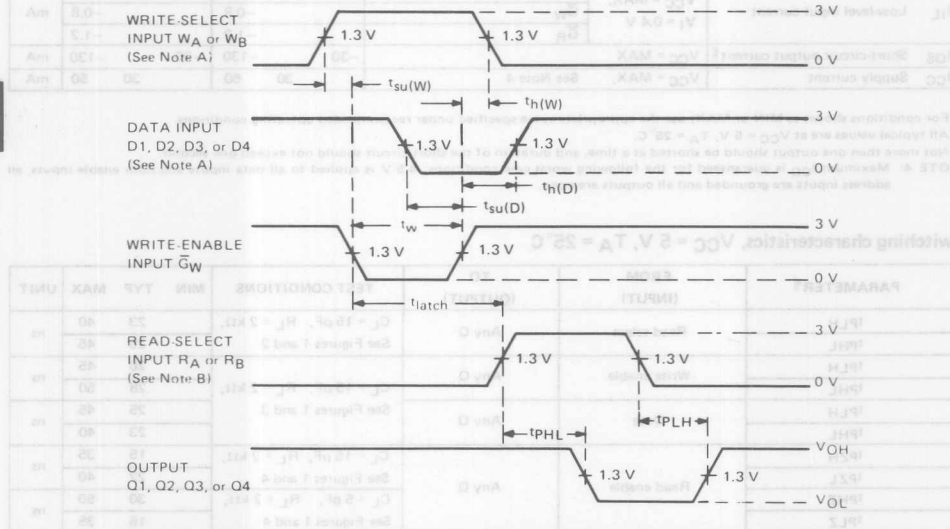
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.

LOAD CIRCUIT

FIGURE 1

3

TTL DEVICES



VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

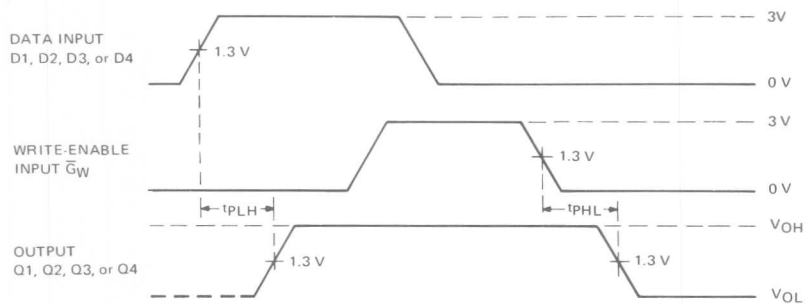
NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: PRR \approx 2 MHz, Z_{out} \approx 50 Ω , duty cycle \approx 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

FIGURE 2

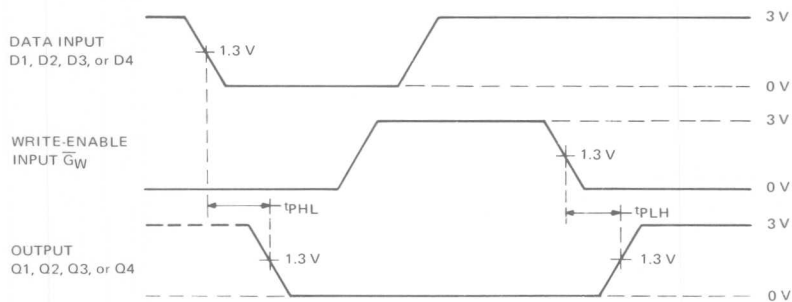
TYPES SN54LS670, SN74LS670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



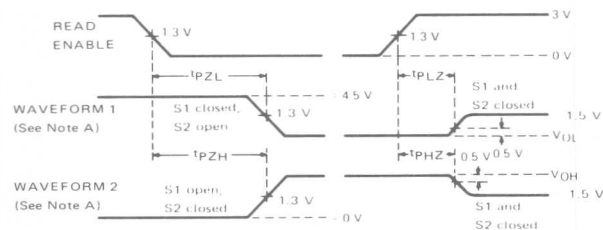
VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

- NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
B. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

FIGURE 3

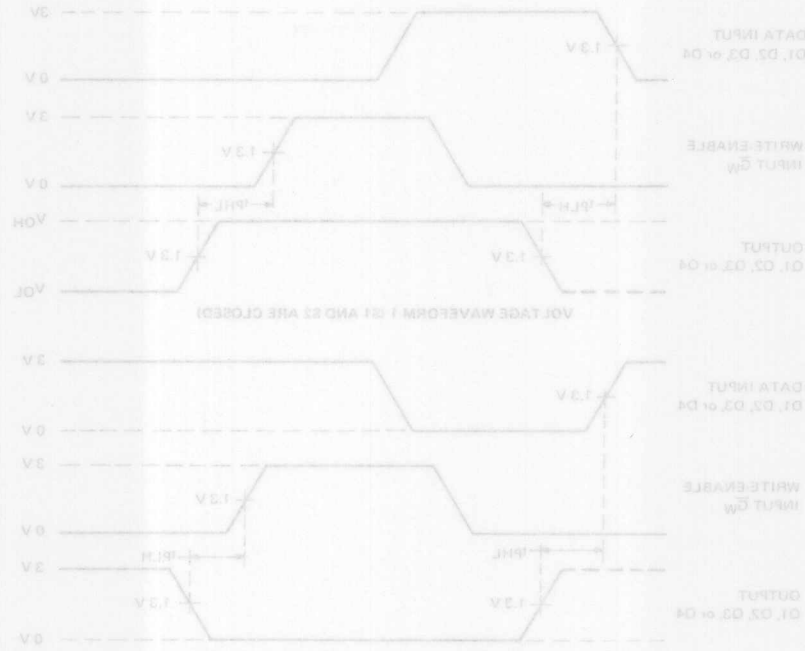


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the read enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read enable input.
B. When measuring delay times from the read enable input, both read select inputs have been established at steady states.
C. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

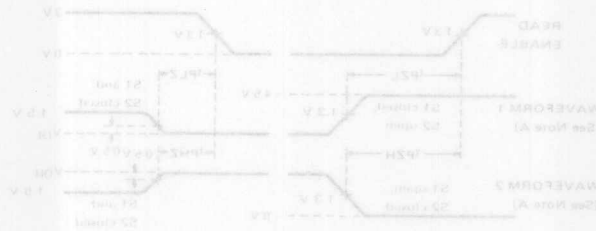
FIGURE 4

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Each signal address is tested. Prior to the start of each of the above tests both write and read address inputs are registered with WE = 0 and WE = 1. During the test Q is 0.
B. Input waveforms are supplied by generators having the following characteristics: $f_{CLK} < 1 \text{ MHz}$, $t_{SETUP} = 50 \text{ ns}$, data rate $< 50 \text{ ns}$, $V_{CC} = 5 \text{ V}$, $V_{EE} = 0 \text{ V}$.
C. Input waveforms are supplied by generators having the following characteristics: $f_{CLK} < 1 \text{ MHz}$, $t_{SETUP} = 50 \text{ ns}$, data rate $< 50 \text{ ns}$, $V_{CC} = 5 \text{ V}$, $V_{EE} = 0 \text{ V}$.

FIGURE 3



VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low when disabled by the read enable signal. Waveform 2 is for an output with internal conditions such that the output is high when disabled by the read enable signal.
B. When measuring delay times from the read enable input, both read and write inputs have been established as steady state.
C. Input waveforms are supplied by generators having the following characteristics: $f_{CLK} < 1 \text{ MHz}$, $t_{SETUP} = 50 \text{ ns}$, data rate $< 50 \text{ ns}$, $V_{CC} = 5 \text{ V}$, $V_{EE} = 0 \text{ V}$.

FIGURE 4

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672 4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

D2638, JANUARY 1981

- 4-Bit Universal Shift Registers/Latches
- Multiplexed Outputs for Shift Register or Latched Data
- Choice of Direct SR Clear ('LS671) or Synchronous SR Clear ('LS672)
- 3-State Outputs Drive Bus Lines Directly
- Expandable to Any Word Length

description

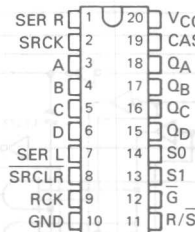
The 'LS671 and 'LS672 each contain a 4-bit universal shift register (similar to the 'LS194A) and a 4-bit storage register (similar to the 'LS175) multiplexed to a 3-state output stage (similar to the 'LS258). The user has the option of selecting the shift or storage register via the register/shift select input R/ \bar{S} . The 'LS671 has a direct-overriding shift register clear while the 'LS672 features a synchronous shift register clear. The shift register has four distinct modes of operation, namely:

- Inhibit clock (do nothing)
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Parallel (broadside) load

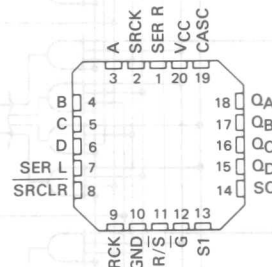
A cascade output for the shift register is provided so that full shift register functionality is provided even while the outputs are in the high-impedance mode. The cascade output presents Q_A data in the shift-left mode, Q_D data in the shift-right mode.

Both the shift register clock and the latch clock are triggered on the positive transition. The output control (\bar{G}) activates Q_A thru Q_D when low, it places Q_A thru Q_D into the high-impedance state when high.

SN54LS671, SN54LS672 ... J PACKAGE
SN74LS671, SN74LS672 ... DW, J OR N PACKAGE
(TOP VIEW)



SN54LS671, SN54LS672 ... FK PACKAGE
SN74LS671, SN74LS672
(TOP VIEW)



3

TTL DEVICES

PRODUCTION DATA

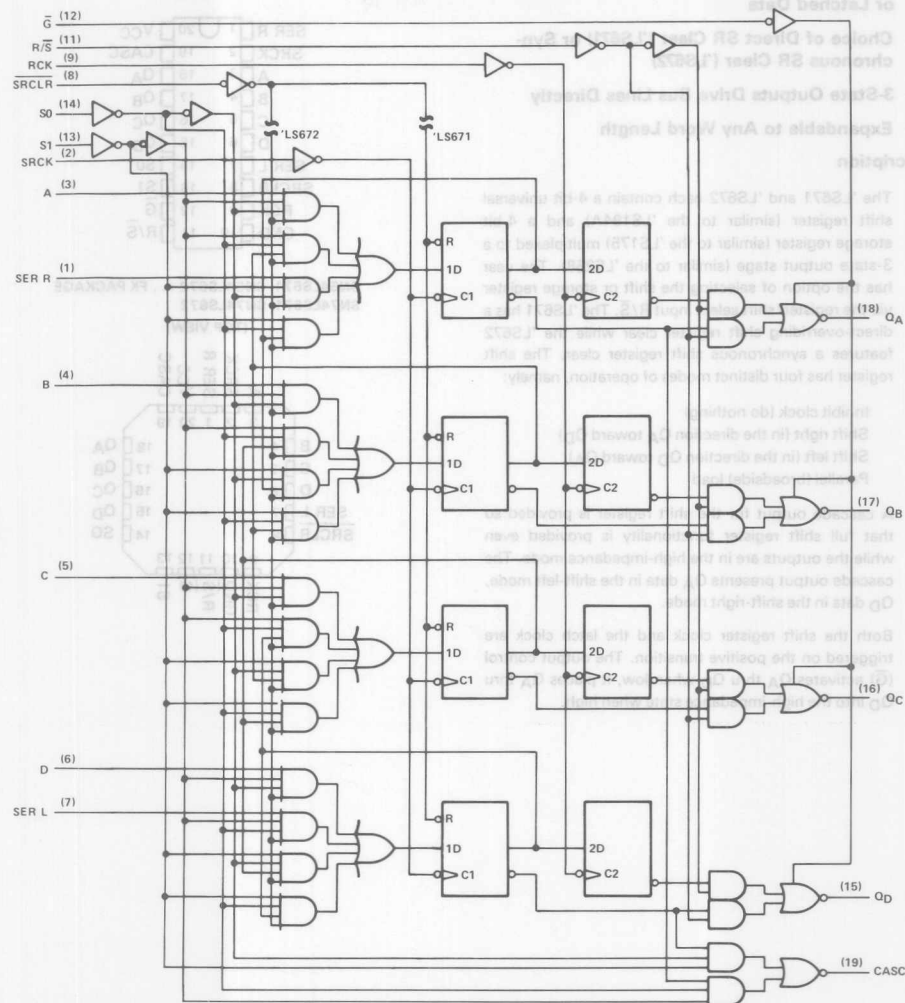
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-1125

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672 4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

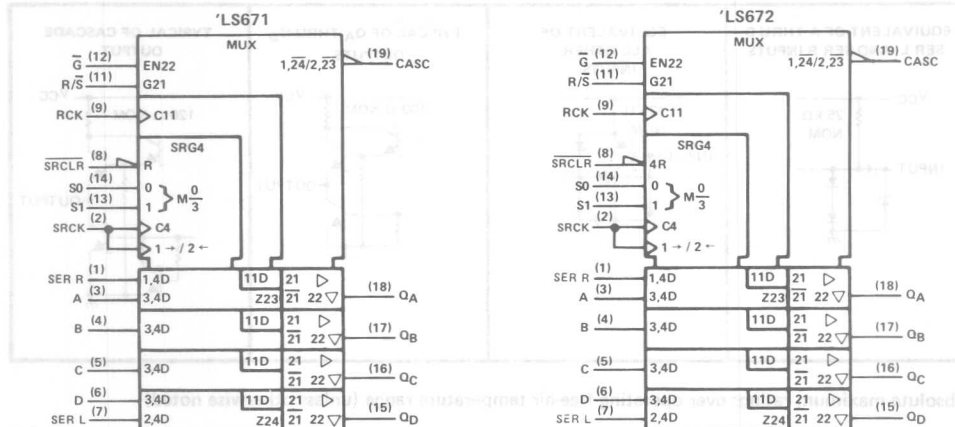
3

TTL DEVICES

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672

4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

FUNCTION TABLE

\bar{G}	R/\bar{S}	$SRCLR$	SR MODE		SRCK		SERIAL INPUTS		PARALLEL INPUTS				PARALLEL OUTPUTS				CASC*
			S1	S0	'LS671	'LS672	SL	SR	A	B	C	D	QA	QB	QC	QD	
L	L	L	X	X	X	†	X	X	X	X	X	X	L	L	L	L	(*)
L	L	H	X	X	L	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0	(*)
L	L	H	L	H	†	†	X	H	X	X	X	X	QA0	QB0	QC0	QD0	H
L	L	H	L	H	†	†	X	H	X	X	X	X	H	QAn	QBn	QCn	QCn
L	L	H	L	H	†	†	X	L	X	X	X	X	L	QAn	QBn	QCn	QCn
L	L	H	H	L	†	†	H	X	X	X	X	X	QBn	QCn	QDn	H	QBn
L	L	H	H	L	†	†	L	X	X	X	X	X	QBn	QCn	QDn	L	QBn
L	L	H	H	H	†	†	X	X	a	b	c	d	a	b	c	d	H
H	X	X	L	H	†	†	X	X	X	X	X	X	Z	Z	Z	Z	QCn
H	X	X	H	L	†	†	X	X	X	X	X	X	Z	Z	Z	Z	QBn
L	H	X	X	X	X	X	X	X	X	X	X	X	Internal register contents				(*)

When the output control \bar{G} is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the shift register and the output at CASC are not affected.

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

† = transition from low to high level

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively

QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established

QAn, QBn, QCn = the level of QA, QB, or QC, respectively, before the most-recent transition of the clock

Z = high-impedance state

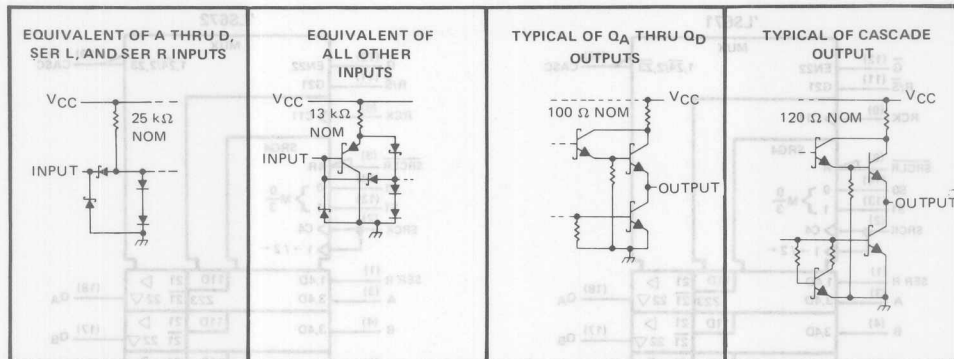
*The cascade output displays the D bit of the shift register in mode 1 (S1, S0 = L, H), the A bit in mode 2 (S1, S0 = LL), and is inactive (H) in modes 0 and 3 (S1, S0 = LL and HH).

3

TTL DEVICES

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672 4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS671, SN54LS672	-55°C to 125°C
SN74LS671, SN74LS672	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'				SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
I _{OH}	High-level output current	-0.4			-0.4			mA	
	Cascade out				-1				
	Q _A , Q _B , Q _C , Q _D				-2.6				
I _{OL}	Low-level output current	4			8			mA	
	Q _A , Q _B , Q _C , Q _D	12			24				
t _W	Width of SRCK, RCK, or SRCLR ('LS671 only) input pulse	30			30			ns	
t _{SU}	Inactive state setup time	30			30			ns	
t _{SU}	Setup time	SRCLR before SRCK ↑ ('LS671 only)	45		45			ns	
		S0 or S1 to SRCK ↑	25		25				
		SRCLR ↓ ('LS672 only) to SRCK ↑	30		30				
		A, B, C, D to SRCK ↑	30		30				
		SRCK ↑ to RCK ↑	30		30				
	SER to SRCK ↑	35		35					
t _H	Hold time	0			0			ns	
T _A	Operating free-air temperature	- 55		125	0		70	°C	

3

TTL DEVICES

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672 4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS*		SN74LS*		UNIT		
				MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IH}	High-level input voltage			2			2	V		
V _{IL}	Low-level input voltage					0.7		0.8 V		
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA				-1.5		-1.5 V		
V _{OH}	High-level output voltage	Q _A - Q _D	V _{CC} = MIN, I _{OH} = -1 mA	2.4	3.1			V		
		Q _A - Q _D	V _{IH} = 2 V, I _{OH} = -2.6 mA			2.4	3.1			
		CASC	V _{IL} = V _{IL max} , I _{OH} = -400 μA	2.5	3.2		2.7		3.2	
V _{OL}	Low-level output voltage	Q _A - Q _D	V _{CC} = MIN, I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		Q _A - Q _D	V _{IH} = 2 V, I _{OL} = 24 mA					0.35	0.5	
		CASC	V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	
		CASC	I _{OL} = 8 mA					0.35	0.5	
I _{OZH}	Off-state output current, high-level voltage applied	Q _A - Q _D	V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V, V _{IL} = V _{IL max}			20		20	μA	
I _{OZL}	Off-state output current, low-level voltage applied	Q _A - Q _D	V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V, V _{IL} = V _{IL max}			-20		-20	μA	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1		0.1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				20		20	μA	
I _{IL}	Low-level input current	A, B, C, D	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA	
		All others				-0.2		-0.2		
I _{OS}	Short-circuit output current§	Q _A - Q _D	V _{CC} = MAX, V _O = 0 V			-30	-130	-130	mA	
		CASC				-20	-100	-20		-100
I _{CC}	Supply current	All outputs low	V _{CC} = MAX,	See Note 2		35	70	35	70	mA
		All outputs high	All outputs open	See Note 3		30	65	30	65	
		Q _A thru Q _D , at Hi-Z	See Note 4		37	70	37	70		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

- NOTES: 2. I_{CCL} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SRCK and RCK while S0 is at 4.5 V and all other inputs are grounded.
3. I_{CCH} is tested after two 4.5-V to 0-V to 4.5-V pulses have been applied to SRCK and RCK while all other inputs are at 4.5 V.
4. I_{CCZ} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SRCK and RCK while S0 and \bar{G} are at 4.5 V and all other inputs are grounded.



FIGURE 1. SN54LS671, SN74LS671 (13-PIN PACKAGE)

Any desired word length may be obtained using the scheme shown. Connections to control pins of all the packages are tied in common, e.g., all GND pins are connected together, all ST pins are connected together, etc.

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672 4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, see note 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS671			'LS672			UNIT	
			MODE	LOAD	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	SRCK \uparrow	CASCADE	SHIFT LEFT OR RIGHT	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	31	45		31	45		ns	
t_{PHL}					14	25		14	25		ns	
t_{PLH}	S0, S1		SR CLEAR		11	20		12	20		ns	
t_{PHL}					11	20		12	20		ns	
t_{PLH}	SRCK \uparrow	$Q_A - Q_D$	SHIFT LEFT OR RIGHT	$R_L = 667\text{ }\Omega$, $C_L = 45\text{ pF}$	19	30		19	30		ns	
t_{PHL}	SRCLR \downarrow				10	20		10	20		ns	
t_{PLH}	SRCK \uparrow		SR LOAD		16	25		16	25		ns	
t_{PHL}					10	20		10	20		ns	
t_{PLH}			SR CLEAR		15	25		15	25		ns	
t_{PHL}					17	25		17	30		ns	
t_{PLH}	SRCLR \downarrow		LATCH		21	30		21	30		ns	
t_{PHL}	RCK \uparrow				10	20		10	20		ns	
t_{PLH}			MUX		15	25		15	25		ns	
t_{PHL}	R/ \bar{S} \uparrow				12	25		13	25		ns	
t_{PLH}			3-STATE ENABLE		15	25		15	25		ns	
t_{PHL}	R/ \bar{S} \downarrow				17	25		17	25		ns	
t_{PLH}			3-STATE DISABLE	$R_L = 667\text{ }\Omega$, $C_L = 5\text{ pF}$	16	25		16	25		ns	
t_{PHL}	\bar{G} \downarrow				16	25		16	25		ns	
t_{PLH}			3-STATE ENABLE		19	30		19	30		ns	
t_{PHL}	\bar{G} \uparrow				16	25		16	25		ns	
t_{PLZ}					16	25		16	25		ns	

NOTE 5: See General Information Section for load circuits and voltage waveforms.

t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 t_{PZH} = Output enable time to high level
 t_{PZL} = Output enable time to low level
 t_{PHZ} = Output disable time from high level
 t_{PLZ} = Output disable time from low level

TYPICAL APPLICATION DATA

The 'LS671 or 'LS672 can easily be expanded utilizing the cascade output and the SER L and SER R inputs. A typical expansion is shown below.

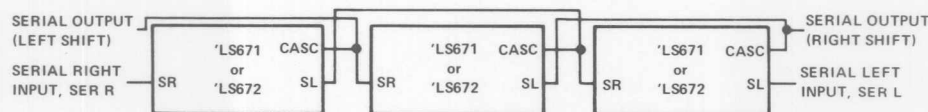


FIGURE 1 - 'LS671, 'LS672 EXPANDED TO 12 BITS, (3 PACKAGES)

Any desired word length may be obtained using the scheme shown. Corresponding control pins of all the packages are tied in common, i.e., all S0 pins are connected together, all S1 pins are connected together, etc.

TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

D2421, REVISED APRIL 1985

'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level (\overline{CS}) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

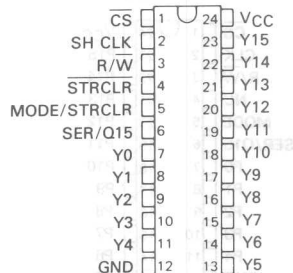
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

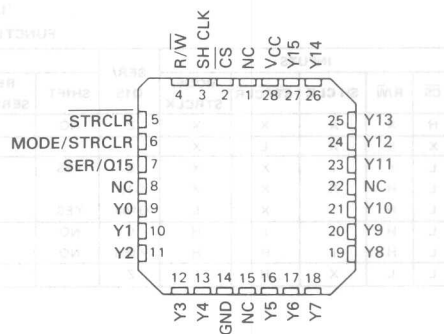
- 1) Hold (do nothing)
- 2) Write (serially via input/output)
- 3) Read (serially)
- 4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

SN54LS673 ... J OR W PACKAGE SN74LS673 ... DW, J OR N PACKAGE (TOP VIEW)



SN54LS673 ... FK PACKAGE SN74LS673 (TOP VIEW)



NC—No internal connection

FUNCTION	UNIT	STATE	MODE	DATA
Hold	0	0	0	0
Write	1	0	0	0
Read	0	1	0	0
Load	1	1	0	0

3

TTL DEVICES

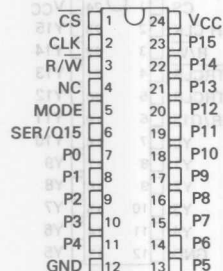
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TEXAS
INSTRUMENTS

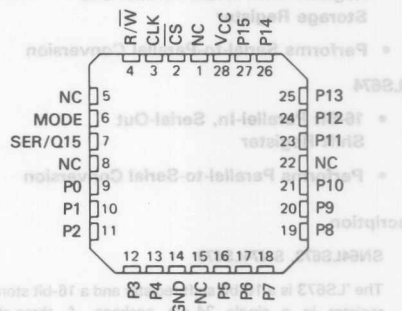
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TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SN54LS674 ... J OR W PACKAGE
SN74LS674 ... DW, J OR N PACKAGE
(TOP VIEW)



SN54LS674 ... FK PACKAGE
SN74LS674 ... FN PACKAGE
(TOP VIEW)



'LS673
FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
CS	R/W	SH CLK	STRCLR	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		NO
L	H	↓	X	X	Q15		YES	NO	NO		NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES	YES	YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES	YES	YES	NO	NO
L	L	X	H	↓	Z		NO		NO	NO	YES

'LS674 FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
CS	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)

L = low level (steady state)

↓ = transition from low to high level

↑ = transition from high to low level

X = irrelevant (any input including transitions)

Z = high impedance, input mode

Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.

Q15 = present content of 15th bit of the shift register

Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.

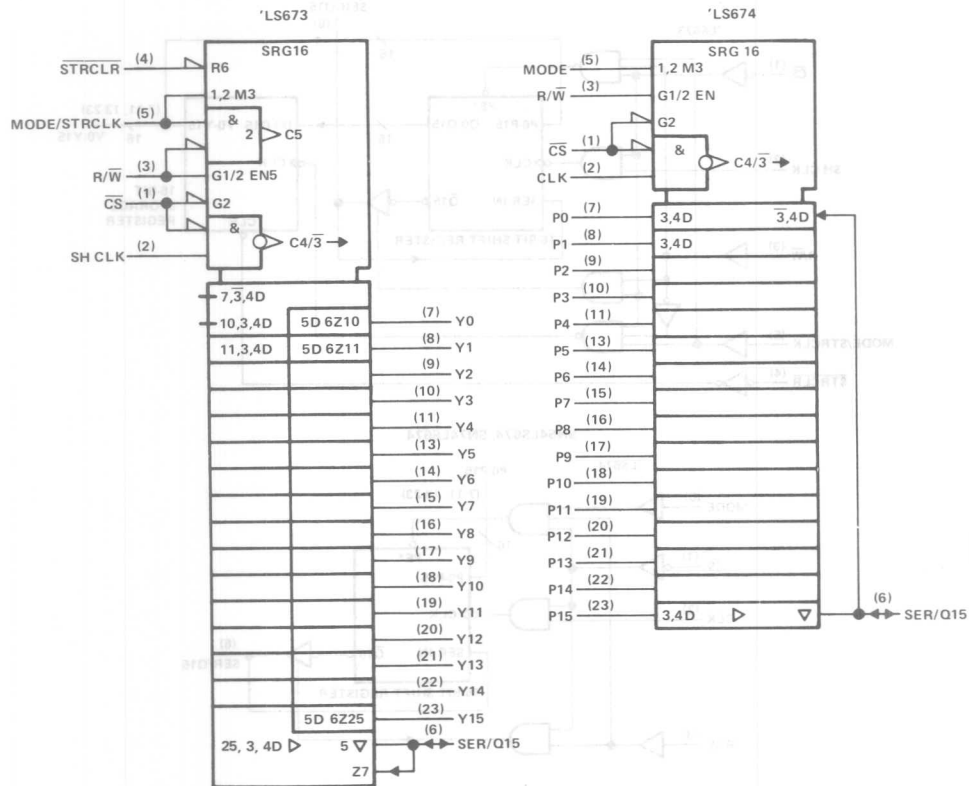
P15 = level of input P15

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TTL DEVICES

TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

logic symbols



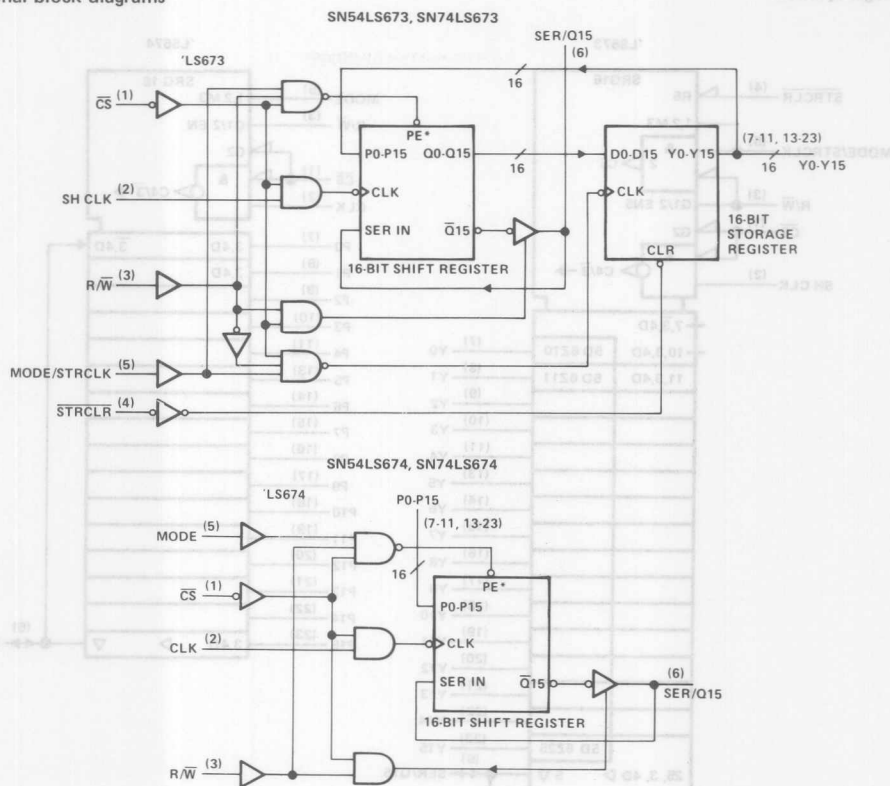
Pin numbers shown on logic notation are for DW, J or N packages.

3
TTL DEVICES

TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674

16-BIT SHIFT REGISTERS

functional block diagrams



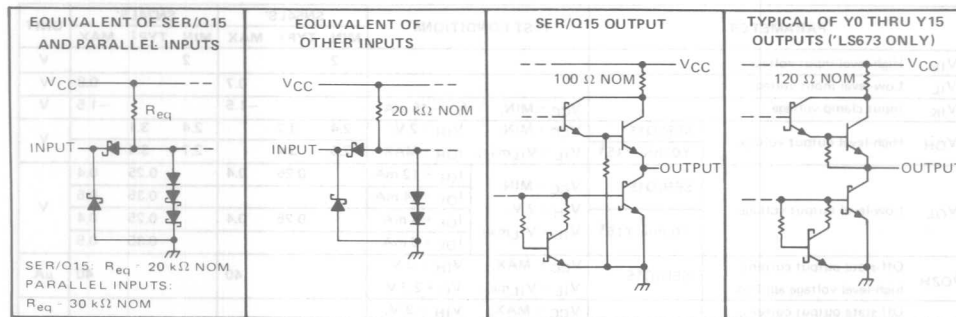
*When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SER/Q15	5.5 V
All others	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674	-55°C to 125°C
SN74LS673, SN74LS674	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current		SER/Q15	-1			-2.6			mA
			Y0 thru Y15	-0.4			-0.4			
I _{OL}	Low-level output current		SER/Q15	12			24			mA
			Y0 thru Y15	4			8			
f _{clock}	Clock frequency			0	20		0	20		MHz
t _{w(clock)}	Width of clock input pulse			20			20			ns
t _{w(clear)}	Width of clear input pulse			20			20			ns
t _{su}	Setup time		SER/Q15	20			20			ns
			P0 thru P15	20			20			
			Mode	35			35			
			R/W, CS	35			35			
			SH CLK ↓ to Mode/STR CLK ↑ See Note 2			25			25	
t _h	Hold time		SER/Q15	0			0			ns
			P0 thru P15	'LS673		0		0		
				'LS674		5.0		5.0		
				Mode		0			0	
T _A	Operating free-air temperature			-55	125		0	70		°C

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.

TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage						0.7			0.8 V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V
V _{OH}	High-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OH} = MAX	2.4	3.2		2.4	3.1		V
		Y0 thru Y15¶		2.5	3.4		2.7	3.4		
V _{OL}	Low-level output voltage	SER/Q15	V _{CC} = MIN, I _{OL} = 12 mA	0.25		0.4	0.25		0.4	V
			V _{IH} = 2 V, I _{OL} = 24 mA			0.35		0.5		
		Y0 thru Y15¶	V _{IL} = V _{ILmax} , I _{OL} = 4 mA	0.25		0.4	0.25		0.4	
			I _{OL} = 8 mA			0.35		0.5		
I _{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 2.7 V	40			40			μA
I _{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 0.4 V	-0.4			-0.4			mA
I _I	Input current at maximum input voltage	SER/Q15	V _{CC} = MAX, V _I = 5.5 V	0.1			0.1			mA
		Others	V _I = 7 V	0.1			0.1			
I _{IH}	High-level input current	SER/Q15	V _{CC} = MAX, V _I = 2.7 V	40			40			μA
		Others		20			20			
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V	-0.4			-0.4			mA
I _{OS}	Short-circuit output current§	SER/Q15	V _{CC} = MAX	-30			-130			mA
		Y0 thru Y15¶		-20			-100			
I _{CC}	Supply current	'LS673	V _{CC} = MAX	50			52			mA
		'LS674		25			40			

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

¶ 'LS673 only.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$, see note 2

PARAMETER	'LS673		'LS674		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	FROM	TO	FROM	TO					
f_{max}	SH CLK	SER/Q15	CLK	SER/Q15	$R_L = 667 \Omega, C_L = 45 \text{ pF}$	20	28		MHz
t_{PHL}	STRCLR	Y0 thru Y15					25	40	ns
t_{PLH}	MODE/	Y0 thru Y15			$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		28	45	ns
t_{PHL}	STRCLK						30	45	ns
t_{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	$R_L = 667 \Omega, C_L = 45 \text{ pF}$		21	33	ns
t_{PHL}							26	40	ns
t_{PZH}	$\overline{\text{CS}}, R/\overline{\text{W}}$	SER/Q15	$\overline{\text{CS}}, R/\overline{\text{W}}$	SER/Q15	$R_L = 667 \Omega, C_L = 45 \text{ pF}$		30	45	ns
t_{PZL}							30	45	ns
t_{PHZ}	$\overline{\text{CS}}, R/\overline{\text{W}}$	SER/Q15	$\overline{\text{CS}}, R/\overline{\text{W}}$	SER/Q15	$R_L = 667 \Omega, C_L = 5 \text{ pF}$		25	40	ns
t_{PLZ}							25	40	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

t_{PLZ} = Output disable time from low level

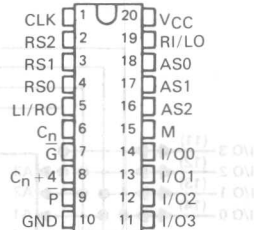
TYPES SN54LS681, SN74LS681 4-BIT PARALLEL BINARY ACCUMULATORS

D2422, JANUARY 1981 REVISED APRIL 1985

- Full 4-Bit Binary Accumulator in a Single 20-Pin Package
- Contains Two Synchronous Registers:
Word A
Word B Shift/Accumulator
- 16 Arithmetic Operations Including
B Minus A and A Minus B
- 16 Logic-Mode Operations
- Expandable to Handle N-Bit Words
with Full Carry Look-Ahead
- Bus Driving I/O Ports

SN54LS681 ... J PACKAGE
SN74LS681 ... DW, J OR N PACKAGE

(TOP VIEW)



description

These low-power Schottky IC's integrate a high-speed arithmetic logic unit (ALU) complete with word A and word B registers on a single chip. The ALU performs 16 arithmetic and 16 logic functions (see Tables 1 and 2). Full carry look-ahead is provided for fast carry of four-bit words. The carry input (C_n) and propagate and generate outputs (P and G) are provided for direct use with SN54S182/SN74S182 carry look-ahead generators for optimum performance with longer words.

The A and B registers are controlled by three inputs (RS0, RS1, and RS2). These pins define eight distinct register modes (see Table 3). The A register is a simple storage register while the B register is a combination storage/shift/accumulator register. The contents of the A and B registers provide the A and B words for the ALU.

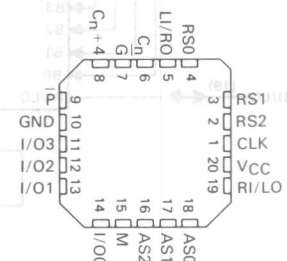
Four I/O ports (I/O 0 thru I/O 3) are provided for parallel loading of word A and/or word B into their respective registers. These same ports also serve as bus driving outputs for the ALU/accumulator results (F_j). Two additional I/O ports (RI/LO and LI/RO) are provided to allow expansion of the accumulator for words greater than four bits in length.

The A or B register can be parallel loaded from the four I/O ports. The B register can also be parallel loaded from the ALU as an accumulator register and in addition, the B register can be serially loaded from either the RI/LO or the LI/RO ports.

The SN54LS681 is characterized for operation over the full military temperature range from -55°C to 125°C. The SN74LS681 is characterized for operation from 0°C to 70°C.

SN54LS681 ... FK PACKAGE
SN74LS681

(TOP VIEW)



3

TTL DEVICES

PRODUCTION DATA

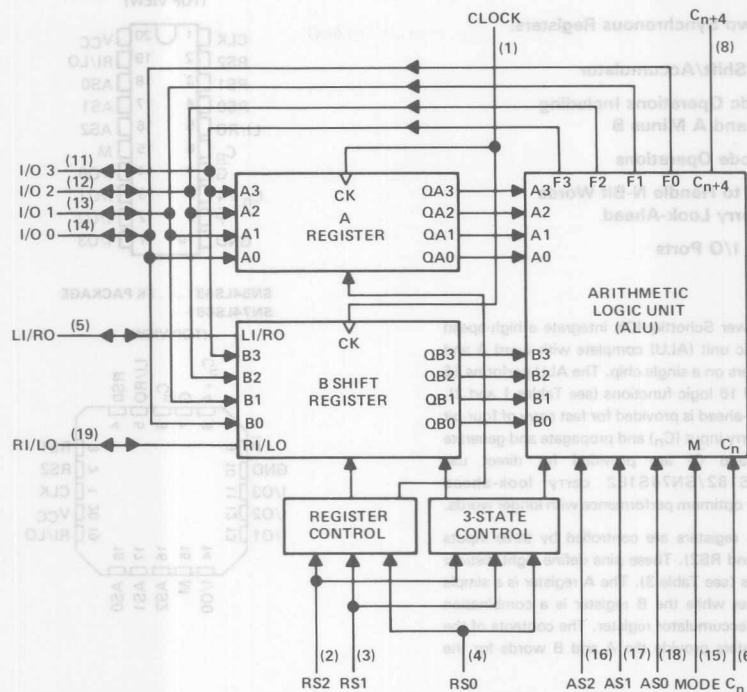
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

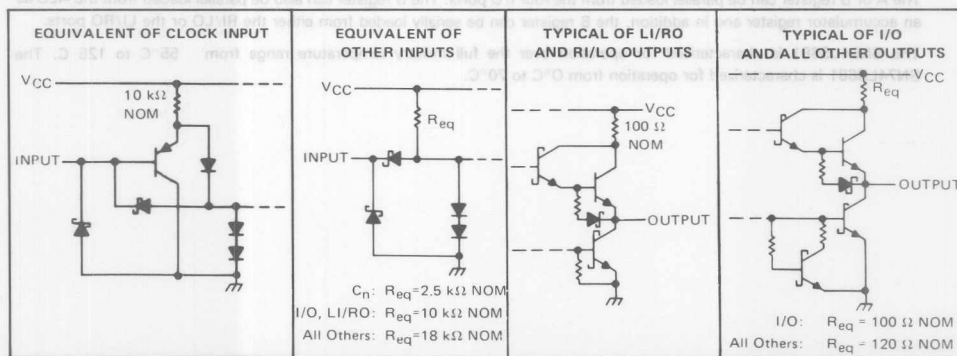
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TYPES SN54LS681, SN74LS681 4-BIT PARALLEL BINARY ACCUMULATORS

functional block diagram



schematics of inputs and outputs



TYPES SN54LS681, SN74LS681

4-BIT PARALLEL BINARY ACCUMULATORS

FUNCTION TABLES

TABLE 1 — ARITHMETIC FUNCTIONS

Mode Control (M) = Low

ALU SELECTION	ACTIVE-HIGH DATA	
	C _n = H (with carry)	C _n = L (no carry)
AS2 AS1 AS0		
L L L	F _j = L	F _j = H
L L H	F = B MINUS A	F = B MINUS A MINUS 1
L H L	F = A MINUS B	F = A MINUS B MINUS 1
L H H	F = A PLUS B PLUS 1	F = A PLUS B
H L L	F = B PLUS 1	F _j = B _j
H L H	F = B PLUS 1	F _j = B _j
H H L	F = A PLUS 1	F _j = A _j
H H H	F = A PLUS 1	F _j = A _j

TABLE 2 — LOGIC FUNCTIONS

Mode Control (M) = High

ALU SELECTION	ACTIVE-HIGH DATA	
	C _n = H (with carry)	C _n = L (no carry)
AS2 AS1 AS0		
L L L	F ₀ = H, F ₁ = F ₂ = F ₃ = L	F _j = L
L L H	F _j = A _j ⊕ B _j PLUS 1	F _j = A _j ⊕ B _j
L H L	F _j = A _j ⊕ B _j PLUS 1	F _j = A _j ⊕ B _j
L H H	F _j = L	F _j = H
H L L	F _j = A _j B _j PLUS 1	F _j = A _j B _j
H L H	F _j = A _j + B _j PLUS 1	F _j = A _j + B _j
H H L	F _j = A _j B _j PLUS 1	F _j = A _j B _j
H H H	F _j = A _j + B _j PLUS 1	F _j = A _j + B _j

TABLE 3 — REGISTER FUNCTIONS

FUNCTION	INPUTS BEFORE L TO H CLOCK TRANSITION										INTERNAL OUTPUTS AFTER L TO H CLOCK TRANSITION													
	REGISTER SELECTION			DATA INPUTS							A REGISTER				B SHIFT REGISTER						ALU			
	RS2	RS1	RS0	LI/RO	I/O 3	I/O 2	I/O 1	I/O 0	RI/LO	QA3	QA2	QA1	QA0	LI/RO	QB3	QB2	QB1	QB0	RI/LO	F3	F2	F1	F0	
ACCUM	L	L	L	Z	F3	F2	F1	F0	Z	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	Z	F3 _n	F2 _n	F1 _n	F0 _n	Z	F3	F2	F1	F0	
LOAD B	L	L	H	Z	b3	b2	b1	b0	Z	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	Z	b3	b2	b1	b0	Z	Z	Z	Z	Z	
LEFT SHIFT LOGICAL	L	H	L	li	F3	F2	F1	F0	QB0	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	li	li	QB3 _n	QB2 _n	QB1 _n	QB1 _n	F3	F2	F1	F0	
LEFT SHIFT ARITH	L	H	H	li	F3	F2	F1	F0	QB0	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	li	QB3 _n	li	QB2 _n	QB1 _n	QB1 _n	F3	F2	F1	F0	
RIGHT SHIFT LOGICAL	H	L	L	QB3	F3	F2	F1	F0	ri	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	QB2 _n	QB2 _n	QB1 _n	QB0 _n	ri	ri	F3	F2	F1	F0	
RIGHT SHIFT ARITH	H	L	H	QB2	F3	F2	F1	F0	ri	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	QB1 _n	QB3 _n	QB1 _n	QB0 _n	ri	ri	F3	F2	F1	F0	
HOLD	H	H	L	Z	F3	F2	F1	F0	Z	QA3 ₀	QA2 ₀	QA1 ₀	QA0 ₀	Z	QB3 ₀	QB2 ₀	QB1 ₀	QB0 ₀	Z	F3 ₀	F2 ₀	F1 ₀	F0 ₀	
LOAD A	H	H	H	Z	a3	a2	a1	a0	Z	a3	a2	a1	a0	Z	QB3 ₀	QB2 ₀	QB1 ₀	QB0 ₀	Z	Z	Z	Z	Z	

H = high level (steady state)

L = low level (steady state)

Z = high impedance (output off)

a0 ... a3, b0 ... b3 = the level of steady-state condition at I/O 0 thru I/O 3, respectively and intended as A or B input data

F0 ... F3 = internal ALU results

QA0₀ ... QB0₀, F0₀ ... F3₀ = the level of QA0 thru QB3 and F0 thru F3, respectively, before the indicated steady-state input conditions were established

QA0_n ... QB3_n = the level of QA0 thru QB3 before the most recent 1 transition of the clock

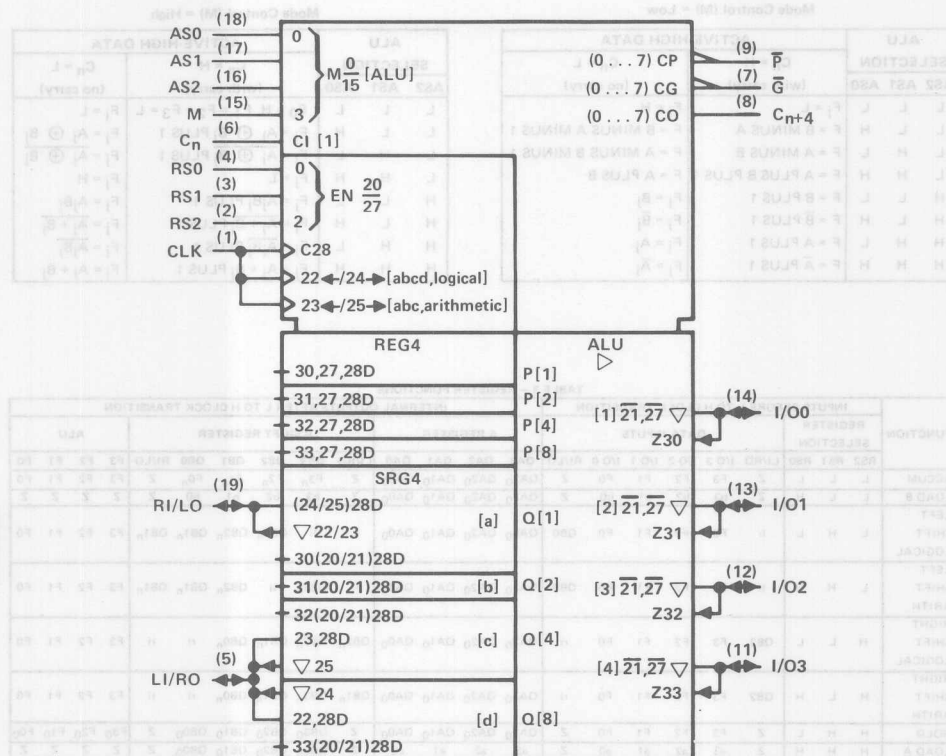
ri, li = the level of steady-state conditions at RI/LO or LI/RO, respectively

3

TTL DEVICES

TYPES SN54LS681, SN74LS681 4-BIT PARALLEL BINARY ACCUMULATORS

logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS681	-55°C to 125°C
SN74LS681	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

TYPES SN54LS681, SN74LS681 4-BIT PARALLEL BINARY ACCUMULATORS

recommended operating conditions

PARAMETER	TEST CONDITIONS	SN54LS681			SN74LS681			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	LI/RO, I/O, RI/LO			-1			-2.6	mA
	\overline{P} , \overline{G} , C_{n+4}			-0.4			-0.4	mA
Low-level output current, I_{OL}	I/O			12			24	mA
	C_{n+4} , LI/RO, RI/LO			4			8	
	\overline{P}			8			8	
	\overline{G}			16			16	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Setup time, t_{su}	RS0-RS2 to CLK†	30			30			ns
	Data I/O to CLK†	25			25			ns
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS681			SN74LS681			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage	C_n			0.7			0.7	V
	All others			0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	All I/O	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OH} = \text{MAX}$	2.4	3.1	2.4	3.2		V
	\overline{P} , \overline{G} , C_{n+4}		2.5	3.4		2.7	3.4	
V_{OL} Low-level output voltage	I/O	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 12 \text{ mA}$						
		$I_{OL} = 24 \text{ mA}$						
	LI/RO, RI/LO, C_{n+4}	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	0.25	0.4	0.25	0.4		
	\overline{P}							
	\overline{G}							
I_{OZH} Off-state output current, high-level voltage applied	I/O, LI/RO, RI/LO	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{OL} = 2.7 \text{ V}$		40			40	µA
I_{OZL} Off-state output current, low-level voltage applied	I/O, LI/RO	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_{OL} = 0.4 \text{ V}$		-0.8			-0.8	mA
	RI/LO			-0.4			-0.4	
I_I Input current at maximum input voltage	All I/O	$V_{CC} = \text{MAX}$		0.1			0.1	mA
	C_n			0.5			0.5	
	All others			0.1			0.1	
I_{IH} High-level input current	C_n			100			100	µA
	All I/O	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		40			40	
	All others			20			20	
I_{IL} Low-level input current	C_n			-4			-4	mA
	I/O, LI/RO	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.8			-0.8	
	CLK			-0.2			-0.2	
	All others			-0.4			-0.4	
I_{OS} Short-circuit output current§	I/O	$V_{CC} = \text{MAX}$	-30	-130	-30		-130	mA
	LI/RO, RI/LO, \overline{P} , \overline{G} , C_{n+4}		-20	-100	-20		-100	
I_{CC} Supply current	$V_{CC} = \text{MAX}$, RS0 at 4.5 V, All other I/O at 0 V		100	150		100	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operations.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

TYPES SN54LS681, SN74LS681 4-BIT PARALLEL BINARY ACCUMULATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	CLOCK [†]	\bar{P}	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	25	40		ns
t_{PHL}		\bar{P}		30	45		ns
t_{PLH}		\bar{G}		26	40		ns
t_{PHL}		\bar{G}		27	40		ns
t_{PLH}		I/O		27	40		ns
t_{PHL}		I/O		29	40		ns
t_{PLH}		C_n+4	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	36	55		ns
t_{PHL}		C_n+4		34	50		ns
t_{PLH}		LI/RO		25	40		ns
t_{PHL}		LI/RO		23	35		ns
t_{PLH}		RI/LO		19	30		ns
t_{PHL}		RI/LO		17	30		ns
t_{PLH}	AS0-AS2	\bar{P}	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	30	45		ns
t_{PHL}		\bar{P}		30	45		ns
t_{PLH}		\bar{G}		27	35		ns
t_{PHL}		\bar{G}		28	35		ns
t_{PLH}		I/O		31	45		ns
t_{PHL}		I/O		29	45		ns
t_{PLH}		C_n+4	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	39	55		ns
t_{PHL}		C_n+4		34	50		ns
t_{PLH}		\bar{P}	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	9	25		ns
t_{PHL}		\bar{P}		9	20		ns
t_{PLH}		I/O		17	35		ns
t_{PHL}		I/O		13	20		ns
t_{PLH}	MODE	C_n+4	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	20	30		ns
t_{PHL}		C_n+4		16	25		ns
t_{PLH}		\bar{P}		28	40		ns
t_{PHL}		\bar{P}		29	40		ns
t_{PLH}		\bar{G}	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	21	30		ns
t_{PHL}		\bar{G}		23	30		ns
t_{PLH}		I/O		30	45		ns
t_{PHL}		I/O		28	40		ns
t_{PLH}		C_n+4	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	40	60		ns
t_{PHL}		C_n+4		37	50		ns
t_{PZH}	RS0-RS2	I/O	$R_L = 667\ \Omega$	$C_L = 45\text{ pF}$	28	45	ns
t_{PZL}				$C_L = 45\text{ pF}$	28	45	ns
t_{PHZ}				$C_L = 5\text{ pF}$	35	65	ns
t_{PLZ}				$C_L = 5\text{ pF}$	39	65	ns
t_{PZH}		LI/RO	$R_L = 2\text{ k}\Omega$	$C_L = 15\text{ pF}$	25	40	ns
t_{PZL}				$C_L = 15\text{ pF}$	22	40	ns
t_{PHZ}				$C_L = 5\text{ pF}$	21	40	ns
t_{PLZ}				$C_L = 5\text{ pF}$	34	60	ns
t_{PZH}		RI/LO	$R_L = 2\text{ k}\Omega$	$C_L = 15\text{ pF}$	22	40	ns
t_{PZL}				$C_L = 15\text{ pF}$	24	40	ns
t_{PHZ}				$C_L = 5\text{ pF}$	11	30	ns
t_{PLZ}				$C_L = 5\text{ pF}$	16	40	ns

[†] t_{PLH} = Propagation delay time, low-to-high-level input

t_{PHL} = Propagation delay time, high-to-low-level input

t_{PZL} = Output enable time to low level

t_{PZH} = Output enable time to high level

t_{PLZ} = Output disable time from low level

t_{PHZ} = Output disable time from high level

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS682 THRU SN54LS689, SN74LS682 THRU SN74LS689 8-BIT MAGNITUDE/IDENTITY COMPARATORS

D2617, JANUARY 1981—REVISED DECEMBER 1983

- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 and 'LS683 have 20-k Ω Pullup Resistors on the Q Inputs
- 'LS686 and 'LS687 . . . New JT and NT 24-Pin, 3000-Mil Packages

TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-k Ω PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS683	yes	yes	no	open-collector	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
'LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no
'LS689	yes	no	yes	open-collector	no

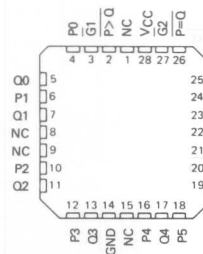
SN54LS686, SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . DW, JT OR NT PACKAGE

(TOP VIEW)



SN54LS686, SN54LS687 . . . FK PACKAGE
SN74LS686, SN74LS687 . . . FN PACKAGE

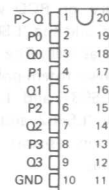
(TOP VIEW)



NC - No internal connection

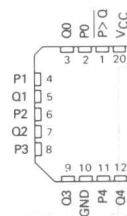
SN54LS682 THRU SN54LS685 . . . J PACKAGE
SN74LS682 THRU SN74LS685 . . . DW, J OR N PACKAGE

(TOP VIEW)



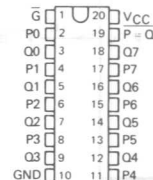
SN54LS682 THRU SN54LS685 . . . FK PACKAGE
SN74LS682 THRU SN74LS685

(TOP VIEW)



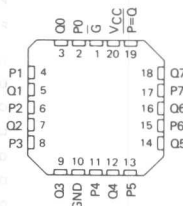
SN54LS688, SN54LS689 . . . J PACKAGE
SN74LS688, SN74LS689 . . . DW, J OR N PACKAGE

(TOP VIEW)



SN54LS688, SN54LS689 . . . FK PACKAGE
SN74LS688, SN74LS689

(TOP VIEW)



PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

3-1143

3

TTL DEVICES

TYPES SN54LS682 THRU SN54LS689, SN74LS682 THRU SN74LS689 8-BIT MAGNITUDE/IDENTITY COMPARATORS

description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P = Q}$ outputs and the 'LS682 thru 'LS687 provide $\overline{P > Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS683, 'LS685, 'LS687, and 'LS689 have open-collector outputs. The 'LS682 and 'LS683 feature 20-k Ω pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

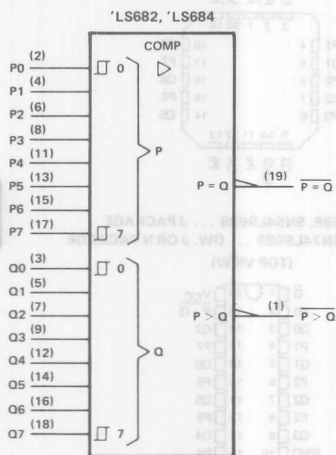
INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P = Q}$	$\overline{P > Q}$
P, Q	$\overline{G_1}, \overline{G_2}$	$\overline{G_2}$		
P = Q	L	X	L	H
P > Q	X	L	H	L
P < Q	X	X	H	H
P = Q	H	X	H	H
P > Q	X	H	H	H
X	H	H	H	H

- NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS689.
2. The $\overline{P < Q}$ function can be generated by applying the $\overline{P = Q}$ and $\overline{P > Q}$ outputs to a 2-input NAND gate.
3. For 'LS686, 'LS687 $\overline{G_1}$ enables $\overline{P = Q}$, and $\overline{G_2}$ enables $\overline{P > Q}$.

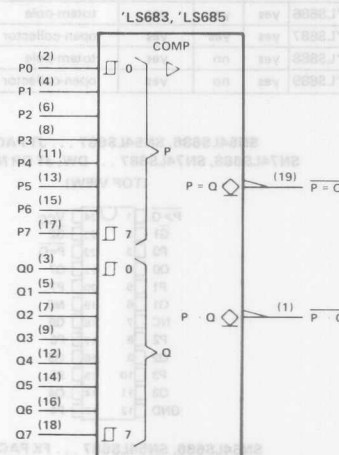
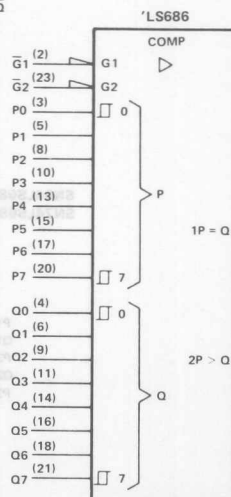
logic symbols

3

TTL DEVICES

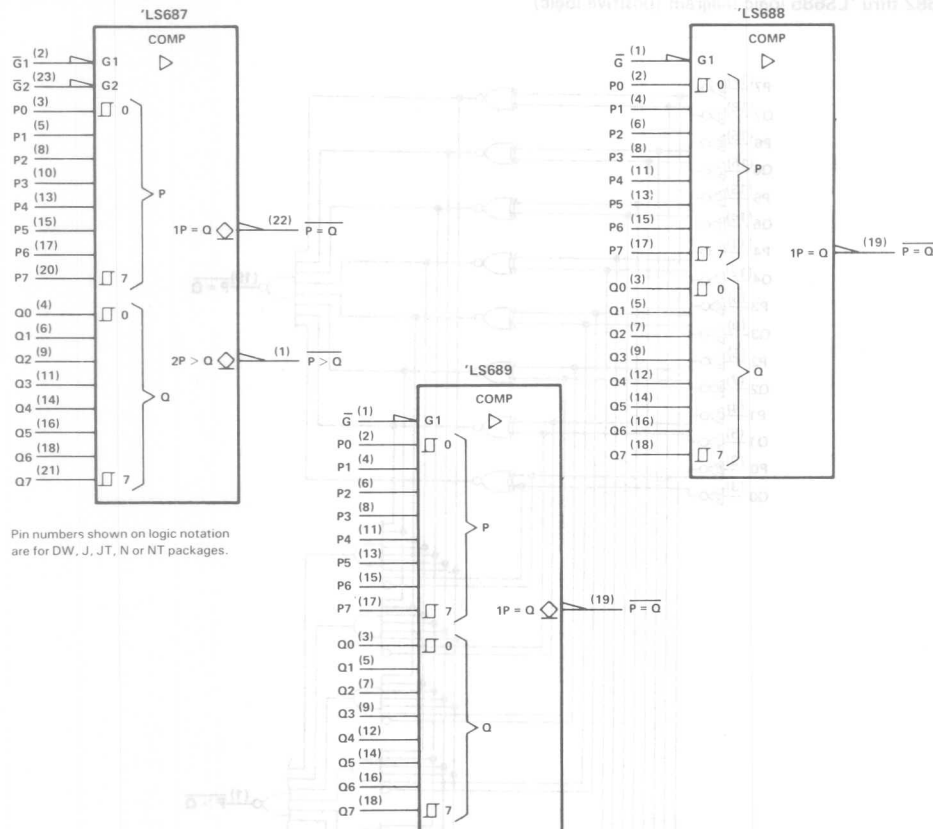


Pin numbers shown on logic notation are for DW, J, JT, N or NT packages.

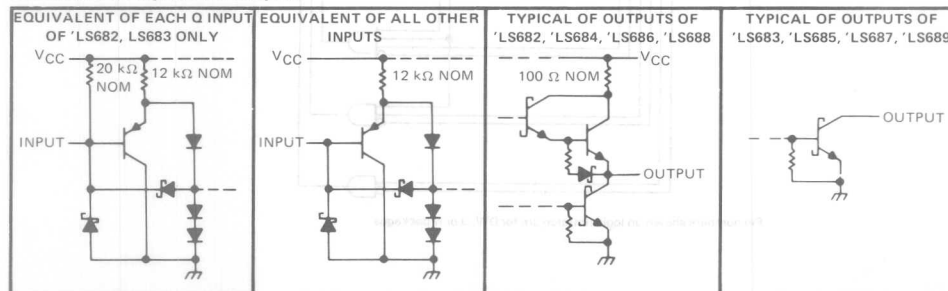


TYPES SN54LS682 THRU SN54LS689, SN74LS682 THRU SN74LS689 8-BIT MAGNITUDE/IDENTITY COMPARATORS

logic symbols (continued)

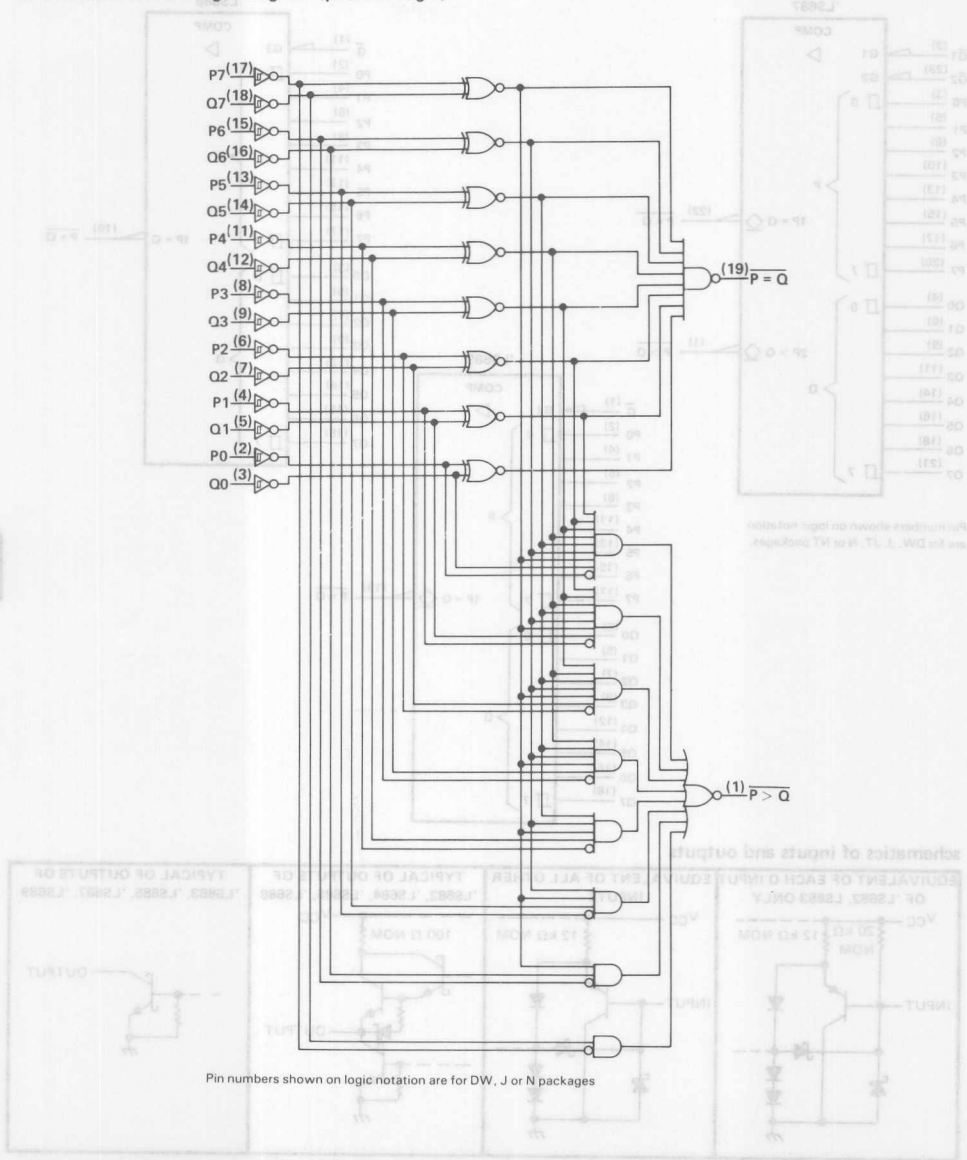


schematics of inputs and outputs



TYPES SN54LS682 THRU SN54LS685
SN74LS682 THRU SN74LS685
8-BIT MAGNITUDE/IDENTITY COMPARATORS

'LS682 thru 'LS685 logic diagram (positive logic)

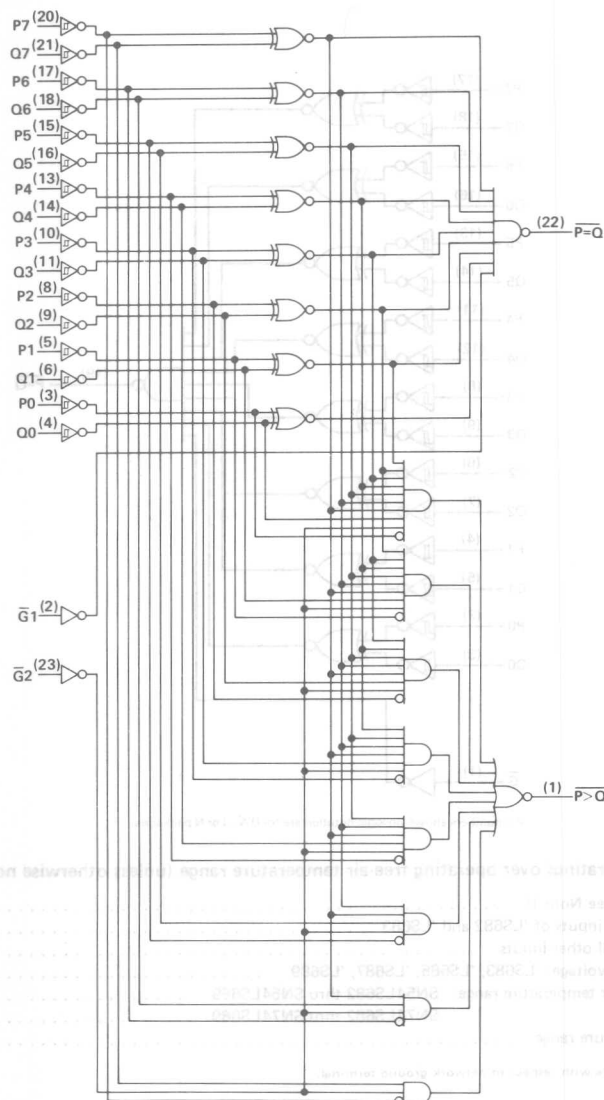


3

TTL DEVICES

TYPES SN54LS686, SN54LS687
SN74LS686, SN74LS687
8-BIT MAGNITUDE/IDENTITY COMPARATORS

'LS686, 'LS687 logic diagram (positive logic)



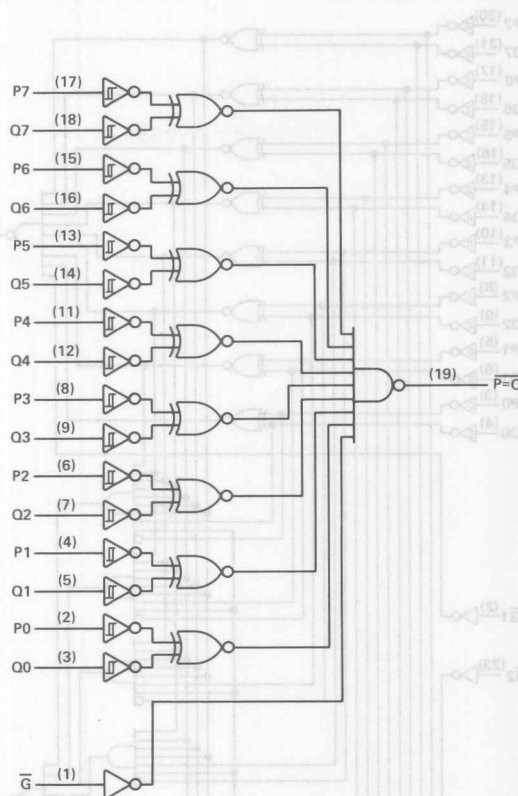
Pin numbers shown on logic notation are for DW, JT, or NT packages.

3

TTL DEVICES

**TYPES SN54LS688, SN54LS689,
SN74LS688, SN74LS689**
8-BIT IDENTITY COMPARATORS

'LS688, 'LS689 logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: Q inputs of 'LS682 and 'LS683	5.5 V
All other inputs	7 V
Off-state output voltage: 'LS683, 'LS685, 'LS687, 'LS689	7 V
Operating free-air temperature range: SN54LS682 thru SN54LS689	-55°C to 125°C
SN74LS682 thru SN74LS689	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TTL DEVICES

**TYPES SN54LS682, SN54LS684, SN54LS686, SN54LS688,
SN74LS682, SN74LS684, SN74LS686, SN74LS688**
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

‘LS682, ‘LS684, ‘LS686, ‘LS688

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis P or Q inputs			0.4			0.4	V
V_{IK}	Input clamp voltage			-1.5			-1.5	V
V_{OH}	High-level output voltage			2.5			2.7	V
V_{OL}	Low-level output voltage			0.25			0.25	V
				0.4			0.5	V
I_I	Input current at maximum input voltage			0.1			0.1	mA
	Q inputs, 'LS682							
	All other inputs							
I_{IH}	High-level input current			20			20	μA
I_{IL}	Low-level input current			-0.4			-0.4	mA
	Q inputs, 'LS682							
	All other inputs							
$I_{OS} §$	Short-circuit output current			-20			-100	mA
I_{CC}	Supply current			42			42	mA
	'LS682			40			65	
	'LS684			44			75	
	'LS686			40			65	
	'LS688							

†All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}C$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with any \bar{G} inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^{\circ}C$

PARAMETER#	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$P = Q$	$R_L = 667 \Omega$, $C_L = 45$ pF, All other inputs low, See Note 3	13	25		15	25		13	25		18	27		ns
t_{PHL}				15	25		17	25		20	30		20	30		
t_{PLH}	Q	$P = \bar{Q}$		14	25		16	25		13	25		18	27		ns
t_{PHL}				15	25		15	25		21	30		20	30		
t_{PLH}	\bar{G}, \bar{G}_1	$P = \bar{Q}$								11	20		12	18		ns
t_{PHL}										19	30		13	20		
t_{PLH}	P	$P > \bar{Q}$		20	30		22	30		19	30					ns
t_{PHL}				15	30		17	30		15	30					
t_{PLH}	Q	$P > \bar{Q}$		21	30		24	30		18	30					ns
t_{PHL}				19	30		20	30		19	30					
t_{PLH}	\bar{G}_2	$P > \bar{Q}$								21	30					ns
t_{PHL}										16	25					

t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

3

TTL DEVICES

recommended operating conditions 'LS683, 'LS685, 'LS687, 'LS689

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs		0.4			0.4		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 5.5 \text{ V}$			250			100	µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$		0.25	0.4		0.25	0.4	V
		$V_{IL} = V_{IL \text{ max}}$, $I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS683			$V_I = 5.5 \text{ V}$			0.1	mA
		All other inputs			$V_I = 7 \text{ V}$			0.1	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	Low-level input current	Q inputs, 'LS683			-0.4			-0.4	mA
		All other inputs			-0.2			-0.2	
I_{CC}	Supply current	'LS683			42			42	mA
		'LS685			40			40	
		'LS687			44			44	
		'LS689			40			40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with any \bar{G} inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER§	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS683		'LS685		'LS687		'LS689		UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
t_{PLH}	P	$\bar{P} = Q$	$R_L = 667 \Omega$, $C_L = 45 \text{ pF}$, All other inputs low, See Note 3	30	45	30	45	24	35	24	40	ns
t_{PHL}				20	30	19	35	20	30	22	35	
t_{PLH}	Q	$\bar{P} = Q$		24	35	24	45	24	35	24	40	ns
t_{PHL}				23	35	23	35	20	30	22	35	
t_{PLH}	\bar{G}, \bar{G}_1	$\bar{P} = Q$						21	35	22	35	ns
t_{PHL}								18	30	19	30	
t_{PLH}	P	$\bar{P} > Q$		31	45	32	45	24	35			ns
t_{PHL}				17	30	16	35	16	30			
t_{PLH}	Q	$\bar{P} > Q$		30	45	30	45	24	35			ns
t_{PHL}				21	30	20	35	16	30			
t_{PLH}	\bar{G}_2	$\bar{P} > Q$						24	35			ns
t_{PHL}								15	30			

§ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2423, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . . Decade Counter, Direct Clear
- 'LS691 . . . Binary Counter, Direct Clear
- 'LS692 . . . Decade Counter, Synchronous Clear
- 'LS693 . . . Binary Counter, Synchronous Clear

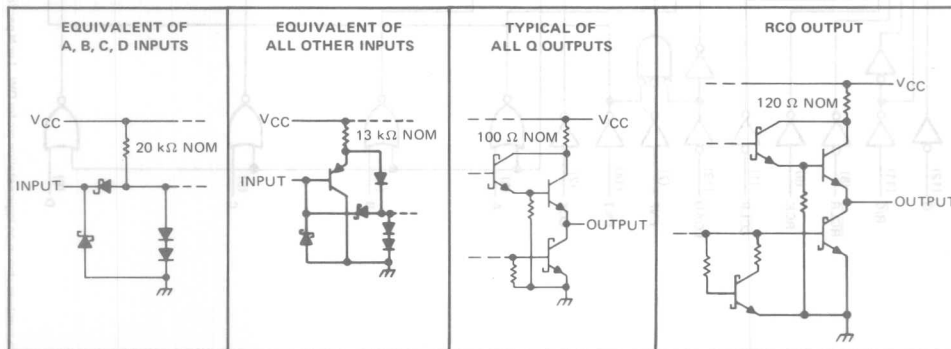
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P inputs and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered: The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS692 and 'LS693. Loading of the counter is accomplished when $\overline{\text{LOAD}}$ is taken low and a positive-transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting RCO of the first stage to ENT of the second stage, etc. All ENP inputs can be tied common and used as a master enable or disable control.

schematics of inputs and outputs

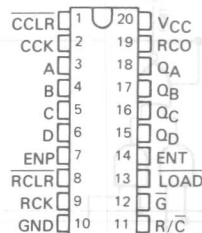


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TEXAS
INSTRUMENTS

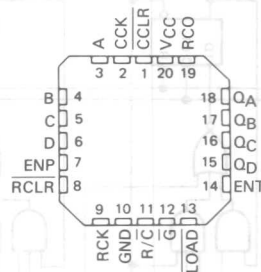
SN54LS690 THRU SN54LS693 . . . J PACKAGE
SN74LS690 THRU SN74LS693 . . . DW, J OR N PACKAGE

(TOP VIEW)



SN54LS690 THRU SN54LS693 . . . FK PACKAGE
SN74LS690 THRU SN74LS693

(TOP VIEW)



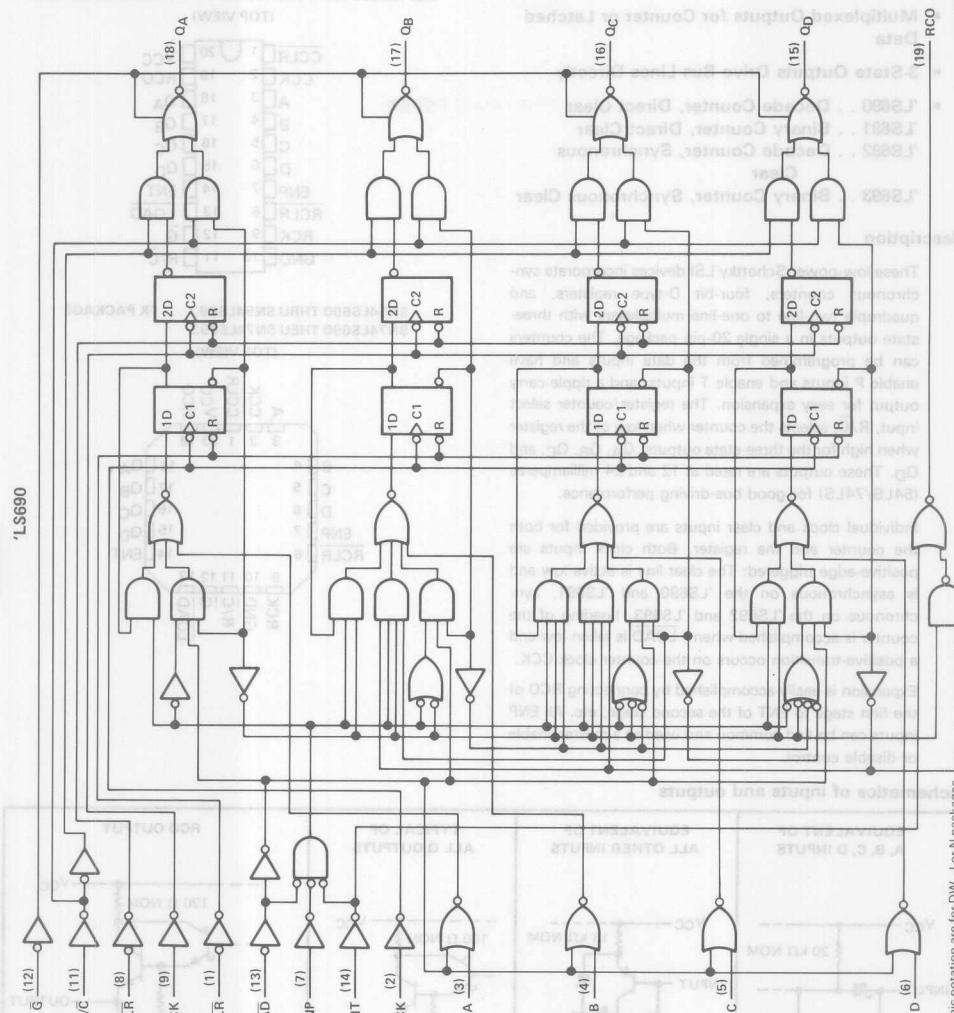
3

TTL DEVICES

TYPE SN54LS690, SN74LS690
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams

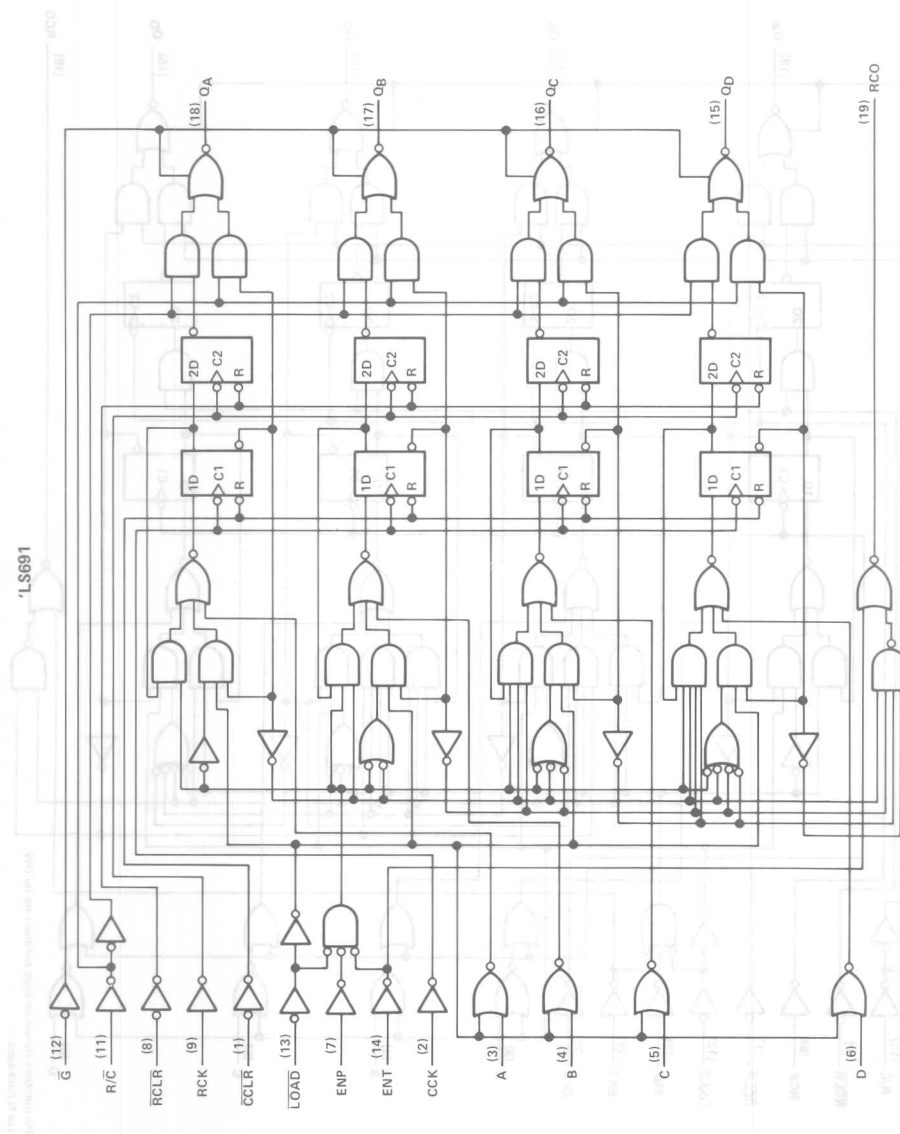
3 TTL DEVICES



Pin numbers shown on logic notation are for DW, J or N packages.

TYPE SN54LS691, SN74LS691
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)



Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPE SN54LS692, SN74LS692
 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
 AND MULTIPLEXED 3-STATE OUTPUTS

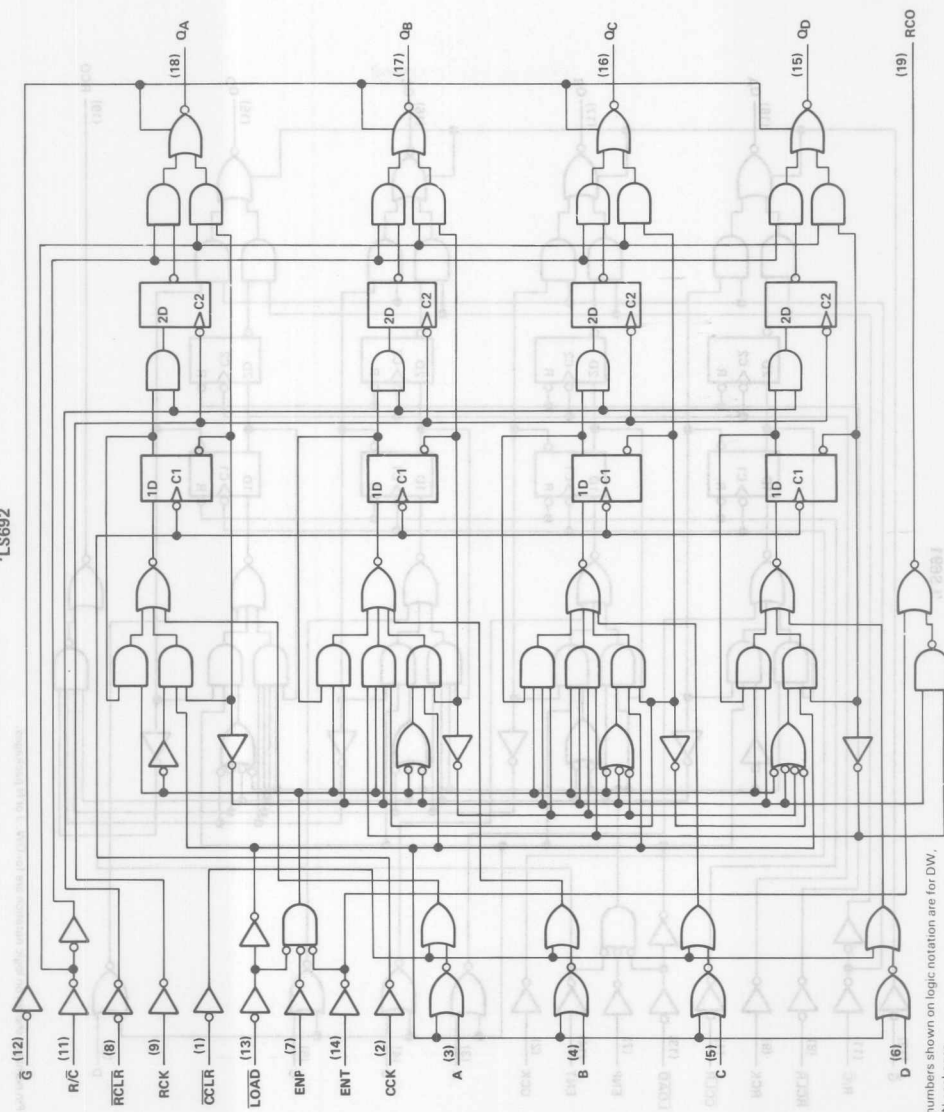
logic diagrams (continued)

(continued)

3

TTL DEVICES

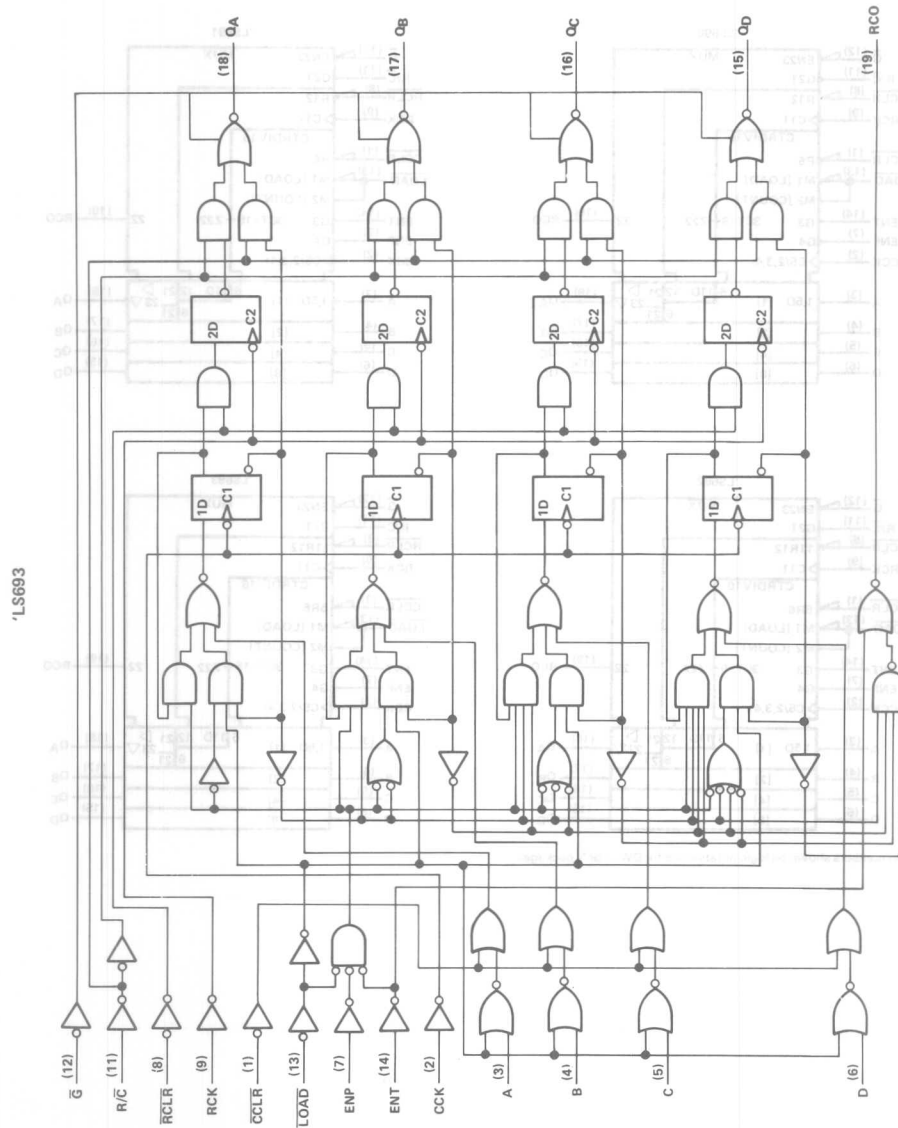
LS692



Pin numbers shown on logic notation are for DW, J or N packages.

TYPE SN54LS693, SN74LS693
 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
 AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)

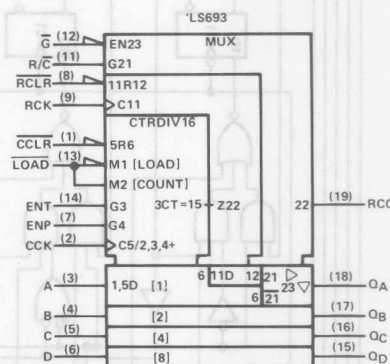
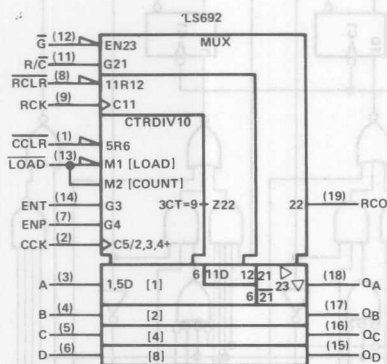
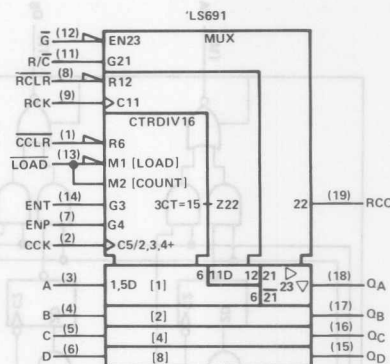
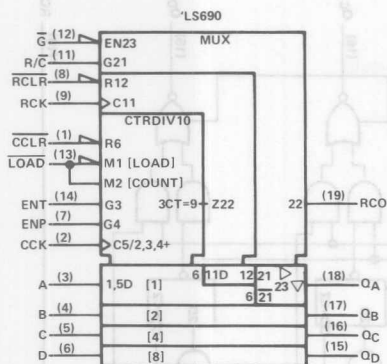


Pin numbers shown on logic notation are for DW, J or N packages.

TTL DEVICES

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
AND MULTIPLEXED 3-STATE OUTPUTS

logic symbols



Pin numbers shown on logic notation are for DW, J or N packages.

3 TTL DEVICES

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693 **SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS** **AND MULTIPLEXED 3-STATE OUTPUTS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS690 thru SN54LS693	-55°C to 125°C
SN74LS690 thru SN74LS693	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS*			SN74LS*			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
I _{OH}	High-level output current	Q			− 1			− 2.6	mA
		RCO			− 0.4			− 0.4	mA
I _{OL}	Low-level output current	Q			12			24	mA
		RCO			4			8	mA
f _{clock}	Clock frequency	CCK			20			20	MHz
		RCK			0			0	MHz
t _w	Pulse duration	CCK high or low			25			25	ns
		RCK high or low			25			25	
		'LS690, 'LS691			20			20	
					20			20	
t _{su}	Setup time before CCK ↑	A thru D			30			30	ns
		ENP or ENT			30			30	
		LOAD ↓			30			30	
		'LS692, 'LS693			40			40	
		'LS690, 'LS691			25			25	
t _{su}	Setup time before RCK ↑	CCK ↑ (see Note 2)			30			30	ns
		'LS690, 'LS691			25			25	
		'LS692, 'LS693			20			20	
					0			0	
t _h	Hold time	Any input from CCK ↑ or RCK ↑							ns
T _A	Operating free-air temperature		− 55		125		0	70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

3

TTL DEVICES

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V
V _{OH}	Any Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA			2.4 3.1			V
	I _{OH} = -2.6 mA			2.4 3.1					
	I _{OH} = -0.4 mA			2.5 3.2					
V _{OL}	Any Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA			0.25 0.4			V
	I _{OL} = 24 mA			0.35 0.5					
	I _{OL} = 4 mA			0.25 0.4					
	I _{OL} = 8 mA			0.35 0.5					
I _{OZH}	Any Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 2.7 V	20			20			μA
I _{OZL}	Any Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _O = 0.4 V	-20			-20			μA
I _I		V _{CC} = MAX, V _I = 7 V	0.1			0.1			mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V	20			20			μA
I _{IL}	A thru D	V _{CC} = MAX, V _I = 0.4 V	-0.4			-0.4			mA
	All others		-0.2			-0.2			
I _{OS} §	Any Q	V _{CC} = MAX, V _O = 0 V	-30			-30			mA
	RCO		-20			-20			
I _{CCH}		V _{CC} = MAX, All outputs open	See Note 3		46	65	46	65	mA
I _{CCL}			See Note 4		48	70	48	70	
I _{CCZ}			See Note 5		48	70	48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured after two 4.5 V to 0-V to 4.5-V pulses have been applied to CCK and RCK while \bar{G} is grounded and all other inputs are at 4.5 V.

4. I_{CCL} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while all other inputs are grounded.

5. I_{CCZ} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while \bar{G} is at 4.5 V and all other inputs are grounded.

3
TTL DEVICES

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS690, 'LS691		'LS692, 'LS693		UNIT	
				MIN	TYP	MAX	MIN		TYP
t _{PLH}	CCK1	RCO	R _L = 2 kΩ, C _L = 15 pF	23	40		23	40	ns
t _{PHL}				23	40		23	40	
t _{PLH}	ENT	RCO		13	20		13	20	ns
t _{PHL}				13	20		13	20	
t _{PLH}	CCK1	Q	R _L = 667 Ω, C _L = 45 pF	12	20		12	20	ns
t _{PHL}				17	25		17	25	
t _{PLH}	RCK1	Q		12	20		12	20	ns
t _{PHL}				17	25		17	25	
t _{PHL}	CCLR _i	Q		23	40				ns
t _{PHL}	RCLR _i	Q		20	30				ns
t _{PLH}	R/ \overline{C}	Q		16	25		16	25	ns
t _{PHL}				16	25		16	25	
t _{PZH}	\overline{G}_i	Q		19	30		19	30	ns
t _{PZL}	\overline{G}_i	Q		19	30		19	30	
t _{PHZ}			R _L = 667 Ω, C _L = 5 pF	17	30		17	30	ns
t _{PLZ}	17	30			17	30			

NOTE 6: See General Information Section for load circuits and voltage waveforms.

- t_{PLH} Propagation delay time, low-to-high-level output
- t_{PHL} Propagation delay time, high-to-low-level output
- t_{PZH} Output enable time to high level
- t_{PZL} Output enable time to low level
- t_{PHZ} Output disable time from high level
- t_{PLZ} Output disable time from low level

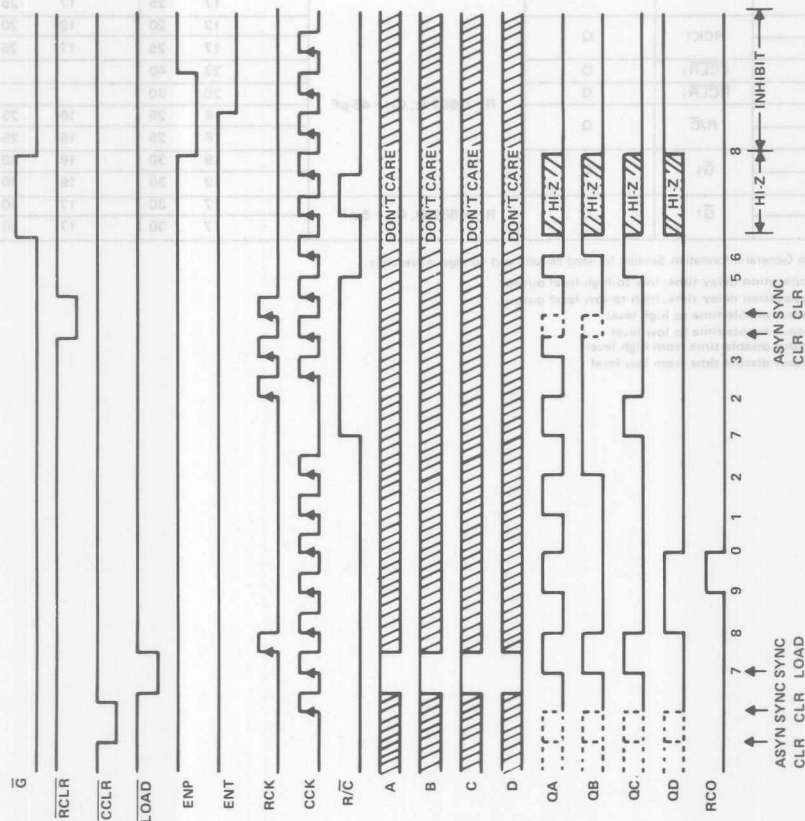


3

TTL DEVICES

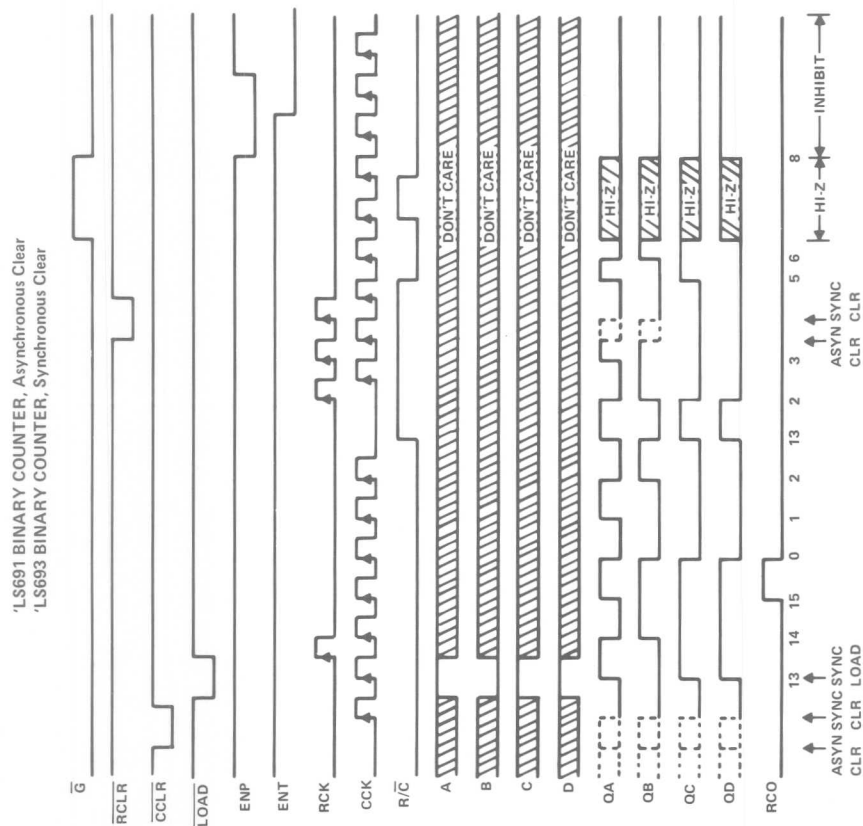
3 TTL DEVICES

LS690 DECADE COUNTER, Asynchronous Clear
LS692 DECADE COUNTER, Synchronous Clear



TYPES SN54LS691, SN54LS693, SN74LS691, SN74LS693
 SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS
 AND MULTIPLEXED 3-STATE OUTPUTS

typical operating sequences (continued)



TTL DEVICES



3 TTL DEVICES

TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699 SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2424, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS696 . . . Decade Counter, Direct Clear
- 'LS697 . . . Binary Counter, Direct Clear
- 'LS698 . . . Decade Counter, Synchronous Clear
- 'LS699 . . . Binary Counter, Synchronous Clear

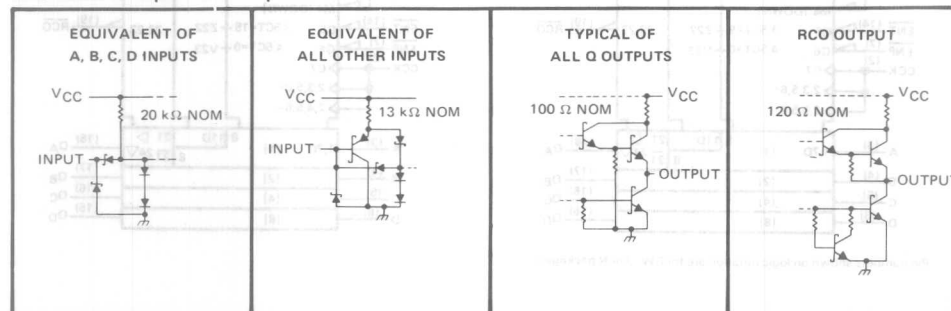
description

These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three state outputs in a single 20-pin package. The up/down counters are programmable from the data inputs and feature enable P and enable T and a ripple-carry output for easy expansion. The register/counter select input R/C, selects the counter when low and the register when high for the three-state outputs, Q_A , Q_B , Q_C , and Q_D . These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus driving performance.

Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is asynchronous on the 'LS696 and 'LS697, synchronous on the 'LS698 and 'LS699. Loading of the counter is accomplished when \overline{LOAD} is taken low and a positive transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting RCO of the first stage to ENT of the second stage, etc. All ENP inputs can be tied common and used as a master enable or disable control.

schematics of inputs and outputs

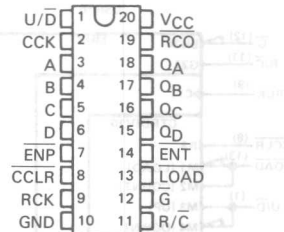


PRODUCTION DATA

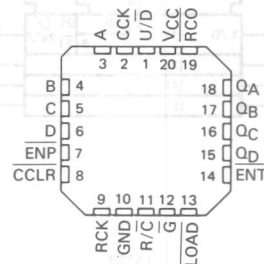
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

SN54LS696 THRU SN54LS699 . . . J PACKAGE
SN74LS696 THRU SN74LS699 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS696 THRU SN54LS699 . . . FK PACKAGE
SN74LS696 THRU SN74LS699
(TOP VIEW)

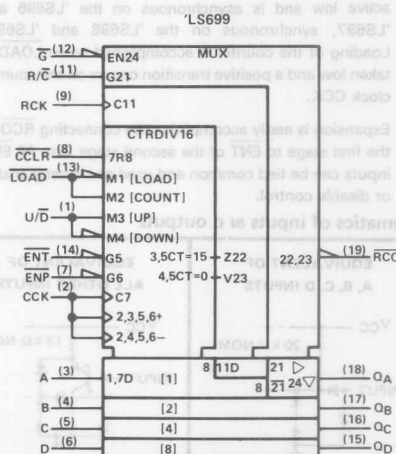
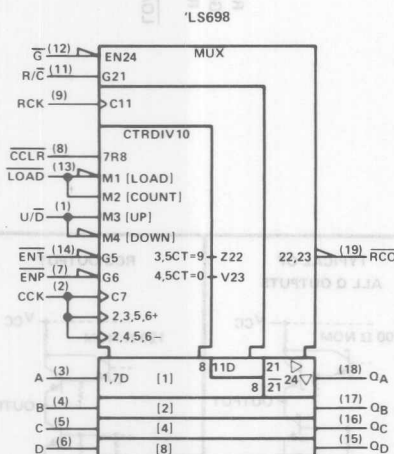
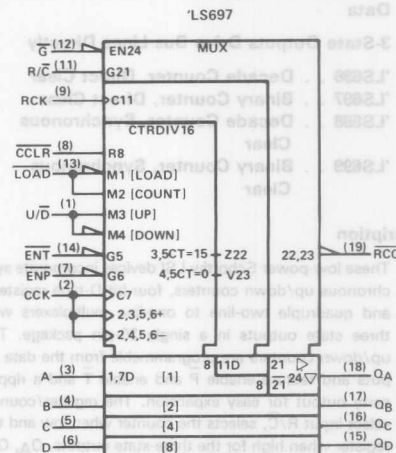
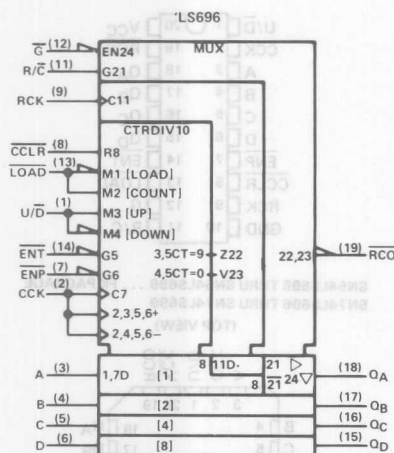


3

TTL DEVICES

TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699 SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic symbols

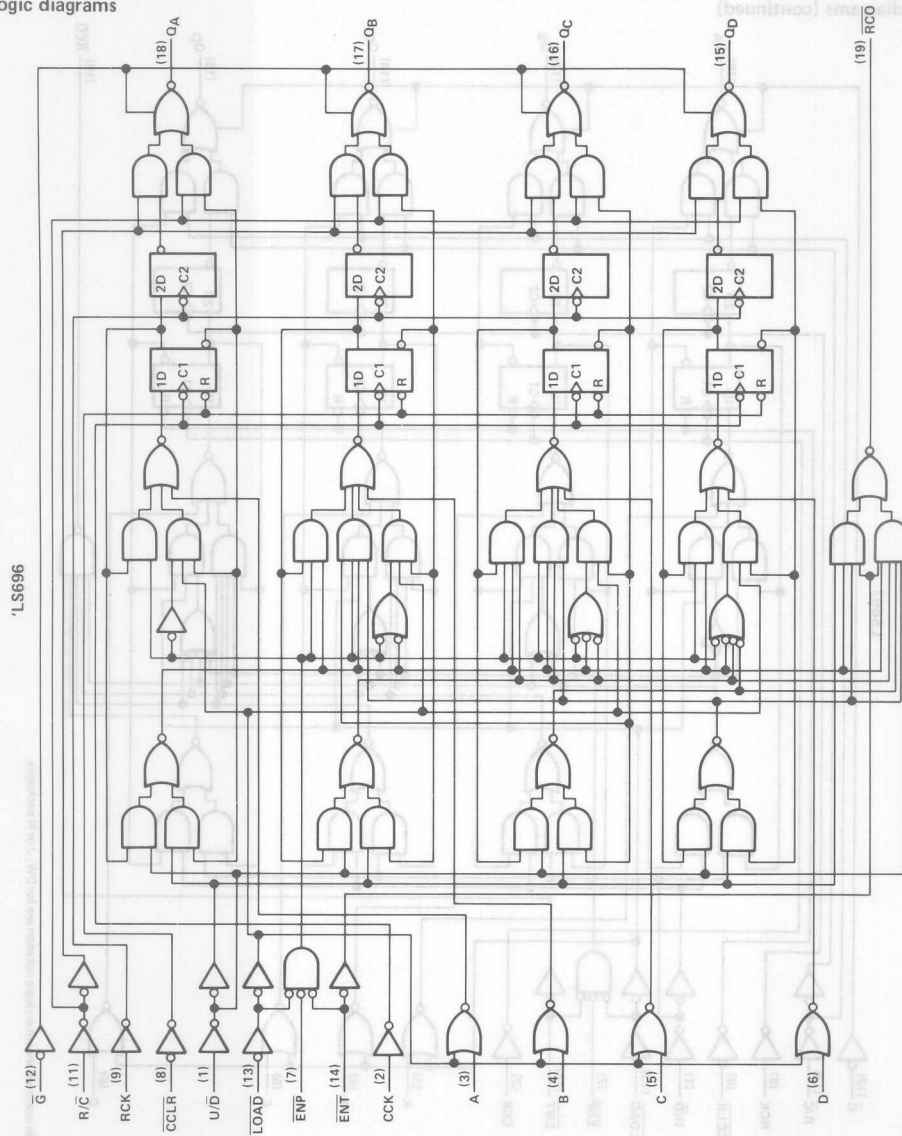


Pin numbers shown on logic notation are for DW, J or N packages.

3
TTL DEVICES

TYPES SN54LS696, SN74LS696
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams



LS696

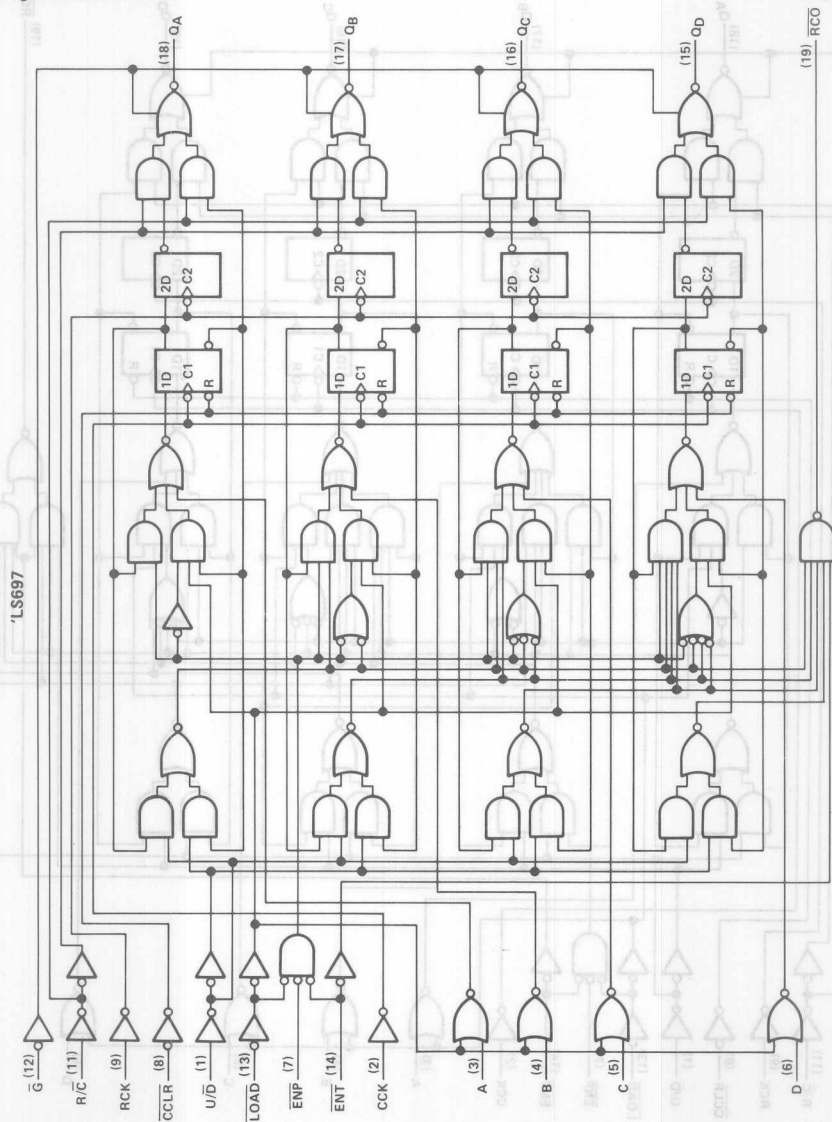
Pin numbers shown on logic notation are for DW, J or N packages.

3

TTL DEVICES

TYPES SN54LS697, SN74LS697
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)

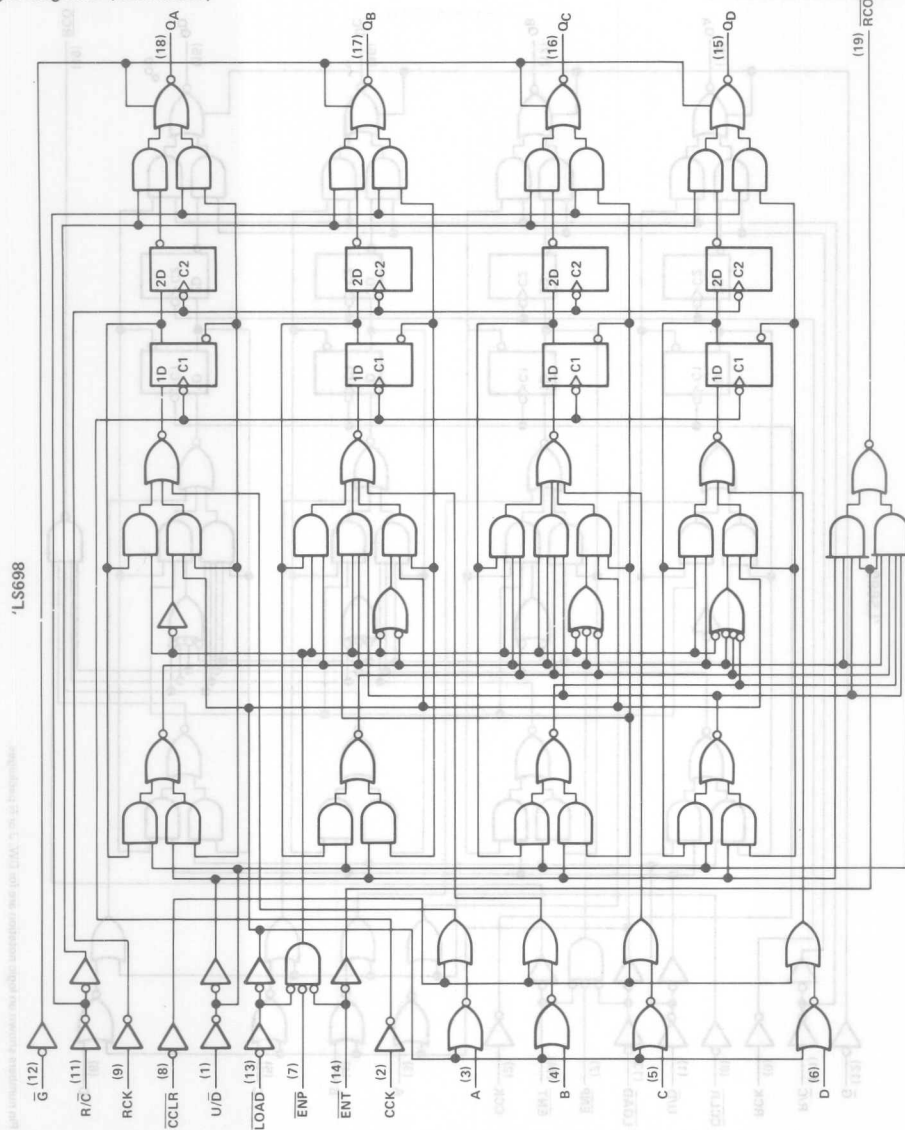


Pin numbers shown on logic notation are for DW, J or N packages.

3 TTL DEVICES

TYPES SN54LS696, SN74LS696, SN54LS698, SN74LS698
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)

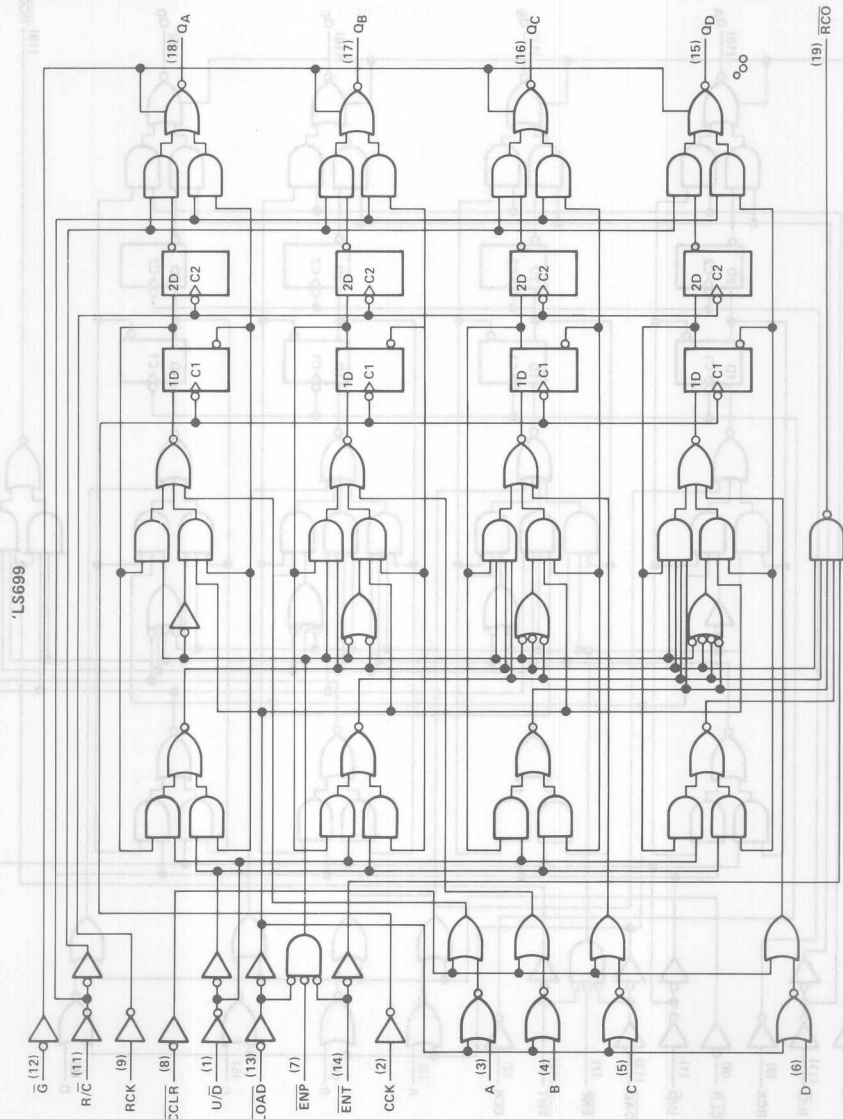


Pin numbers shown on logic notation are for DW, J or N packages.

TTL DEVICES 3

TYPES SN54LS697, SN74LS697, SN54LS699, SN74LS699
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)



Pin numbers shown on logic notation are for DW, J or N packages.

3 TTL DEVICES

**TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS696 thru SN54LS699	–55°C to 125°C
SN74LS696 thru SN74LS699	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current	Q			− 1			− 2.6	mA
		$\overline{R}CO$			− 0.4			− 0.4	
I _{OL}	Low-level output current	Q			12			24	mA
		$\overline{R}CO$			4			8	
f _{clock}	Clock frequency	CCK	0		20	0		20	MHz
		RCK	0		20	0		20	
t _w	Pulse duration	CCK high or low	25		25				ns
		RCK high or low	25		25				
		'LS696, 'LS697 CCLR low	20		20				
		A thru D	30		30			30	
		ENP or ENT	30		30			30	
t _{su}	Setup time	LOAD	30		30			30	ns
	before CCK †	U/D	35		35			35	
		'LS696, 'LS697, CCLR inactive	25		25				
		'LS698, 'LS699, CCLR	30		30				
t _{su}	Setup time CCK † before RCK † (see Note 2)		30		30			30	ns
t _H	Hold time		0		0			0	ns
T _A	Operating free-air temperature		− 55		125	0		70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.



TEXAS
INSTRUMENTS

3-1169

TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS*			SN74LS*			UNIT		
				MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IH}	High-level input voltage			2			2			V		
V _{IL}	Low-level input voltage						0.7			0.8	V	
V _{IK}	Input clamp voltage	V _{CC} =MIN, I _I =-18 mA					-1.5			-1.5	V	
V _{OH}	High-level output voltage	Any Q	V _{CC} =MIN, V _{IH} =2 V, V _{IL} =V _{IL} max	I _{OH} =-1 mA	2.4		3.1				V	
		I _{OH} =-2.6 mA						2.4	3.1			
		I _{OH} =-400 µA		2.5		3.2		2.7		3.2		
V _{OL}	Low-level output voltage	Any Q	V _{CC} =MIN, V _{IH} =2 V, V _{IL} =V _{IL} max	I _{OL} =12 mA	0.25		0.4		0.25		0.4	V
		I _{OL} =24 mA						0.35		0.5		
		I _{OL} =4 mA		0.25		0.4		0.25		0.4		
		I _{OL} =8 mA						0.35		0.5		
I _{OZH}	Off-state output current, high-level voltage applied	Any Q	V _{CC} =MAX, \overline{G} at 2 V, V _O =2.7 V				20			20	µA	
I _{OZL}	Off-state output current, low-level voltage applied	Any Q	V _{CC} =MAX, \overline{G} at 2 V, V _O =0.4 V				-20			-20	µA	
I _I	Input current at maximum input voltage		V _{CC} =MAX, V _I =7 V				0.1			0.1	mA	
I _{IH}	High-level input current		V _{CC} =MAX, V _I =2.7 V				20			20	µA	
I _{IL}	Low-level input current	A thru D	V _{CC} =MAX, V _I =0.4 V				-0.4			-0.4	mA	
		All others					-0.2			-0.2		
I _{OS}	Short-circuit output current§	Any Q	V _{CC} =MAX, V _O =0 V				-30			-130	mA	
		R _{CO}					-20			-100		-20
I _{CCH}	Supply current, outputs high		V _{CC} =MAX,	See Note 3	46		65		46	65	mA	
I _{CCL}	Supply current, outputs low		All outputs open	See Note 4	48		70		48	70		
I _{CCZ}	Supply current, outputs off			See Note 5	48		70		48	70		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured after two 4.5 V to 0 V to 4.5 V pulses have been applied to CCK and RCK while \bar{G} is grounded and all other inputs are at 4.5 V.

4. I_{CCL} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while all other inputs are grounded.

5. I_{CCZ} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while \bar{G} is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

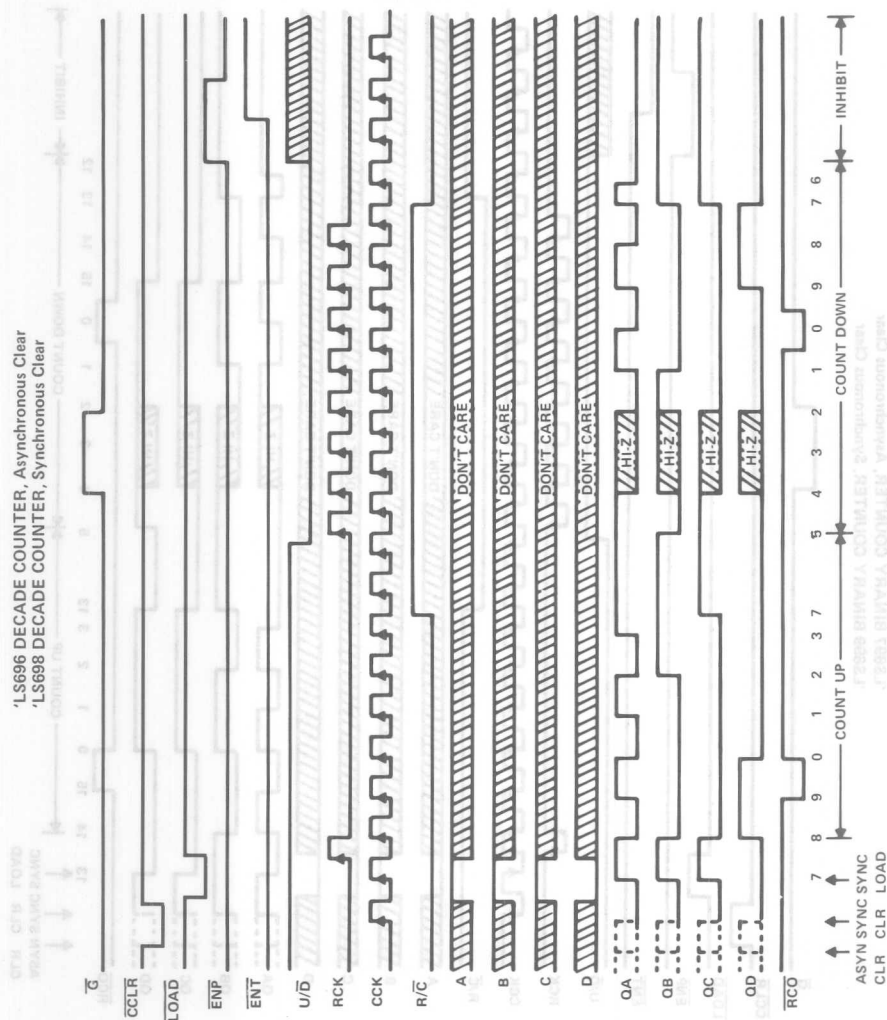
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS696, 'LS697			'LS698, 'LS699			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
t _{PLH}	CCK↑	\overline{RCO}	R _L = 2 kΩ, C _L = 15 pF		23	40		23	40	ns	
t _{PHL}					23	40		23	40	ns	
t _{PLH}	\overline{ENT}	\overline{RCO}			13	20		13	20	ns	
t _{PHL}					13	20		13	20	ns	
t _{PLH}	CCK↑	Q	R _L = 667 Ω, C _L = 45 pF		12	20		12	20	ns	
t _{PHL}					17	25		17	25	ns	
t _{PLH}	RCK↑	Q			12	20		12	20	ns	
t _{PHL}					17	25		17	25	ns	
t _{PHL}	$\overline{CCLR}↓$	Q			23	40				ns	
t _{PLH}											
t _{PHL}	R/ \overline{C}	Q			16	25		16	25	ns	
t _{PHL}					16	25		16	25	ns	
t _{PZH}	$\overline{G}↓$	Q			19	30		19	30	ns	
t _{PZL}					19	30		19	30	ns	
t _{PHZ}	$\overline{G}↑$	Q	R _L = 667 Ω, C _L = 5 pF		17	30		17	30	ns	
t _{PLZ}					17	30		17	30	ns	

NOTE 6: See General Information Section for load circuits and voltage waveforms.

3
TTL DEVICES

TYPES SN54LS696, SN54LS698, SN74LS696, SN74LS698
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

typical operating sequences



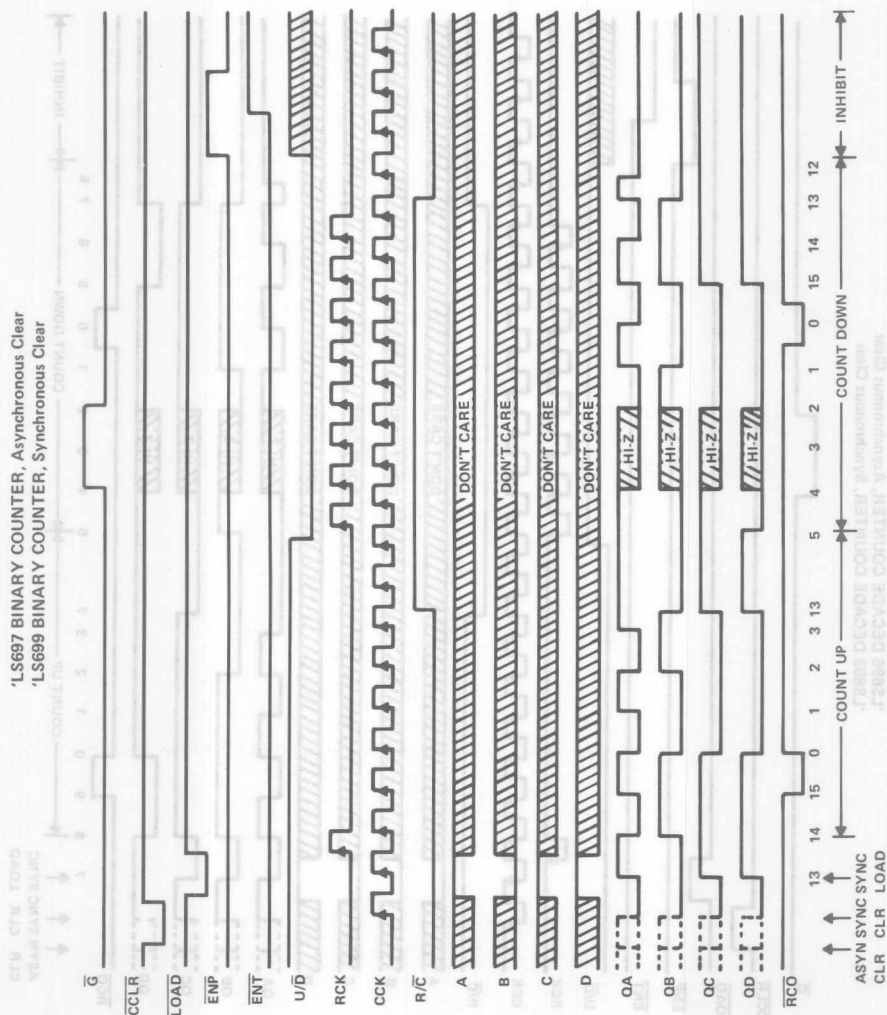
TTL DEVICES

3

TYPES SN54LS697, SN54LS699, SN74LS697, SN74LS699
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

typical operating sequences (continued)

3 TTL DEVICES



The TTL Data Book

General Information

1

Functional Index

2

TTL Devices

3

Mechanical Data

4

MECHANICAL DATA

1 General Information

2 Functional Index

3 TTL Devices

4 Mechanical Data

MECHANICAL DATA

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

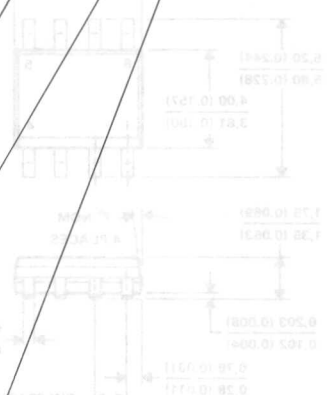
EXAMPLE SN 54LS01 J 4

1. Prefix
MUST CONTAIN TWO TO FOUR LETTERS
SN Standard Prefix
SNJ JEDEC Publication 101, Class B
JANB MIL-M-38510 Qualified

2. Unique Circuit Description
MUST CONTAIN FOUR TO NINE CHARACTERS
(From Individual Data Sheet)
Examples:
5410
74H10
54S112
74LS295A
74LS645-1

3. Package
MUST CONTAIN ONE OR TWO LETTERS
D, DW, J, JD, JG, JT, N, NT, P, W (Dual-in-line packages)[†]
FK or FN (Chip carriers)
(From pin-connection diagram on individual data sheet)

4. Instructions (Dash No.)
3 PEP processing, level 3 (N or NT packages only)



[†] These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

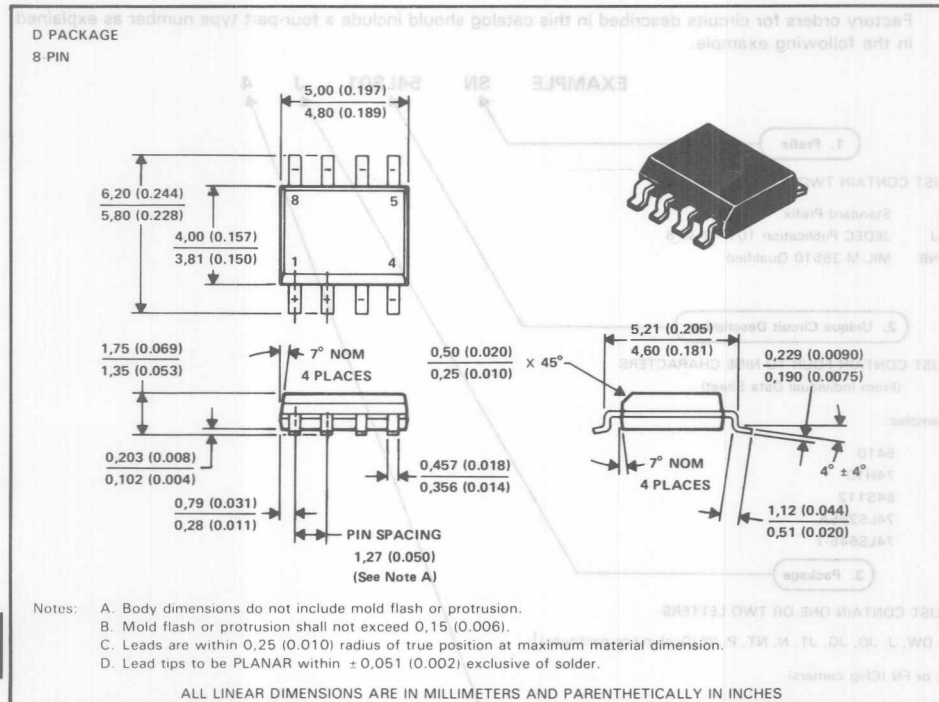
Dual-in-line (D, DW, J, JD, JG, JT, N, NT, P, W)

- A-Channel Plastic Tubing
- Tape and Reel
- Barnes Carrier (W only)

MECHANICAL DATA

D plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



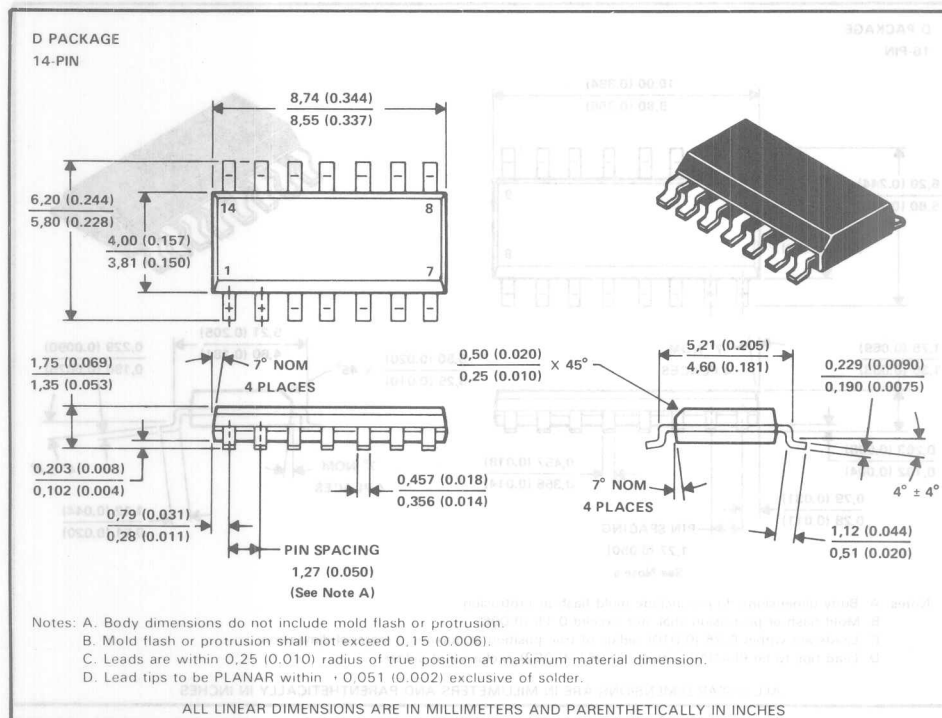
4

MECHANICAL DATA

MECHANICAL DATA

D plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



4

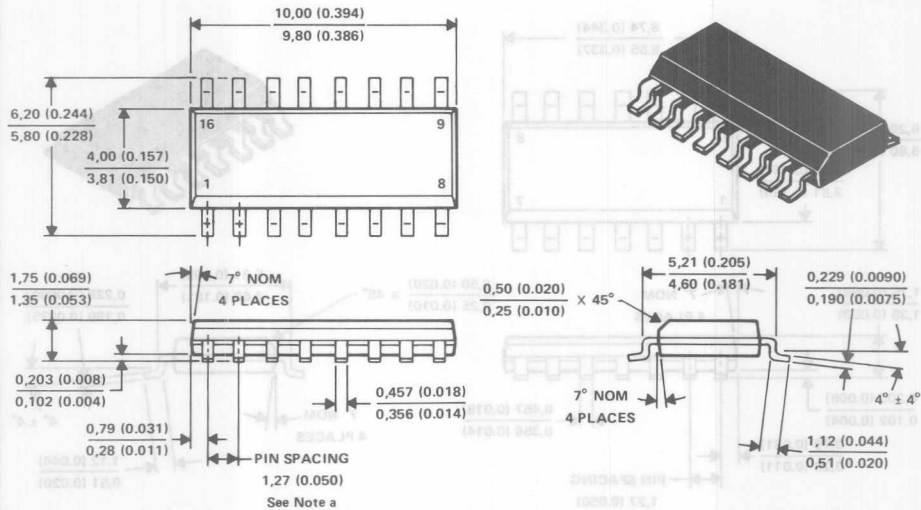
MECHANICAL DATA

MECHANICAL DATA

D plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D PACKAGE
16-PIN



Notes: A. Body dimensions do not include mold flash or protrusion.

B. Mold flash or protrusion shall not exceed 0,15 (0.006).

C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

D. Lead tips to be PLANAR within ±0,051 (0.002) exclusive of solder.

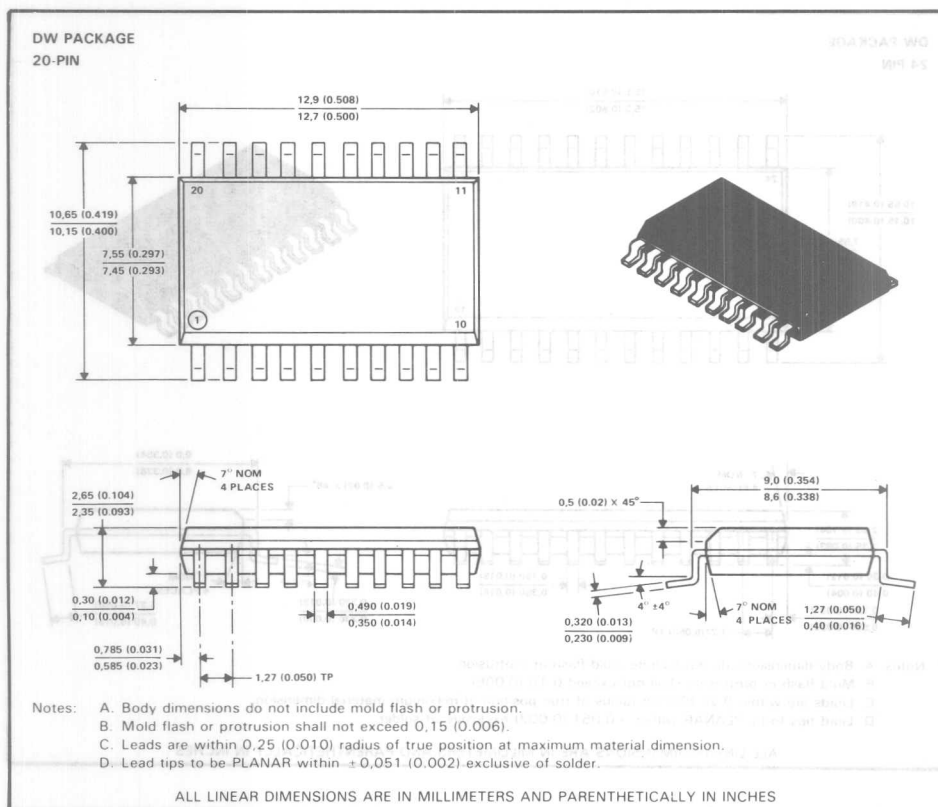
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4

MECHANICAL DATA

DW plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

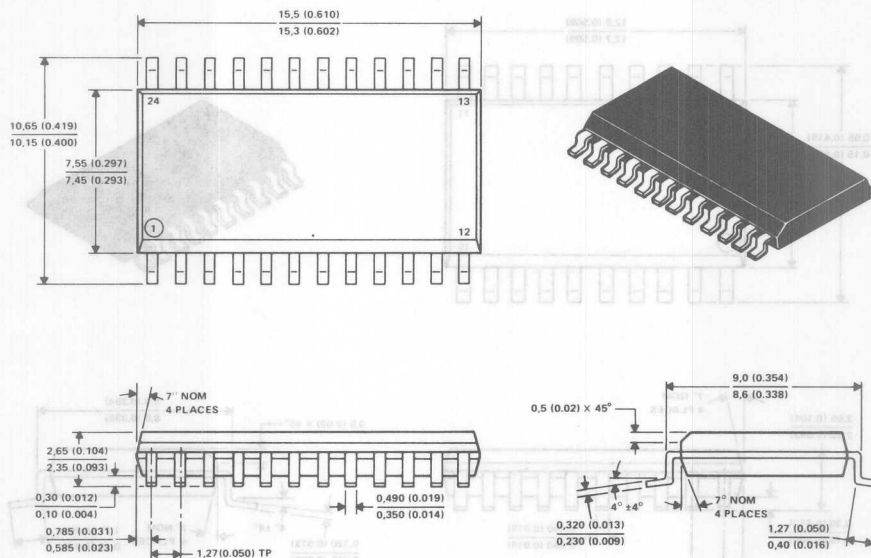


MECHANICAL DATA

DW plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW PACKAGE
24-PIN



Notes: A. Body dimensions do not include mold flash or protrusion.

B. Mold flash or protrusion shall not exceed 0.15 (0.006).

C. Leads are within 0.25 (0.010) radius of true position at maximum material dimension.

D. Lead tips to be PLANAR within ± 0.051 (0.002) exclusive of solder.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4

MECHANICAL DATA

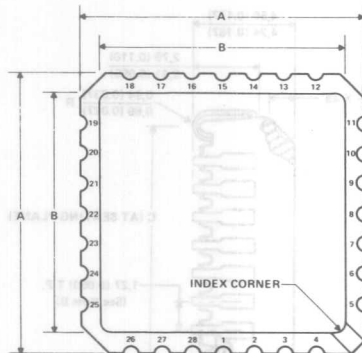
MECHANICAL DATA

FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers; terminals require no additional cleaning or processing when used in soldered assembly. FK package terminal assignments conform to JEDEC Standards 1 and 2.

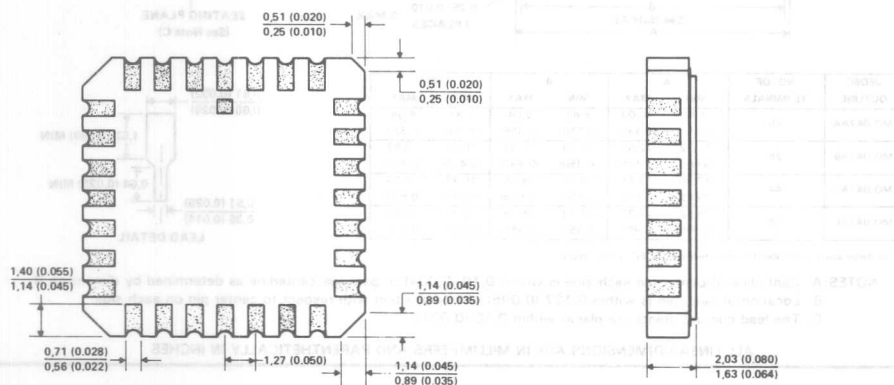
FK CERAMIC CHIP CARRIER PACKAGES

(28-terminal package shown)



JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	8,69 (0,342)	9,09 (0,358)	7,80 (0,307)	9,09 (0,358)
MS004CC	28	11,23 (0,442)	11,63 (0,458)	10,31 (0,406)	11,63 (0,458)

*All dimensions and notes for the specified JEDEC outline apply.



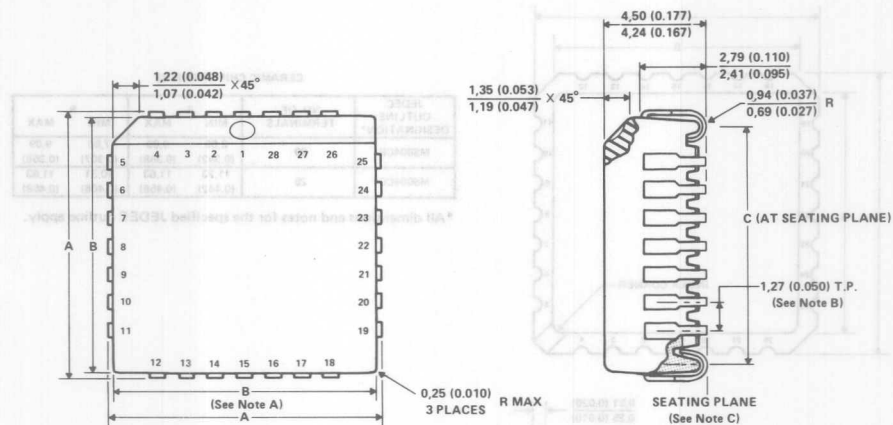
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO 047AA	20	9.78 (0.385)	10.03 (0.395)	8.89 (0.350)	9.04 (0.356)	7.87 (0.310)	8.38 (0.330)
MO 047AB	28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	10.41 (0.410)	10.92 (0.430)
MO 047AC	44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	15.49 (0.610)	16.00 (0.630)
MO 047AE	68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.956)	23.11 (0.910)	23.62 (0.930)

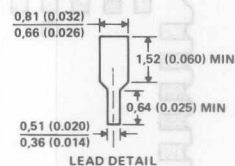
All dimensions and notes for the specified JEDEC outline apply.

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.

B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

C. The lead contact points are planar within 0,10 (0.004).

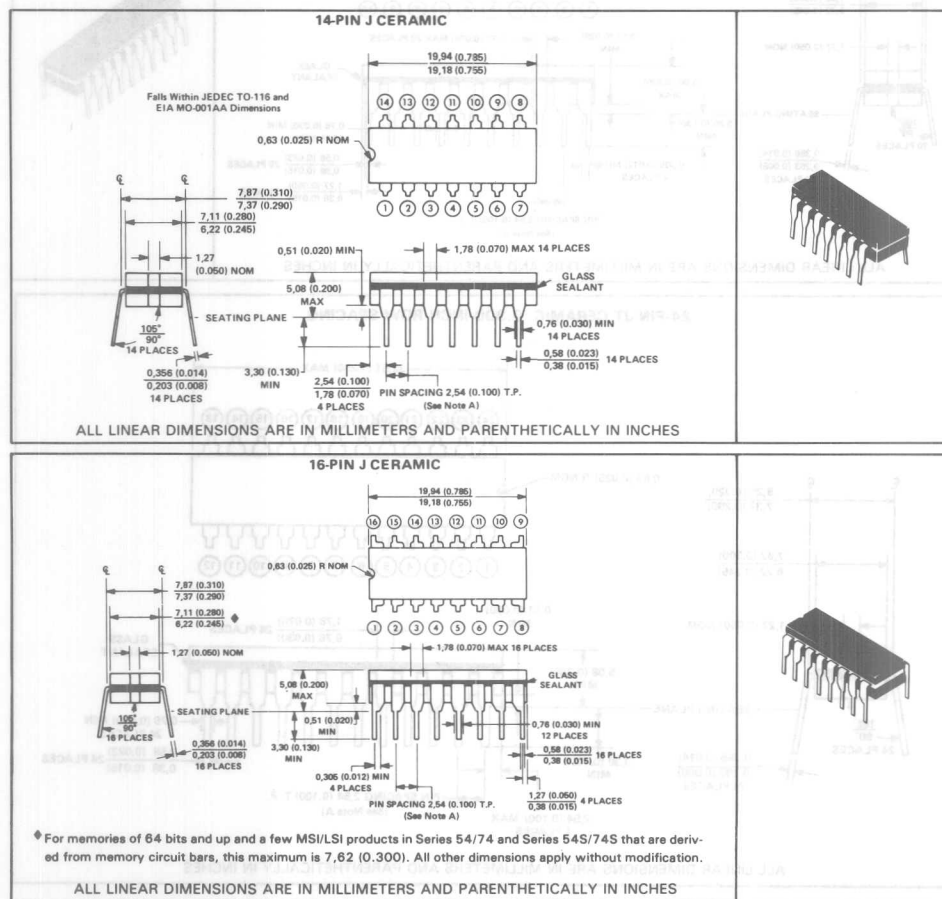
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



J ceramic packages (including JT dual-in-line package)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

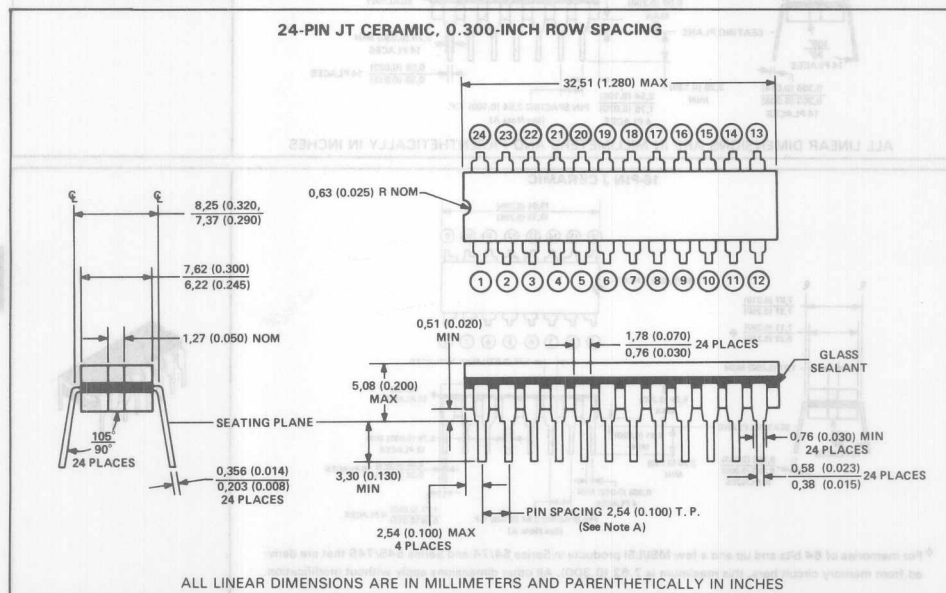
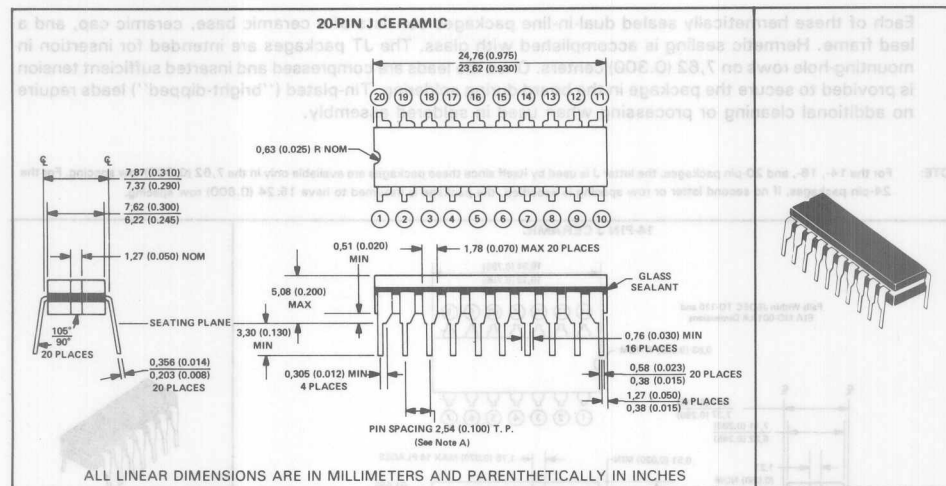
NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

MECHANICAL DATA

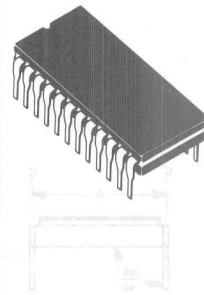
J ceramic dual-in-line packages (continued)



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

4

MECHANICAL DATA

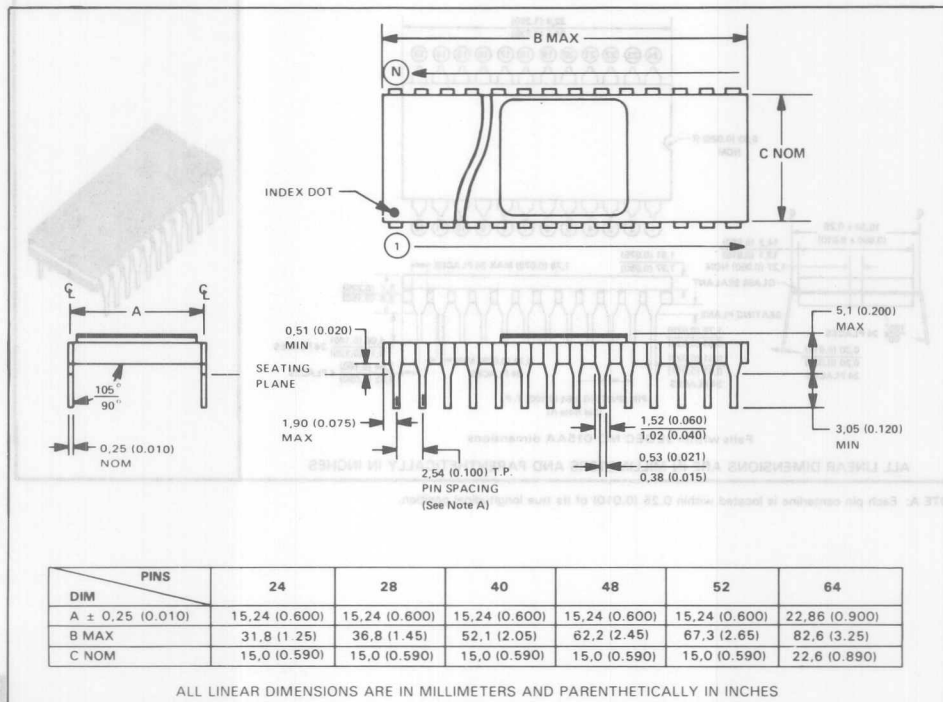


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

MECHANICAL DATA

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



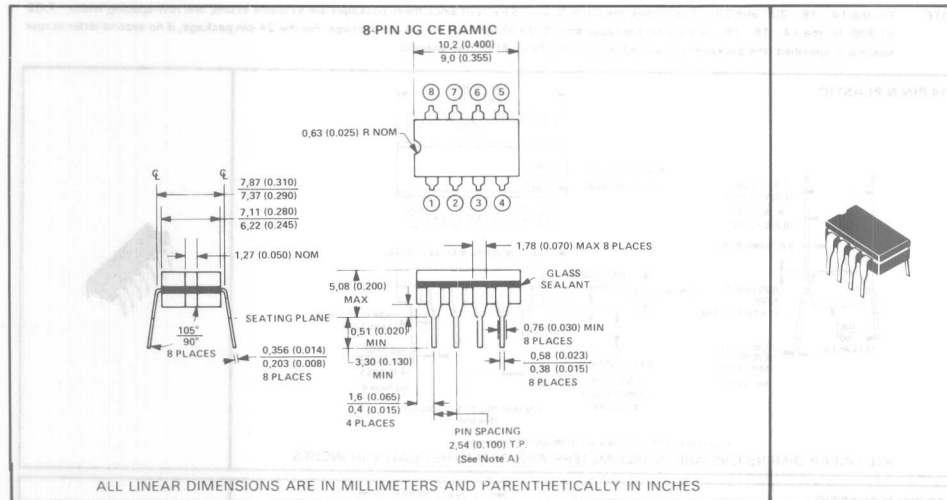
NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

4

MECHANICAL DATA

JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Non-shiny tin-plated leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.



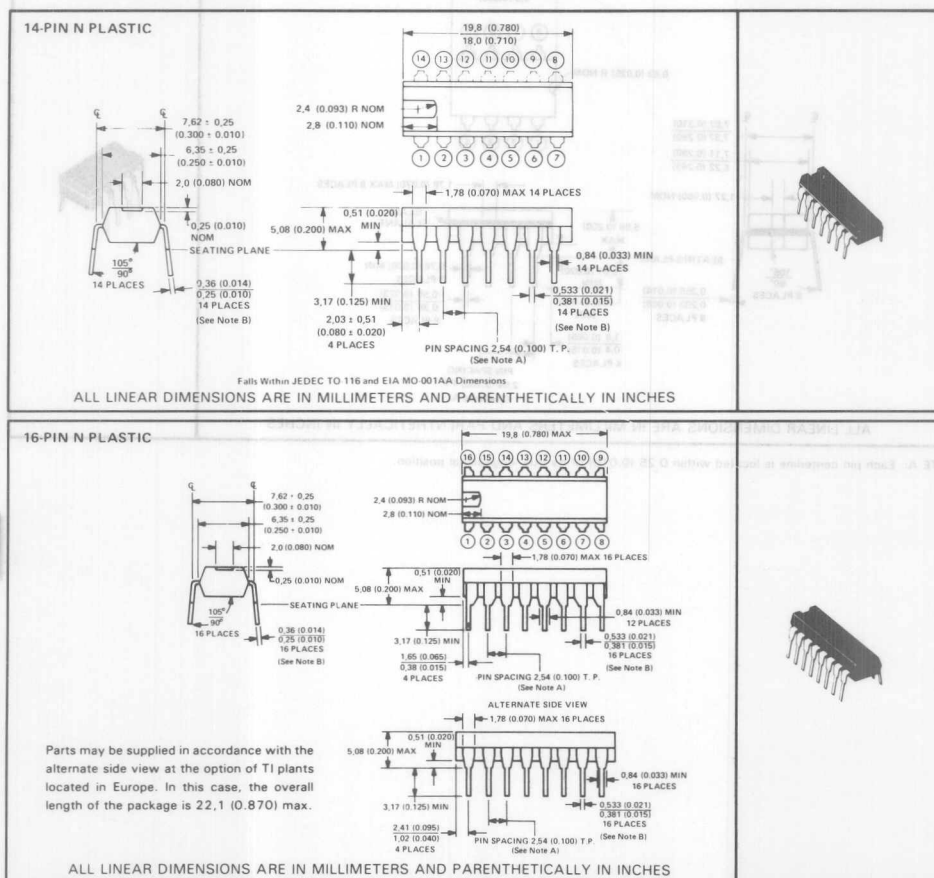
NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

MECHANICAL DATA

N plastic packages (including NT dual-in-package)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the NT package. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

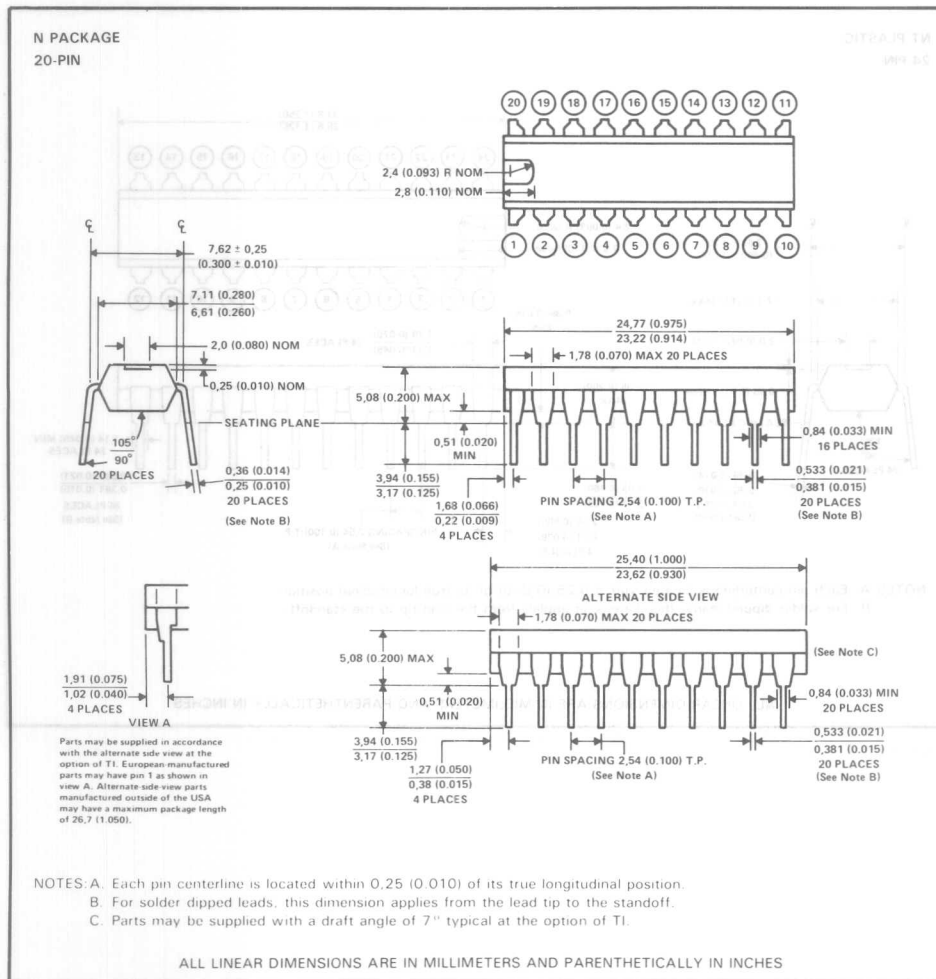
NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width - 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package. For the 24-pin package, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 B. For solder dipped leads, this dimension applies from the lead tip to the standoff.

N package

NT package



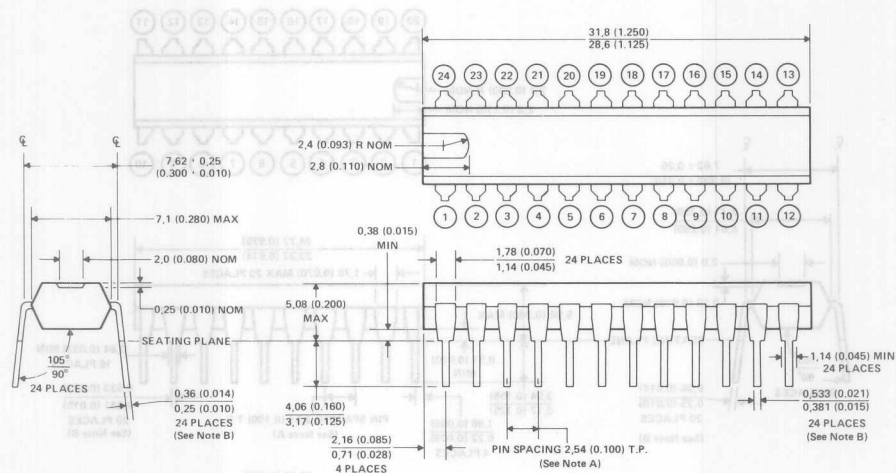
4

MECHANICAL DATA

MECHANICAL DATA

NT package

NT PLASTIC
24-PIN



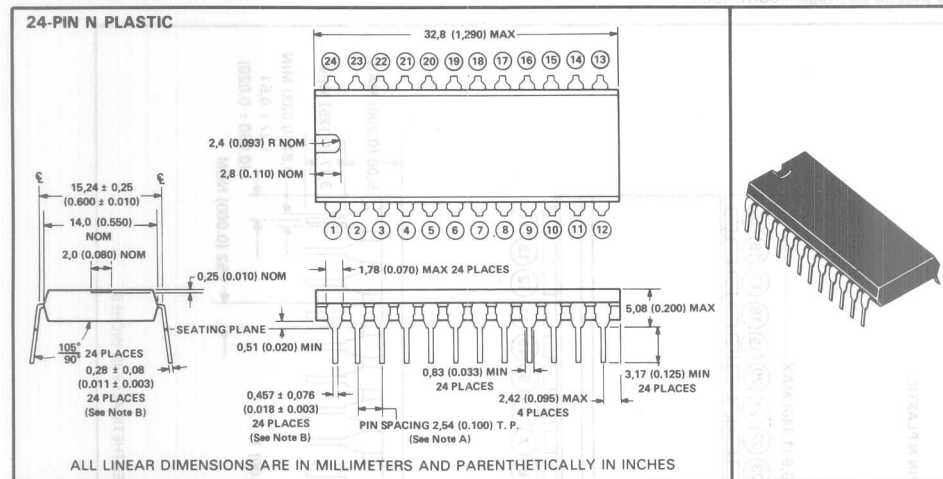
NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
B. For solder dipped leads, this dimension applies from the lead tip to the standoff.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHEMICALLY IN INCHES

4

MECHANICAL DATA

N plastic dual-in-line packages (continued)



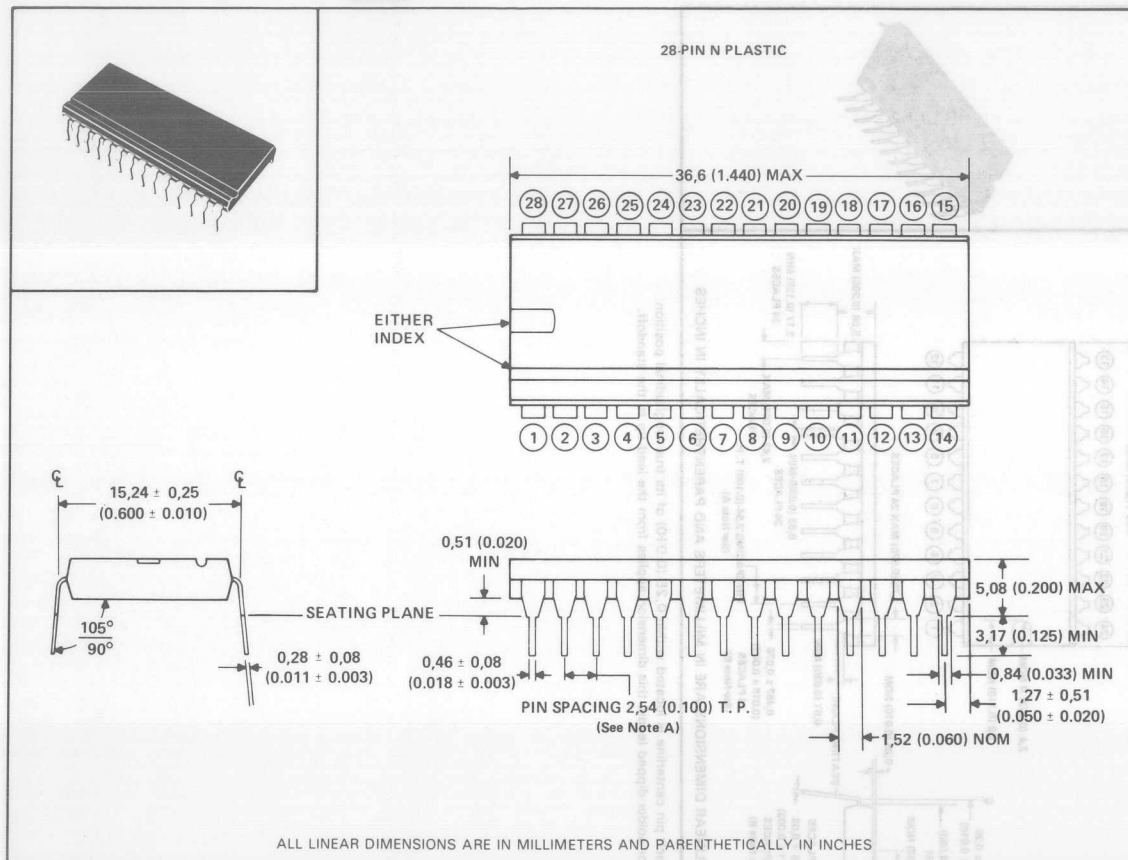
NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
 B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

MECHANICAL DATA

N plastic packages (continued)

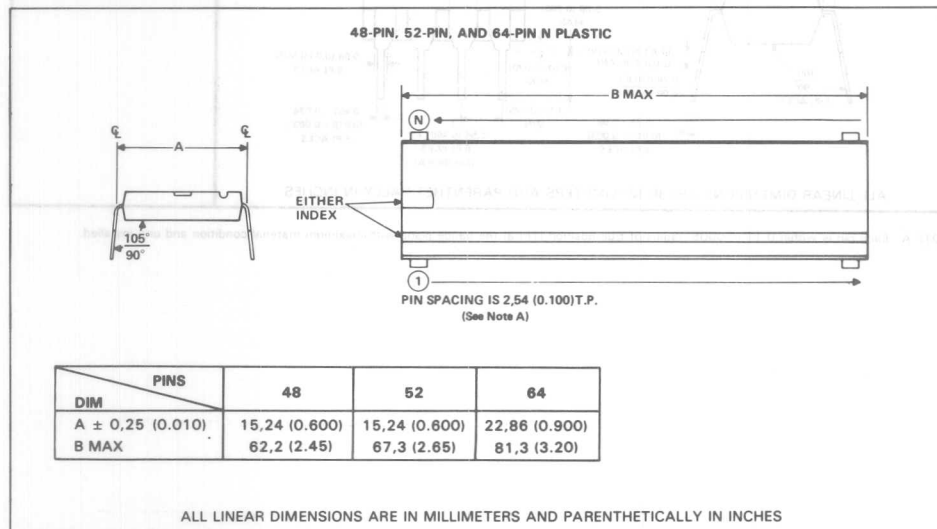
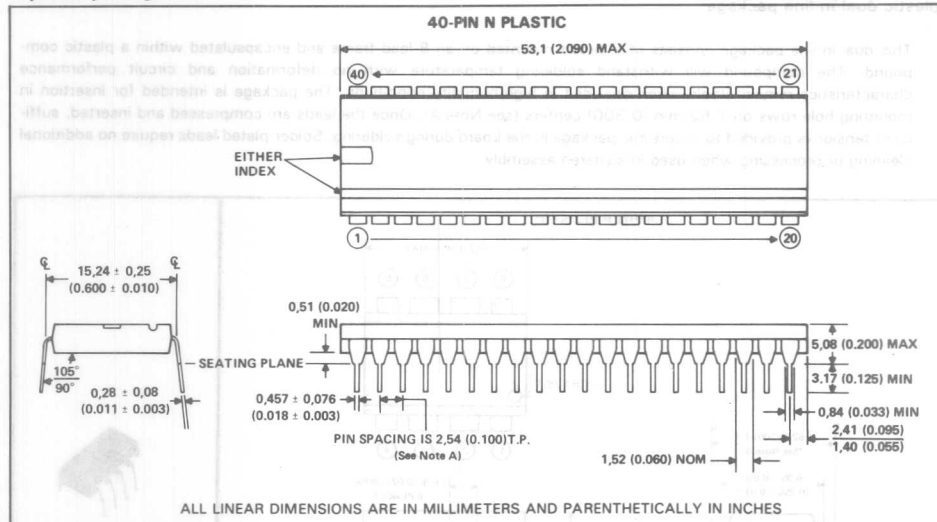
MECHANICAL DATA

4



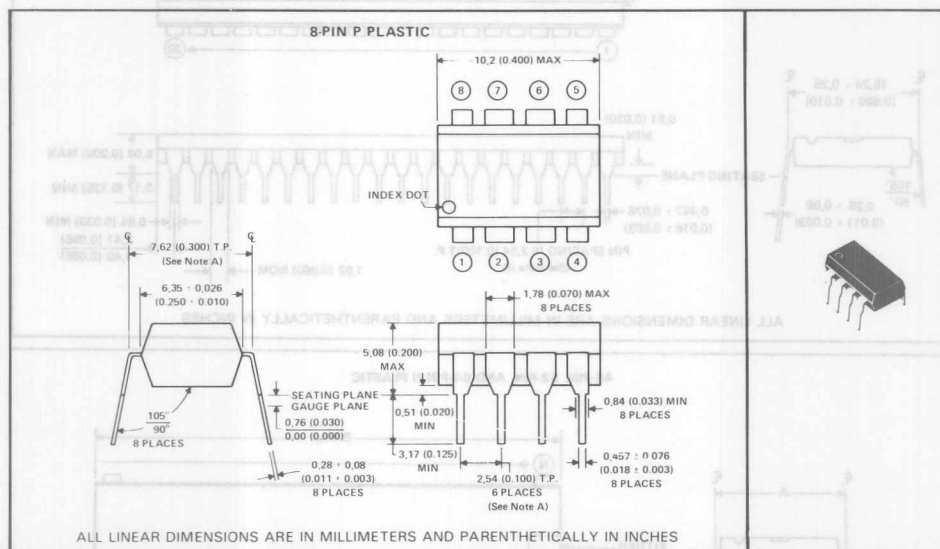
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic packages (continued)



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin is within 0.13 (0.0005) radius of true position (TP) at the gauge plane with maximum material condition and unit installed

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

0.152 (0.006)
0.076 (0.003)
14 LEADS

BASE AND SEATING PLANE

2.03 (0.080)
1.27 (0.050)

7.0 (0.275)
(See Note B)

21.84 (0.860)
21.34 (0.840)

(See Note C)

6.73 (0.265)
5.97 (0.235)

8.00 (0.315)
6.86 (0.270)

1.27 (0.050) TYP
12 PLACES
(See Note A)

0.483 (0.019)
0.381 (0.015)
14 LEADS

8.89 (0.350)
8.56 (0.337)

0.64 (0.025)
0.25 (0.010)
4 PLACES

1 2 3 4 5 6 7

Falls Within JEDEC MO-004AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHESTICALLY IN INCHES

The drawing illustrates the mechanical specifications of a JEDEC MO-004AG package. It includes a side view on the left showing the package height and base dimensions, and a top view on the right showing the pin layout and width. Dimensions are provided in both inches and millimeters, with millimeter values in parentheses.

Side View Dimensions:

- Top lead pitch: 0.152 (0.096) / 0.076 (0.003) / 16 LEADS
- Base and seating plane
- Lead height: 2.03 (0.080) / 1.27 (0.050)
- Body height: 7.62 (0.300) (See Note B)
- Body width: 24.38 (0.960) / 23.88 (0.940)
- Lead height (bottom): 1.02 (0.040) / 0.51 (0.020)

Top View Dimensions:

- Pin pitch: 8.89 (0.350) / 7.87 (0.310)
- Pin width: 0.483 (0.019) / 0.381 (0.015) / 16 LEADS
- Body width: 7.24 (0.285) / 6.27 (0.247) (See Note C)
- Pin height: 8.89 (0.350) / 7.87 (0.310)
- Pin spacing (center-to-center): 9.42 (0.371)
- Pin width (bottom): 0.64 (0.025) / 0.25 (0.010) / 4 PLACES
- Pin numbering: 1, 2, 3, 4, 5, 6, 7, 8

Falls Within JEDEC MO-004AG Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHESTICALLY IN INCHES

Table 1. Demographic characteristics of study population

MECHANICAL DATA

NOTES:

- A. Leads are within 0,13 (0.005) radius of true position (TP) at maximum material condition.
- B. This dimension determines a zone within which all body and lead irregularities lie.
- C. Index point is provided on cap for terminal identification only.
- D. End configuration of 24-pin package is at the option of TI.